THE BRITISH COMPUTER SOCIETY

THE BCS PROFESSIONAL EXAMINATIONS
BCS Level 5 Diploma in IT

COMPUTER ARCHITECTURE

29th April 2008, 10.00 a.m.-12.00 p.m.
Answer FOUR questions out of SIX. All questions carry equal marks.
Time: TWO hours.

*The marks given in brackets are **indicative** of the weight given to each part of the question.*

Only **non-programmable** calculators are allowed in this examination.

1. For the function:

f = A'B'C'D'+ A'BCD' + ABD + AC'D + A'B'D' + AB'C' + AB'CD

a) Construct a Karnaugh map and use it to find a minimum sum of products expression for f.

(4 marks)

b) Draw a logic circuit for the minimised expression using only AND, OR and NOT gates.

(4 marks)

c) Manipulate the minimised expression for f into a form which does not use the AND operator and hence draw a logic circuit for f using only NOR gates.

(5 marks)

d) Manipulate the minimised expression for f into a form which does not use the OR operator and hence draw a logic circuit for f using only NAND gates.

(5 marks)

e) Compare the relative merits of the logic circuit solutions to parts b, c and d.

(3 marks)

f) Discuss the relative merits of implementing the circuit for f as a VLSI chip.

(4 marks)

2.

a) The count sequence for a synchronous modulo six counter is shown in the table below:

state	Q2	Q1	Q0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1

i) By means of Karnaugh maps derive the minimised sum of products expressions for each stage of the counter if it is to be built from D type flipflops.

(7 marks)

ii) By means of Karnaugh maps derive the minimised sum of products expressions for each stage of the counter if it is to be built from JK type flipflops.

(7 marks)

iii) Draw the logic circuit for each of your counter designs and compare their relative merits.

(11 marks)

3.

a) Briefly discuss the memory hierarchy of a conventional digital computer in terms of access time and capacity.

(7 marks)

b) The strategy known as cache is used to enhance the performance of computer memory. Discuss its principles of operation and explain why it is so successful at reducing main store memory access times.

(12 marks)

c) Compare the cache memory strategy with that of virtual memory.

(6 marks)

4.

a) Draw a block diagram of a basic stored programme computer at the register level. Carefully label your diagram and explain the role of each of its main components in the machine code fetch / execute cycle.

(8 marks)

b) When a processor accesses RAM it may simply provide the address of the required memory location in what is called direct or absolute addressing mode. In all but the very simplest cases a range of different, less direct addressing modes is implemented.

i) Identify three such modes of indirect addressing and use your block computer diagram of part a) to illustrate how they would work.

ii) Explain why each of your chosen address modes might be included in support of the machine code instruction set of a typical computer.

(10 marks)

c) Explain the principles of the strategy known as Direct Memory Access and discuss its significance as a feature of a digital computer.

(7 marks)

5.

a) A computer is to be constructed from the list of components given in the table below. Calculate its reliability over 2000 hours. State clearly any assumptions you make in arriving at your answer.

component type	number in system	failure rate (% per 1000 hrs)
integrated circuits	25	0.0012
capacitors	52	0.019
resistors	27	0.006
Wire wraps	1424	0.00001

(14 marks)

b) Discuss three strategies that can be used to improve the *reliability* of a computer system by using redundancy at the component and/or system level.

(11 marks)

6.

a) Each new generation of computers based on the conventional von Neumann architecture is faster than the preceding one. This is in part due to advances in the fabrication technology of the integrated circuit components used to construct the machines. Discuss the assertion that “the physical laws governing the behaviour of circuit components and their interactions will soon limit further advances”.

(7 marks)

b) Outline the principles of operation of **either** a Quantum Computer or a Neural Network and explain how your chosen design may overcome some of the physical limitations that you discussed in part a) of this question.

(18 marks)