# THE BCS PROFESSIONAL EXAMINATIONS
# BCS Level 5 Diploma in IT

## April 2007

## EXAMINERS' REPORT

## COMPUTER ARCHITECTURE

**General comments**

Students are selective in answering questions. Generally questions on logic circuits and computer architecture are favourites. But then these days hardware is hardly the favourite subject for students.

**Question 1**

For the function:

f = AB'D'+ AC'D' + B'CD + AB'C + B'C + A'B'D' + AB'C'

a) Construct a Karnaugh map and use it to find a minimum sum of products expression for f.

**(4 marks)**

b) Draw a logic circuit for the minimised expression using only AND, OR and NOT gates.

**(4 marks)**

c) Manipulate the expression into a suitable form and hence draw a logic circuit using only NOR gates.

**(5 marks)**

d) Manipulate the expression into a suitable form and hence draw a logic circuit using only NAND gates.

**(5 marks)**

e) Compare the relative merits of the logic circuit solutions to parts b, c and d.

**(3 marks)**

f) Discuss the relative merits of implementing the above circuits in a logic array rather than using discrete gates.

**(4 marks)**

**Answer Pointers**

a) The karnaugh map for the given expression is:

| | A'B' | A'B | AB | AB' |
|---|---|---|---|---|
| C'D' | 1 | 0 | 1 | 1 |
| C'D | 0 | 0 | 0 | 1 |
| CD | 1 | 0 | 0 | 1 |
| CD' | 1 | 0 | 0 | 1 |

Hence: f = B'D' + B'C + AC'D'+ AB'

b) The logic gate circuit requires three NOT gates, four AND gates and one OR gate.

c) The expected solution using de Morgan's law is:

f = ( A' + B )' + ( B + C' )' + ( B + D )' + ( A' + C + D )'

The NOR circuit derived from the latter expression requires eight gates and has a maximum propagation delay path of four gates.

d) Using de Morgan's law the expression can be recast as:

f = ( ( A . B' )' . ( B' . C )' . ( B' . D' )' . ( A . C' . D' ) )'

The NAND circuit requires eight gates and has a maximum propagation delay path of three gates.

e) Comparing the circuits of parts (b), (c) and (d) it can be seen that all three circuits require eight gates. The propagation delay is longer for the NOR solution. The NAND circuit has the advantage of requiring only one type of gate.

f) Answers should demonstrate an understanding of what is meant by the term logic array. The relative merits would be based on cost and development time.

**Examiner's Guidance Notes**

The majority of candidates attempted this question and only a few ran into problems in parts a) to d). The comparison of relative merits in part e) was sometimes rather inventive. Few candidates were able to offer a convincing discussion of the relative merits of using a logic array as opposed to discrete gates for part f).

**Question 2**

a) Explain why in many applications synchronous counters are preferred to asynchronous counters.

**(4 marks)**

b) The count sequence for a synchronous counter is shown in the table below:

| state | Q3 | Q2 | Q1 | Q0 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 1 | 0 |
| 4 | 1 | 0 | 0 | 1 |
| 5 | 1 | 1 | 0 | 0 |
| 6 | 1 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 | 1 |
| 8 | 0 | 1 | 1 | 1 |
| 9 | 0 | 0 | 1 | 1 |
| 10 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 |

i) By means of Karnaugh maps derive the minimised sum of products expressions for each stage of the counter if it is to be built from JK flipflops.

**(16 marks)**

ii) Draw the logic circuit for your counter design using JK flip flops and, AND, OR and NOT gates.

**(5 marks)**

**Answer Pointers**

a) An asynchronous counter has a period when its outputs are changing in response to the ripple through during which their value is not valid. Although of short duration these values could cause incorrect operation of high speed circuits that receive them as inputs.

b) i) Minimised sum of products expressions for the JK inputs where $Q_0$ is the least significant bit:

$J_0 = Q_1$ $K_0 = Q_1'$

$J_1 = Q_2$ $K_1 = Q_2'$

$J_2 = Q_3$ $K_2 = Q_3'$

$J_3 = Q_0'. Q_2'$ $K_3 = Q_0. Q_2 + Q_0'. Q_2'$

ii) Correctly drawn circuit diagram requires 4 JK flip flops, 3 AND gates and an OR gate.

**Examiner's Guidance Notes**

This question was generally well answered. An area of weakness was in identifying any assumptions that underpinned the calculations. In part c) a few candidates discussed the use of redundant systems to optimise reliability in spite of this being specifically excluded in the question.

**Question 3**

a) The peripheral devices in a computer system are typically supported by individual interfaces. Explain the tasks that these interfaces must carry out.

**(7 marks)**

b) Compare the vectored interrupt and software poll strategies which are used to communicate requests for attention to the main system processor. Your answer must demonstrate that you understand the principles of operation of each strategy. Support your answer where possible with estimated times for the different stages of each strategy.

**(18 marks)**

**Answer Pointers**

a) The main tasks common to most peripheral interfaces are:

Matching electrical levels – the bus signals inside the computer enclosure are too weak to operate most real world devices or propagate far on external connections and too vulnerable to corruption by electrical noise in the external environment.

Matching speed requirements – processor time scales are of the order of nanoseconds whereas many real world devices cannot operate within several orders of magnitude of this figure. The processor in this way is not delayed whilst it waits for a slow device.

Taking delegated control – such issues as providing support for handshake signals, error management and flagging interrupt requests back to the processor. Intelligence is built into the interface so that it can take care of many of the tasks associated with communicating with a real world device and only involve the processor when its intervention is essential.

**(7 marks)**

b) The essential features of each strategy must be set out. For the software poll:

- each interface has a request flag
- the host processor checks the flags via a software routine
- the poll routine is run at intervals
- priority is determined by the order of the polling.

For the hardwired vector interrupt:

- The device interface asserts IRQ to the processor
- The processor checks the status of the IRQ input at the end of each fetch/execute cycle and branches to a handling routine as required if the request is of high enough priority
- The processor asserts an acknowledge signal to the interface
- The interface sends a vector number which is converted into a start address by the processor
- The current task is put on hold and the machine code environment saved

Estimates of the time for each operation should be given which must be consistent i.e. based consistently on a given clock speed / execution cycle time.

(**18 marks)**

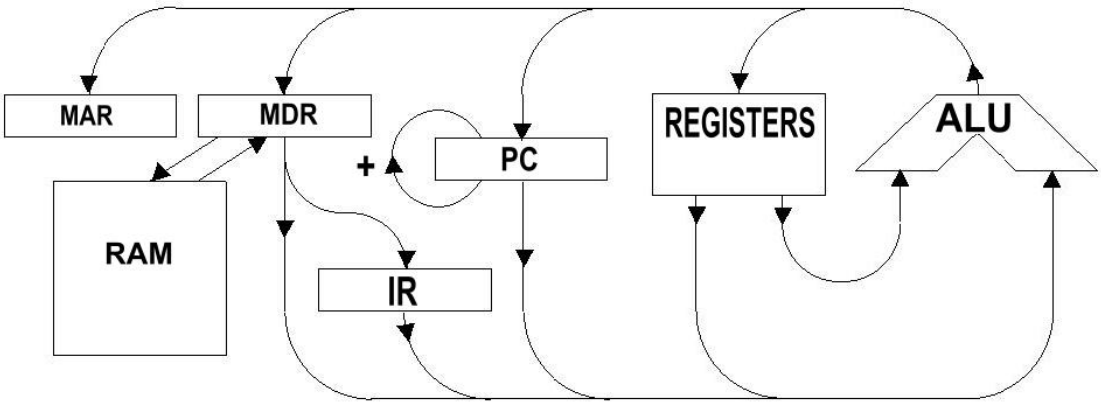
**Examiner's Guidance Pointers**

The few candidates that attempted this question made a solid response to the descriptive sections but the request for estimated times for the different strategies was largely ignored.

**Question 4**

a) The main features of a simple computer at the register level are shown diagrammatically in the figure below. Explain the function of each of these named features within the machine code fetch / execute cycle.

**(8 marks)**



b) The register transfer language below represents a fetch cycle being carried out by the simple computer in the figure above. Explain the small operations that are being carried out by each line of this code. You may assume that the machine code instructions have a single operand field and that a complete instruction can be read from memory in one read cycle.

(PC) > (MAR)
READ
(MDR) > (IR)
(PC) + 1 > (PC)
(IR) OPERATION CODE > CONTROL UNIT

**(3 marks)**

c) At the register transfer language level explain the steps that would be required to execute the following machine code instructions for the simple computer in the figure above. State carefully any assumptions you make.

i) Store the program counter
ii) Branch to subroutine

**(8 marks)**

d) Briefly discuss the assertion that "changing the processor in a given computer system for one that has a higher clockspeed will necessarily result in faster execution of programs".

**(6 marks)**

**Answer Pointers**

a) & b) The function of each feature should be made clear. For example the program counter holds an address value which indicates where the next instruction is held in memory. Its value is increased after an instruction is fetched and may be modified during the execute phase as in a branch instruction. Each line should be briefly interpreted as in:

(PC) > (MAR) The address of the next instruction which is held in the program counter is copied to the memory address register.

c) Any reasonable format for the register transfer language may be used but it must demonstrate an understanding of the simple moves required:

i) to copy the program counter contents to the memory data register, copy the operand of the instruction from the instruction register to the memory address register and cause a write operation before ending the execute phase.
ii) To copy the branch address from the operand in the instruction register to the program counter before ending the execute phase.

Any assumptions about address mode should be stated.

d) The assertion is not valid. There are a number of issues that may be put forward to refute it such as the fact that a higher clock speed does not necessarily mean the actual execution time of a given instruction will be reduced, machine code instruction sets may be less well matched to the problem in hand, there may be more parallelism in the processor with the lower clock speed or more cache.

**Examiner's Guidance Notes**

Candidates demonstrated a good understanding of the basic architecture of the stored program computer. They were able to read and write the register transfer language required in sections b) and c) but were sometimes confused about the addresses required for part c). In the final part of the question candidates either understood how to answer or had no idea at all.

**Question 5**

a) Discuss how the failure rate of computer components varies with time and explain the significance of the term *accelerated life testing*.

**(6 marks)**

b) A computer is to be constructed from the list of components given in the table below. Calculate its reliability over 1500 hours. State clearly any assumptions you make in arriving at your answer.

| component type | number in system | failure rate (% per 1000 hrs) |
|---|---|---|
| integrated circuits | 17 | 0.0017 |
| capacitors | 35 | 0.023 |
| resistors | 22 | 0.007 |
| Wire wraps | 812 | 0.00001 |

**(14 marks)**

c) Discuss the steps that can be taken to optimise the *reliability* of a computer system apart from building in redundancy.

**(5 marks)**

**Answer Pointers**

a) The failure rates for components follow a bathtub curve when plotted against time. This starts with relatively high failure rates due to 'infant mortality', moves into a linear region of low failure rate before climbing to higher levels due to the aging of components. Accelerated life testing is a technique used to estimate failure rates for highly reliable components. Rather than wait for what may be years to get a statistically acceptable sample of failures the components are subjected to increased power levels to promote early failure and then the results scaled back to estimate the failure rates in normal service.

b) The system failure rate is the sum of the failure rates of all the components in the system:

Failure rate for integrated circuits = 17 * 0.0017 = 0.0289
Failure rate for capacitors = 35 * 0.023 = 0.805
Failure rate for resistors = 22 * 0.007 = 0.154
Failure rate for wire wraps = 812 * 0.00001 = 0.00812

Hence the system failure rate = 0.996 failures percent per 1000 hrs
= 0.996* 10^-5 failures per hour

The Exponential failure law: R = e^-(failure rate)*(time)

gives a reliability of 0.985 at 1500 hours.

The expected assumptions are that failure rates are not a function of time, a single failure pulls down the system and that components fail independently of each other.

c) High quality, burnt-in components should be used in the initial construction of the system. They should be specified so that they run well inside their electrical power ratings. The computer should run in a well controlled environment which offers steady temperatures and is free of vibrations. Temperature cycling caused by turning the system power on and off should be avoided.

**Examiner's Guidance Notes**

Most candidates who attempted this question were able to derive an accurate state table but a significant number were not able to successfully convert this into minimised expressions for the J K inputs of the flip flops. Those who did obtain suitable minimised expressions did not have any difficulty in drawing the appropriate logic circuit.

**Question 6**

The von Neumann, stored programme computer has had a very long and successful reign. Explain some of its limitations and discuss one alternative architecture which may overcome some of these limitations.

**(25 marks)**

**Answer Pointers**

The discussion of the limitations imposed by the known physical laws should address most of the topics listed below:

- velocity of light as the ultimate signal speed;
- storage of one bit per electron;
- heat dissipation – faster circuits, more heat;
- miniaturization – ability to draw finer detail;
- quantum tunnelling.

An outline discussion of the principles of operation of one novel computer architecture should be given together with a discussion of how it might mitigate some of the physical limitations discussed in the earlier part of the question.

**Examiner's Guidance Notes**

This question was only attempted by a few candidates and although the limitations of the von Neumann architecture were usually identified ideas about alternative architectures were sketchy.