THE BRITISH COMPUTER SOCIETY

THE BCS PROFESSIONAL EXAMINATIONS
BCS Level 5 Diploma in IT

COMPUTER ARCHITECTURE

27th April 2007, 10.00 a.m.-12.00 p.m.
Answer FOUR questions out of SIX. All questions carry equal marks.
Time: TWO hours.

*The marks given in brackets are **indicative** of the weight given to each part of the question.*

Only **non-programmable** calculators are allowed in this examination.

1. For the function:

f = AB'D'+ AC'D' + B'CD + AB'C + B'C + A'B'D' + AB'C'

a) Construct a Karnaugh map and use it to find a minimum sum of products expression for f. **(4 marks)**

b) Draw a logic circuit for the minimised expression using only AND, OR and NOT gates. **(4 marks)**

c) Manipulate the expression into a suitable form and hence draw a logic circuit using only NOR gates. **(5 marks)**

d) Manipulate the expression into a suitable form and hence draw a logic circuit using only NAND gates. **(5 marks)**

e) Compare the relative merits of the logic circuit solutions to parts *b), c)* and *d).* **(3 marks)**

f) Discuss the relative merits of implementing the above circuits in a logic array rather than using discrete gates. **(4 marks)**

2. *a)* Discuss how the failure rate of computer components varies with time and explain the significance of the term *accelerated life testing.* **(6 marks)**

b) A computer is to be constructed from the list of components given in the table below. Calculate its reliability over 1500 hours. State clearly any assumptions you make in arriving at your answer.

component type	number in system	failure rate (% per 1000 hrs)
integrated circuits	17	0.0017
capacitors	35	0.023
resistors	22	0.007
Wire wraps	812	0.00001

(14 marks)

c) Discuss the steps that can be taken to optimise the *reliability* of a computer system apart from building in redundancy. **(5 marks)**

3. *a)* The peripheral devices in a computer system are typically supported by individual interfaces. Explain the tasks that these interfaces must carry out. **(7 marks)**

b) Compare the vectored interrupt and software poll strategies which are used to communicate requests for attention to the main system processor. Your answer must demonstrate that you understand the principles of operation of each strategy. Support your answer where possible with estimated times for the different stages of each strategy. **(18 marks)**

4. *a)* The main features of a simple computer at the register level are shown diagrammatically in **Figure 1** below. Explain the function of EACH of these named features within the machine code fetch/execute cycle. **(8 marks)**

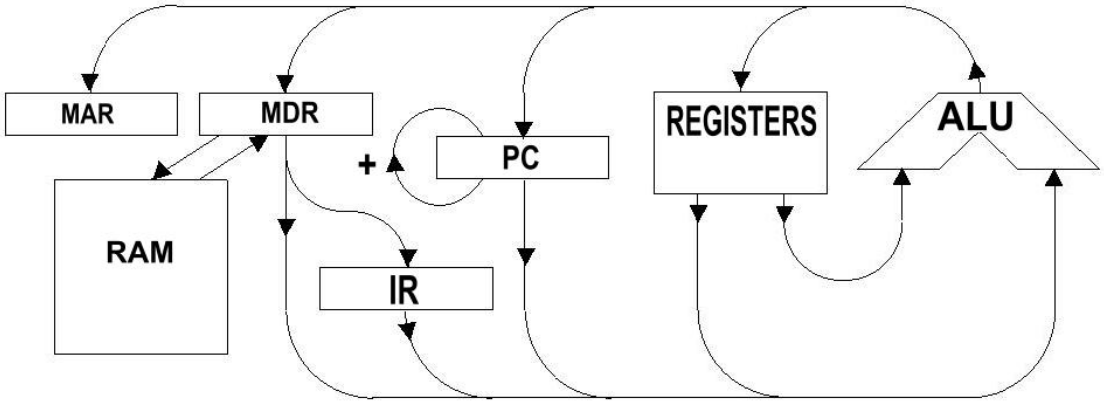

Figure 1

b) The register transfer language below represents a fetch cycle being carried out by the simple computer in **Figure 1**. Explain the small operations that are being carried out by each line of this code. You may assume that the machine code instructions have a single operand field and that a complete instruction can be read from memory in one read cycle.

(PC) > (MAR)
READ
(MDR) > (IR)
(PC) + 1 > (PC)
(IR) OPERATION CODE > CONTROL UNIT **(3 marks)**

c) At the register transfer language level explain the steps that would be required to execute the following machine code instructions for the simple computer in **Figure 1**. State carefully any assumptions you make.

i) Store the program counter
ii) Branch to subroutine **(8 marks)**

d) Briefly discuss the assertion that "changing the processor in a given computer system for one that has a higher clockspeed will necessarily result in faster execution of programs". **(6 marks)**

5. *a)* Explain why in many applications synchronous counters are preferred to asynchronous counters. **(4 marks)**

b) The count sequence for a synchronous counter is shown in the table below:

state	Q3	Q2	Q1	Q0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	1	0	0	1
5	1	1	0	0
6	1	1	1	0
7	1	1	1	1
8	0	1	1	1
9	0	0	1	1
10	0	0	0	1
0	0	0	0	0

i) By means of Karnaugh maps derive the minimised sum of products expressions for each stage of the counter if it is to be built from JK flipflops. **(16 marks)**

ii) Draw the logic circuit for your counter design using JK flip flops and, AND, OR and NOT gates. **(5 marks)**

6. The von Neumann, stored programme computer has had a very long and successful reign. Explain some of its limitations and discuss one alternative architecture which may overcome some of these limitations. **(25 marks)**