

**THE BCS PROFESSIONAL EXAMINATIONS
Diploma**

April 2006

EXAMINERS' REPORT

Architecture

Question 1

1. For the function:

$$f = A'B'C + A'BCD' + ABC'D + BCD + AB'C'D' + ABC'D'$$

- a) Construct a Karnaugh map and use it to find a minimum sum of products expression for f. **(4 marks)**
- b) Draw a logic circuit for the minimised expression using only AND, OR and NOT gates. **(4 marks)**
- c) Manipulate the expression into a suitable form and hence draw a logic circuit using only NAND gates. **(5 marks)**
- d) Show by means of the drop sets that the expression for f can be written in a way that does not use the AND operator. Hence draw a logic circuit for f using only NOR gates. **(5 marks)**
- e) Compare the relative merits of the logic circuit solutions to parts b), c) and d). **(3 marks)**
- f) Discuss the relative merits of implementing the circuit for f as a VLSI chip. **(4 marks)**

Answer Pointers

a) The Karnaugh map:

	AB				
CD		00	01	11	10
00		0	0	1	1
01		0	0	1	0
11		1	1	1	0
10		1	1	0	0

Thus: $f = A'C + AC'D' + ABD$

- b) The circuit requires three not gates, three and gates and an or gate. Maximum of three gates propagation delay.
- c) By de Morgan $f = ((A'C)' + (AC'D')' + (ABD)')'$

The circuit requires seven nand gates. Maximum of three gates propagation delay.

d) From the drop sets $f' = A'C' + ACD' + ABD'$

thus by de Morgan $f = ((A + C)' + (A' + C' + D)' + (A' + B + D'))'$

The circuit requires seven nor gates. Maximum of three gates propagation delay.

e) Comparison based on the number of gates, propagation delays and circuit board area / cost.

f) A very simple circuit to implement in VLSI with all its development overheads but might be practical if a VLSI circuit of much greater complexity were to share the chip.

Question 2

2. a) The count sequence for a synchronous decade counter is shown in the table below:

State	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

b) By means of Karnaugh maps derive the minimised sum of products expressions for each stage of the counter if it is to be built from JK flipflops. **(14 marks)**

c) Draw the logic circuit for the decade counter using JK flip flops, AND, OR and NOT gates. **(6 marks)**

d) Explain how your decade counter would behave if it entered an unused state such as 12 i.e. $Q3 = 1, Q2 = 1, Q1 = 0, Q0 = 0$. **(5 marks)**

Answer Pointers

a) i) $J3 = Q2.Q1.Q0$ $K3 = Q0$

$J2 = Q1.Q0$ $K2 = J2$

$J1 = Q3'.Q0$ $K1 = Q0$

$J0 = K0 = 1$

ii) The circuit for the counter requires four JK flip flops and three and gates.

iii) The answer depends on how the unused states have been treated in the design. This design would step from state 12 to state 13.

Question 3

3. a) Explain what is meant by the terms *failure rate* and *reliability*. (6 marks)
- b) A computer is to be built from the components listed in the table below. Calculate how reliable it will be over a 950 hour period. You must state any assumptions you make and clearly show your working. (10 marks)

Component Type	Number in System	Failure Rate (% per 1000 hrs)
integrated circuits	14	0.0013
capacitors	35	0.018
resistors	60	0.006
soldered joints	1080	0.00005

- c) It is proposed that a cooling fan be included in the computer of part b). If it has a failure rate of 2.1 % per 1000 hrs calculate how it will alter the reliability of the computer and discuss your result. (5 marks)
- d) Briefly compare the merits of strategies that can be used to increase the reliability of the computer of part b). (4 marks)

Answer Pointers

- a) The failure rate for components is the number of failures per unit time compared with the number of non-failed components. Reliability is the probability of non-failure over a given period of time.
- b) The system failure rate is found from the sum of the failure rates of all components in the system and is 1.0622 % per 1000 hours or 1.0622×10^{-5} failures per hour.

From the reliability equation $R = e^{-\text{failure rate} \times \text{time}}$ we get $R = 0.99$ or 99%.

The assumptions are that:

Failure rate is not a function of time.
A single component failure causes the system to fail.
Component failures are independent of one another.

- c) Adding the failure rate for the fan and recalculating gives $R = 0.97$ or 97%.
- d) The discussion should be based on the gain in reliability against the cost.

Most of the following limitations of current technologies should be discussed:

Ultimate signal speed limited by velocity of light
Shorter paths mean higher packing density but higher speeds also imply more waste heat generation with rising problems in terms of cooling.
Smaller storage elements mean fewer electrons per bit so that eventually the limit of one electron per bit will be reached.
Smaller, more densely packed circuits require ever finer drawing tools visible wavelength light is already approaching its limit.
Quantum effects start to dominate at small scales and in particular tunnelling causes what amount to unwanted signal paths.

This is a fairly open question and answers will be judged on their merits in terms of the understanding of the principles of the chosen architecture and how it is shown to address some of the issues identified in the earlier part of the question.

Question 4

4. a) A processor has word length of 32 bits. For a fixed point number representation in 2's complement, determine the number range for this representation. **(4 marks)**
- b) A peripheral with a parallel interface produces 14 bit word length 2's complement (signed) data, e.g. from an analog to digital converter. Where would you place this data in the 32 bit processor word and how would you fill the remaining 18 bits? Justify your answer. **(4 marks)**
- c) Describe in detail the content of each of the fields of the IEEE 754 single precision floating-point standard. Show the representation of the decimal numbers 0.75 and -49.5. **(6 marks)**
- d) How does the IEEE 754 single precision standard deal with overflow and underflow? **(5 marks)**
- e) Show the steps involved in adding two single precision floating point numbers. Illustrate your answer using the addition of 0.75 and -49.5. **(6 marks)**

Answer Pointers

- a) Number range is -2^{31} to $+2^{31} - 1$ or equivalent binary or decimal representations.
- b) Most significant 14 bits, remaining digits filled with zeroes.
or
Least significant 14 Bits, remaining digits filled with copies of the sign digit.
or
Somewhere in the middle, with copies of the sign digit for more significant digits and zeroes for less significant digits

Choice depends on the application. The issue here is the 14 bit 2's complement numbers are not a standard data type, so some conversion is necessary.

- c)
- | Sign | Exponent | Fraction | (Bias) |
|-------|-----------|------------|--------|
| 1[31] | 8 [30-23] | 23 [22-00] | (127) |

$0.75 = 0.5 + 0.25 \equiv 0.11$ in binary. Hence the Exponent is 01111111 and the mantissa is 100000000000000000000000

So the answer is 0 01111111 100000000000000000000000

$49.5 = 32 + 16 + 0 + 0 + 0 + 1 + \frac{1}{2} \equiv 110001.1$

Normalise this as .1100011 (shift right by 6 places)

So the answer should be: 1 1000101 100011000000000000000000

- d) The single precision floating point numbers still has a limited number range. Thus overflow can occur in either a positive or negative sense.
Positive overflow occurs when the result of an arithmetic operation leads to numbers greater than $(2-2^{-23}) * 2^{127}$
Negative overflow occurs when the result of an arithmetic operation leads to numbers less than $-(2-2^{-23}) * 2^{127}$

Either of these conditions sets the V flag in the status register or equivalent.

Positive or negative underflow simply signals a loss of precision, and occurs for numbers greater than -2^{-149} or less than 2^{-149} . This may be signalled to indicate that perhaps the equations are ill conditioned.

e)
0.75 = 0 01111111 100000000000000000000000
-49.5 = 1 1000101 100011000000000000000000

The largest number is -49.5, so we adjust the smaller number to have the same exponent, i.e. shift right by 6 places:

0 1000101 000001100000000000000000 and add the other number:
1 1000101 100011000000000000000000 but take the sign into account

.....
Result is: 1 1000101 100001100000000000000000 Result is already normalised.
In decimal this is $-(.5 + .25 + .0078175 + .0039087) * 64 = -48.75$

Question 5

5. a) Describe the following processor addressing modes:
- i) Immediate
 - ii) Direct
 - iii) Indirect
 - iv) Register
- (5 marks)**
- b) Indicate where each of these might be employed in a processor with a RISC load/store architecture.
- (6 marks)**
- c) List the functions of each of the bits you might expect to find in a processor status register.
- (6 marks)**
- d) Describe how these bits are set and used in relation to each of the following instruction types:
- i) SUB (Subtract)
 - ii) BNE (Branch if Negative or Equal)
 - iii) ADC (Add with Carry)
 - iv) IEN (Interrupt Enable)
- (8 marks)**

Answer Pointers

- a) i) Immediate - The address is the data
ii) Direct - The address points to the data
iii) Indirect - The address points to the location which contains the address of the data
iv) Register - The address is that of the register containing the data
- b) i) Immediate - Used to specify literals or constants.
ii) Direct - Used for load and store data
iii) Indirect - Used for load and store of data through a pointer
iv) Register - Used for register to register arithmetic

c) Basic: N, Z, C, V

Additional: IEN, INTON, BUSEN, DMAEN, etc.

d) i) SUB (Subtract)

This is an arithmetic operation. Therefore after completion:

Z is set if the result is Zero

N is set if the result is Negative

C is set if there was a Carry

V is set if there was an overflow.

ii) BNE (Branch if Negative or Equal)

This conditional branch takes place if either N or Z is set, else execution of instructions continues at PC+1

iii) ADC (Add with Carry)

The addition takes place with the adder carry-in set to 1 if C is set

iv) IEN (Interrupt Enable)

Sets IEN to 1, which enables interrupts to be recognised after execution of this instruction

Question 6

6. a) Describe the OSI 7-Layer model. Give a brief description of the services provided by each layer of the model. **(10 marks)**
- b) Explain the concept of a packet in this context. Identify the information to be found in a packet header and give its purpose. **(5 marks)**
- c) Briefly describe each of the following: Local Area Network (LAN), Metropolitan Area Network (MAN), Wide Area Network (WAN) **(6 marks)**
- d) Identify the main differences between these three network types. **(4 marks)**

ISO 7 Layer Model

The ISO/OSI model describes computer communication services and protocols, without making assumptions concerning:

- programming language bindings
- operating system bindings
- application and user interface issues

A model is simply a way of organizing knowledge and provides the common basis for discussion.

The ISO OSI Reference Model is a layered model - with each layer providing certain services and calling upon the services of other layers.

7 Application layer

responsible for managing the communication between the applications

6 Presentation Layer

provides common operations on the structure of data being exchanged

- Syntax Conversion
 - Encryption
 - Compression
-

5 Session Layer

Provides the control structure for managing communications

- establishing
 - managing
 - terminating sessions (connections).
-

4 Transport Layer

Provides reliable transparent data transfer between end points (there may be more than two end points)

- provide error recovery and flow control.
-

3 Network Layer

Makes the upper layers independent of the data transmission, switching technologies, and topology of the network

- determine which path (or paths) in the network that a given unit of data will take (routing).
-

2 Link Layer

Provides reliable transfer across the physical links

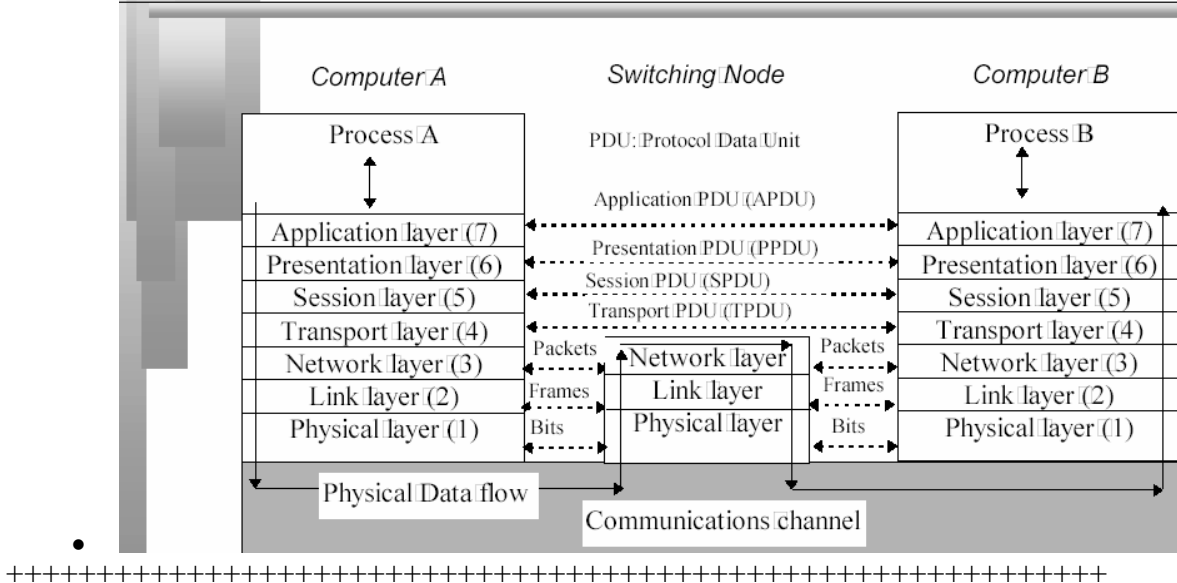
- establishes the beginning and end of blocks of data (with synchronization when necessary) [framing];
 - error detection and possibly correction;
 - (link) flow control.
-

1 Physical Layer

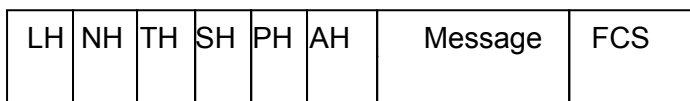
Provides transmission of unstructured bits across the physical medium

- electrical
- optical
- mechanical

THE ISO/ITU-T OSI REFERENCE MODEL



b) (the concept of a packet....etc)



- LH – Link Header
- NH – Network Header
- TH – Transport Header
- SH – Session Header
- PH – Presentation Header
- AH – Application Header
- FCS – Frame Check Sequence (Link Trailer)

c) Local Area Network (LAN): Inside building or set of buildings

Metropolitan Area Network (MAN): LAN-like technologies over km distances
e.g. towns/cities

Wide Area Network (WAN): Distances of many kilometres up to worldwide

d) LANS and MANS employ broadcast technology, e.g. each transmission is to all computers on the network. MANS are more hierarchical.

WANS typically employ mesh networks of nodes (switches and routers) with computers attached at to edge nodes with typically with connectionless, packet routing and forwarding.