THE BRITISH COMPUTER SOCIETY

THE BCS PROFESSIONAL EXAMINATIONS
Diploma

ARCHITECTURE

21st April 2006, 10.00 a.m.-12.00 p.m.
Answer FOUR questions out of SIX. All questions carry equal marks.
Time: TWO hours.

*The marks given in brackets are **indicative** of the weight given to each part of the question.*

1. For the function:

$$f = A'B'C + A'BCD' + ABC'D + BCD + AB'C'D' + ABC'D'$$

   a)   Construct a Karnaugh map and use it to find a minimum sum of products expression for f.   **(4 marks)**

   b)   Draw a logic circuit for the minimised expression using only AND, OR and NOT gates.   **(4 marks)**

   c)   Manipulate the expression into a suitable form and hence draw a logic circuit using only NAND gates.
   (5 marks)

   d)   Show by means of the drop sets that the expression for f can be written in a way that does not use the AND operator. Hence draw a logic circuit for f using only NOR gates.   **(5 marks)**

   e)   Compare the relative merits of the logic circuit solutions to parts *b), c)* and *d)*.   **(3 marks)**

   f)   Discuss the relative merits of implementing the circuit for f as a VLSI chip.   **(4 marks)**

2.   a)   The count sequence for a synchronous decade counter is shown in the table below:

State	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

   b)   By means of Karnaugh maps derive the minimised sum of products expressions for each stage of the counter if it is to be built from JK flipflops.   **(14 marks)**

   c)   Draw the logic circuit for the decade counter using JK flip flops, AND, OR and NOT gates.   **(6 marks)**

   d)   Explain how your decade counter would behave if it entered an unused state such as 12 i.e. Q3 = 1, Q2 =1, Q1 = 0, Q0 = 0.   **(5 marks)**

Turn over]

3. *a)* Explain what is meant by the terms *failure rate* and *reliability*. **(6 marks)**

b) A computer is to be built from the components listed in the table below. Calculate how reliable it will be over a 950 hour period. You must state any assumptions you make and clearly show your working. **(10 marks)**

Component Type	Number in System	Failure Rate (% per 1000 hrs)
integrated circuits	14	0.0013
capacitors	35	0.018
resistors	60	0.006
soldered joints	1080	0.00005

c) It is proposed that a cooling fan be included in the computer of part *b)*. If it has a failure rate of 2.1 % per 1000 hrs calculate how it will alter the reliability of the computer and discuss your result. **(5 marks)**

d) Briefly compare the merits of strategies that can be used to increase the reliability of the computer of part *b)*. **(4 marks)**

4. *a)* A processor has word length of 32 bits. For a fixed point number representation in 2's complement, determine the number range for this representation. **(4 marks)**

b) A peripheral with a parallel interface produces 14 bit word length 2's complement (signed) data, e.g. from an analog to digital converter. Where would you place this data in the 32 bit processor word and how would you fill the remaining 18 bits? Justify your answer. **(4 marks)**

c) Describe in detail the content of each of the fields of the IEEE 754 single precision floating-point standard. Show the representation of the decimal numbers 0.75 and -49.5. **(6 marks)**

d) How does the IEEE 754 single precision standard deal with overflow and underflow? **(5 marks)**

e) Show the steps involved in adding two single precision floating point numbers. Illustrate your answer using the addition of 0.75 and -49.5. **(6 marks)**

5. *a)* Describe the following processor addressing modes:
   i) Immediate
   ii) Direct
   iii) Indirect
   iv) Register **(5 marks)**

b) Indicate where each of these might be employed in a processor with a RISC load/store architecture. **(6 marks)**

c) List the functions of each of the bits you might expect to find in a processor status register. **(6 marks)**

d) Describe how these bits are set and used in relation to each of the following instruction types:
   i) SUB (Subtract)
   ii) BNE (Branch if Negative or Equal)
   iii) ADC (Add with Carry)
   iv) IEN (Interrupt Enable) **(8 marks)**

6. *a)* Describe the OSI 7-Layer model. Give a brief description of the services provided by each layer of the model. **(10 marks)**

    b) Explain the concept of a packet in this context. Identify the information to be found in a packet header and give its purpose. **(5 marks)**

    c) Briefly describe each of the following: Local Area Network (LAN), Metropolitan Area Network (MAN), Wide Area Network (WAN) **(6 marks)**

    d) Identify the main differences between these three network types. **(4 marks)**