

**THE BCS PROFESSIONAL EXAMINATIONS
Diploma**

April 2005

EXAMINERS' REPORT

Architecture

Question 1

1. For the function:

$$f = A'B'D' + A'BD + BC'D + BCD + AB'C + AB'C'D'$$

- a) Construct a Karnaugh map and use it to find a minimum sum of products expression for f . **(4 marks)**
- b) Draw a logic circuit for the minimised expression using only AND, OR and NOT gates. **(4 marks)**
- c) Manipulate the expression into a suitable form and hence draw a logic circuit using only NAND gates. **(5 marks)**
- d) Manipulate the expression into a suitable form and hence draw a logic circuit using only NOR gates. **(5 marks)**
- e) Compare the relative merits of the logic circuit solutions to parts c) and d). **(3 marks)**
- f) Discuss the relative merits of TWO hardware implementation strategies for the above circuits that are not based on discrete gates. **(4 marks)**

Answer Pointers

(a) The karnaugh map for the given expression is:

	A'B'	A'B	AB	AB'
C'D'	1	0	0	1
C'D	0	1	1	0
CD	0	1	1	1
CD'	1	0	0	1

Hence: $f = B'D' + BD + ACD$ **(4 marks)**

(b) The logic gate circuit requires two NOT gates, three AND gates and one OR gate. **(4 marks)**

(c) Using de Morgan's law the expression can be recast as:

$$f = ((B'D')' \cdot (B \cdot D)' \cdot (A \cdot C \cdot D))'$$

The NAND circuit requires six gates and has a maximum propagation delay path of three gates. **(5 marks)**

(d) The expected solution using de Morgan's law is:

$$f = (B' + D')' + (B + D)' + (A' + C' + D')$$

The NOR circuit derived from the latter expression requires nine gates and has a maximum propagation delay path of four gates. (5 marks)

(e) Comparing the circuits of parts (c) and (d) it can be seen that the NOR solution requires more gates and has a greater propagation delay. (3 marks)

(f) Comparisons could be made with implementing the circuit in a form of gate array or in VLSI. The relative merits would be based on cost and development time. (4 marks)

Examiner's Comments

Although most candidates successfully marked up the Karnaugh map some encountered difficulty in reading from it the simplified sum of products expression. A common error was to miss the group of four terms at the corners of the map and as a result get an expression which was not properly minimised.

Candidates had mixed success in recasting the expression into a form suitable for implementation exclusively in NOR or NAND gates. De Morgan's law was usually cited but not always successfully applied.

There was a minor error in part e) which should have asked for a comparison between parts c) and d). All candidates recognised what was intended and answers were generally sound.

Candidates did not tackle the final part of the question with any confidence and often did not attempt it at all.

Question 2

2. The count sequence for a modulo 8 synchronous counter is shown in the table below:

State	Q2	Q1	Q0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

- i) By means of Karnaugh maps derive the minimised sums of products expressions for each stage of the counter if it is to be built from D-type flipflops.
- ii) By means of Karnaugh maps derive the minimised sums of products expressions for each stage of the counter if it is to be built from JK flipflops.
- iii) Draw the logic circuit for each counter design using the appropriate flipflops and AND, OR and NOT gates. Compare the two designs. (20 marks)

Answer Pointers

(i) Minimised sum of products expressions for the D-type F-F where Q_0 is the least significant bit:

$$D_0 = Q_0$$

$$D_1 = Q_1 \cdot Q_0' + Q_1' \cdot Q_0$$

$$D_2 = Q_2 \cdot Q_0' + Q_2 \cdot Q_1' + Q_2' \cdot Q_1 \cdot Q_0$$

(6 marks)

(ii) Minimised sum of products expressions for the JK-type F-F where Q_0 is the least significant bit:

$$J_0 = 1$$

$$J_1 = Q_0$$

$$J_2 = Q_1 \cdot Q_0$$

In each case $J_n = K_n$.

(9 marks)

(iii) Correctly drawn circuit diagrams at four marks each.

(8 marks)

A comparison can be based on the relative simplicity of the D-type F-F which results in a larger number of additional gates to make the circuit. To some extent this may be mitigated by the smaller silicon area required for each such F-F. (2 marks)

Examiner's Comments

Candidates seemed well versed in the solution of this type of problem and any errors arose from carelessness rather than lack of knowledge.

Question 3

3. As the current technologies for the construction of computer hardware are pushed ever harder, it is becoming apparent that the physical laws will omit future developments. Identify these limitations and discuss ONE of the novel approaches to computer design that have been advanced to find a way forward. (20 marks)

Answer Pointers

The discussion of the limitations imposed by the known physical laws should address most of the topics listed below:

- velocity of light as the ultimate signal speed;
- storage of one bit per electron;
- heat dissipation – faster circuits, more heat;
- miniaturization – ability to draw finer detail;
- quantum tunnelling.

(10 marks)

An outline discussion of the principles of operation of one novel computer architecture should be given together with a discussion of how it might mitigate some of the physical limitations discussed in the earlier part of the question. (15 marks)

Examiner's Comments

There were too few answers to this question to make a meaningful comment.

Question 4

4. a) In respect of computer disks, explain the terms:
- i) Sector
 - ii) Track
 - iii) Cylinder
 - iv) Rotational latency (8 marks)
- b) A disk consists of 7 data surfaces, 9926 cylinders and 1152 sectors per track. If a sector is 512 bytes, calculate the capacity of the disk. (4 marks)
- c) If the disk spins at 10000 rpm, the time taken for the heads to move from cylinder 0 to cylinder 9925 is 115 ms and the time for the heads to move between adjacent cylinders is 8ms, estimate the mean latency of the disk. State clearly any assumptions in your calculation. (6 marks)
- d) What is disk fragmentation? Explain the benefits of carrying out defragmentation on your hard drive. (7 marks)

Answer Pointers

- a) (2 marks for each, with a little more emphasis on (iv))
- b) Full marks for a correct calculation which should result with an answer of just under 41GB.
- c) Latency consists of 2 components: rotational & seek time [1 mark]
Rotational latency is half the rotation time, i.e. 3mS [1 mark]
Mean seek time is the time to traverse 1/3 disc [1 mark]
Calculation: seek time = $t \times Y + Z$.
 $Z = 8\text{ms}$ (start/stop time)
 $Y = (115 - Z)/9925 = 0.01078 \text{ mS}$
Hence the seek time will be $3308 \times Y + Z = 35.66 + 8 = 43.7 \text{ mS}$ [3 mks]
Credit will be awarded for any sensible attempt.
- d) For full marks, the candidate should describe:
- 1. File fragmentation [2 marks]
 - 2. Directory fragmentation [1 mark]
 - 3. Free Space fragmentation [1 mark]
- Benefits of defragmentation:
- 1. Faster file access due to reduced head movement [2 marks]
 - 2. Lower mechanical wear of the disc mechanism. [1 mark]

Question 5

5. a) What is the OSI 7-layer model? Give a brief description of the services provided by each layer of the model. (9 marks)
- b) What is meant by *Carrier Sense Multiple Access with Collision Detect (CSMA-CD)*? Using a real protocol, such as Ethernet (IEEE 803.2), explain how such a system works. (12 marks)
- c) In a CSMA-CD system, with a carrier clock frequency of 10MHz and more than 10 stations trying to use the network at the same time, what maximum effective data transfer rate would you expect? Give your reasons. (4 marks)

Answer Pointers

- a) Up to 2 marks for an explanation of what it is for. One mark for the description of each layer. Little credit will be awarded for bald headings and gobbledegook.
- b) Full credit will be given for a description along the lines of:
1. A station intending to transmit will firstly listen to the medium. If it is quiet it will transmit. [2 marks]
 2. At the end of then transmission, it listens again to determine if anyone else has attempted to transmit. If so a "collision" has been detected. [3 marks]
 3. Upon detection of a collision, the MAC will emit a "jam sequence" so that stations on the network will detect the collision. Stations wishing to transmit will wait for a random period calculated from its MAC address so as to prevent knock on collisions. [5 marks]
 4. If a further immediate collision is detected, the stand off time is increased. The MAC will limit the number of retries to a predetermined limit. [2 marks]
- c) As the network gets busier the likelihood of collisions increases. Each collision followed by the compulsory stand off results in the wastage of a lot of network time. In the limit, the effective usable network bandwidth is reduced to about 23% of the speed of the carrier medium. Hence the answer to the question is about 2.5Mbits/s

Question 6

6. a) Explain what is mean by *stack machine*. (4 marks)
- b) What are the stages in the execution of a computer instruction? (4 marks)
- c) The central processor unit (CPU) shown in **Figure 1**, at the end of this page, is a 16 bit microprocessor with 16-bit registers and is designed to be programmed as a "stack machine". The registers which the programmer can access directly are implemented in RAM.

Address	Description	Abbreviation
0..1	Register 0	R0
2..3	Register 1	R1
4..5	Index Register	Rx
6..7	Reserved	
8..9	Stack Pointer	SP
10..11	Frame Pointer	FP
12..15	Reserved	

If the CPU hardware clock rate is 500MHz and the memory clock rate is 333MHz, estimate the execution time for a simple ADD instruction which sums the contents of the two locations at the top of the stack and leaves the result on the top of the stack. The stack is held in RAM. State clearly any assumptions in your calculations. (10 marks)

- d) In order to improve the performance of the processor, the designers have decided to put 8kB of 2GHz cache between the CPU and the RAM. The cache is designed so that 90% of all memory accesses by the CPU can be satisfied immediately by the cache. Estimate the revised instruction execution time for the simple ADD instruction described in c) above, with the cache enabled. (7 marks)

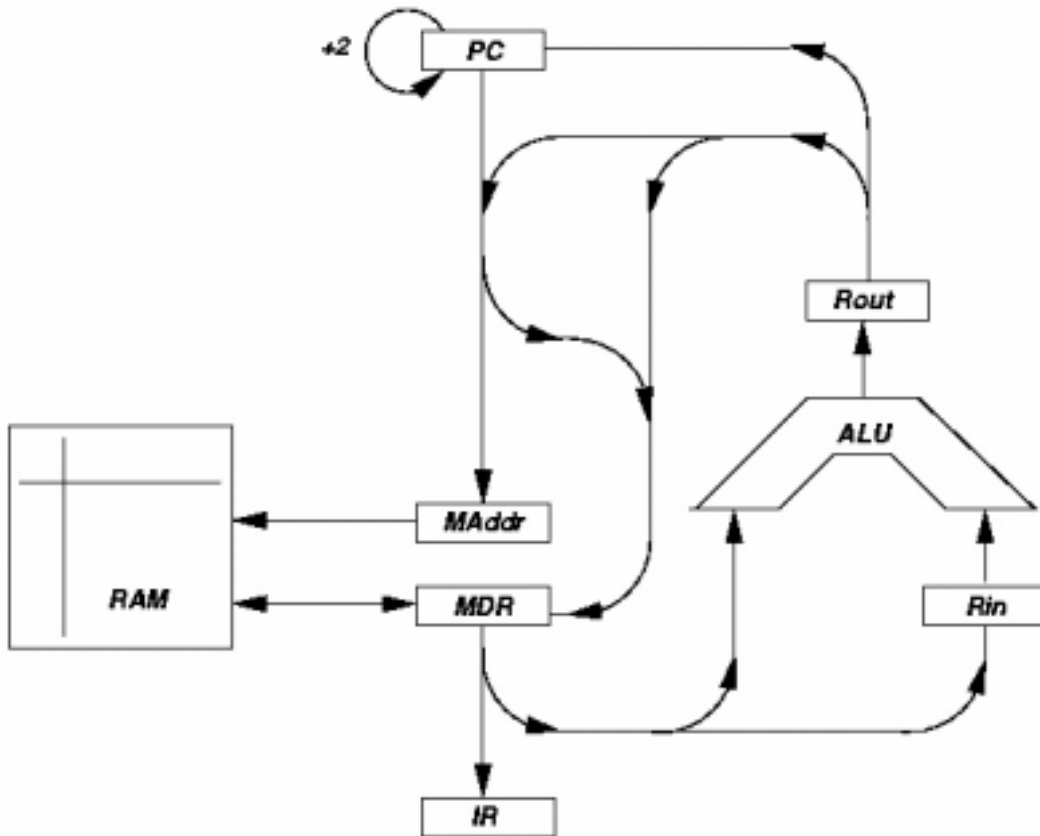


Figure 1

Answer Pointers

a) A stack machine is a processor where, from the programmers' viewpoint, instruction operands are held on the top of a push-down stack as opposed to named registers.

b) One mark each for a description which amounts to:

1. Instruction fetch
2. Instruction decode
3. Operand(s) fetch (if necessary)
4. Instruction execute

[1 mark each]

c) Hopefully the candidate will come up with something like:

- | | |
|-------------------------------------|-------|
| 1. Fetch instruction @PC | 1 MEM |
| 2. Instruction decode; Increment PC | 1 CPU |
| 3. Pop 1st opd from @SP-- to Rin | 1 MEM |
| 4. Pop 2nd opd from @SP-- to ALU | 1 MEM |
| 5. Perform Add to Rout | 1 CPU |
| 6. Push Rout to @++SP | 1 MEM |

This results in 4 x Memory cycles + 2 CPU cycles

Thus the timings are $4 \times 3 + 2 \times 2 = 16 \text{ nS}$

1 mark for each step enumerated above

2 marks for the calculation

2 marks for the general concept.

d) Firstly, the candidate should calculate a revised effective memory access time: $(0.9 \times 0.5) + (0.1 \times 3) \text{ nS} = 0.75 \text{ nS}$ [4 marks]

The new execution time will be $4 \times 0.75 + 2 \times 2 = 7 \text{ nS}$ [3 marks]