

**THE BRITISH COMPUTER SOCIETY**  
**THE BCS PROFESSIONAL EXAMINATION**  
**Diploma**

**ARCHITECTURE**

29<sup>th</sup> April 2005, 10.00 a.m.-12.00 p.m.  
Answer FOUR questions out of SIX. All questions carry equal marks.  
Time: TWO hours.

*The marks given in brackets are **indicative** of the weight given to each part of the question.*

1. For the function:

$$f = A'B'D' + A'BD + BC'D + BCD + AB'C + AB'C'D'$$

- a) Construct a Karnaugh map and use it to find a minimum sum of products expression for f. **(4 marks)**
- b) Draw a logic circuit for the minimised expression using only AND, OR and NOT gates. **(4 marks)**
- c) Manipulate the expression into a suitable form and hence draw a logic circuit using only NAND gates. **(5 marks)**
- d) Manipulate the expression into a suitable form and hence draw a logic circuit using only NOR gates. **(5 marks)**
- e) Compare the relative merits of the logic circuit solutions to parts c) and d). **(3 marks)**
- f) Discuss the relative merits of TWO hardware implementation strategies for the above circuits that are not based on discrete gates. **(4 marks)**

2. The count sequence for a modulo 8 synchronous counter is shown in the table below:

| State | Q2 | Q1 | Q0 |
|-------|----|----|----|
| 0     | 0  | 0  | 0  |
| 1     | 0  | 0  | 1  |
| 2     | 0  | 1  | 0  |
| 3     | 0  | 1  | 1  |
| 4     | 1  | 0  | 0  |
| 5     | 1  | 0  | 1  |
| 6     | 1  | 1  | 0  |
| 7     | 1  | 1  | 1  |

- i) By means of Karnaugh maps derive the minimised sums of products expressions for each stage of the counter if it is to be built from D-type flipflops.
- ii) By means of Karnaugh maps derive the minimised sums of products expressions for each stage of the counter if it is to be built from JK flipflops.
- iii) Draw the logic circuit for each counter design using the appropriate flipflops and AND, OR and NOT gates. Compare the two designs. **(20 marks)**

**Turn over]**

3. As the current technologies for the construction of computer hardware are pushed ever harder, it is becoming apparent that the physical laws will omit future developments. Identify these limitations and discuss ONE of the novel approaches to computer design that have been advanced to find a way forward. **(20 marks)**
4. a) In respect of computer disks, explain the terms:  
i) Sector  
ii) Track  
iii) Cylinder  
iv) Rotational latency **(8 marks)**
- b) A disk consists of 7 data surfaces, 9926 cylinders and 1152 sectors per track. If a sector is 512 bytes, calculate the capacity of the disk. **(4 marks)**
- c) If the disk spins at 10000 rpm, the time taken for the heads to move from cylinder 0 to cylinder 9925 is 115 ms and the time for the heads to move between adjacent cylinders is 8ms, estimate the mean latency of the disk. State clearly any assumptions in your calculation. **(6 marks)**
- d) What is disk fragmentation? Explain the benefits of carrying out defragmentation on your hard drive. **(7 marks)**
5. a) What is the OSI 7-layer model? Give a brief description of the services provided by each layer of the model. **(9 marks)**
- b) What is meant by *Carrier Sense Multiple Access with Collision Detect (CSMA-CD)*? Using a real protocol, such as Ethernet (IEEE 803.2), explain how such a system works. **(12 marks)**
- c) In a CSMA-CD system, with a carrier clock frequency of 10MHz and more than 10 stations trying to use the network at the same time, what maximum effective data transfer rate would you expect? Give your reasons. **(4 marks)**

6. a) Explain what is mean by *stack machine*. (4 marks)
- b) What are the stages in the execution of a computer instruction? (4 marks)
- c) The central processor unit (CPU) shown in **Figure 1**, at the end of this page, is a 16 bit microprocessor with 16-bit registers and is designed to be programmed as a "stack machine". The registers which the programmer can access directly are implemented in RAM.

| Address | Description    | Abbreviation |
|---------|----------------|--------------|
| 0..1    | Register 0     | R0           |
| 2..3    | Register 1     | R1           |
| 4..5    | Index Register | Rx           |
| 6..7    | Reserved       |              |
| 8..9    | Stack Pointer  | SP           |
| 10..11  | Frame Pointer  | FP           |
| 12..15  | Reserved       |              |

If the CPU hardware clock rate is 500MHz and the memory clock rate is 333MHz, estimate the execution time for a simple ADD instruction which sums the contents of the two locations at the top of the stack and leaves the result on the top of the stack. The stack is held in RAM. State clearly any assumptions in your calculations. (10 marks)

- d) In order to improve the performance of the processor, the designers have decided to put 8kB of 2GHz cache between the CPU and the RAM. The cache is designed so that 90% of all memory accesses by the CPU can be satisfied immediately by the cache. Estimate the revised instruction execution time for the simple ADD instruction described in c) above, with the cache enabled. (7 marks)

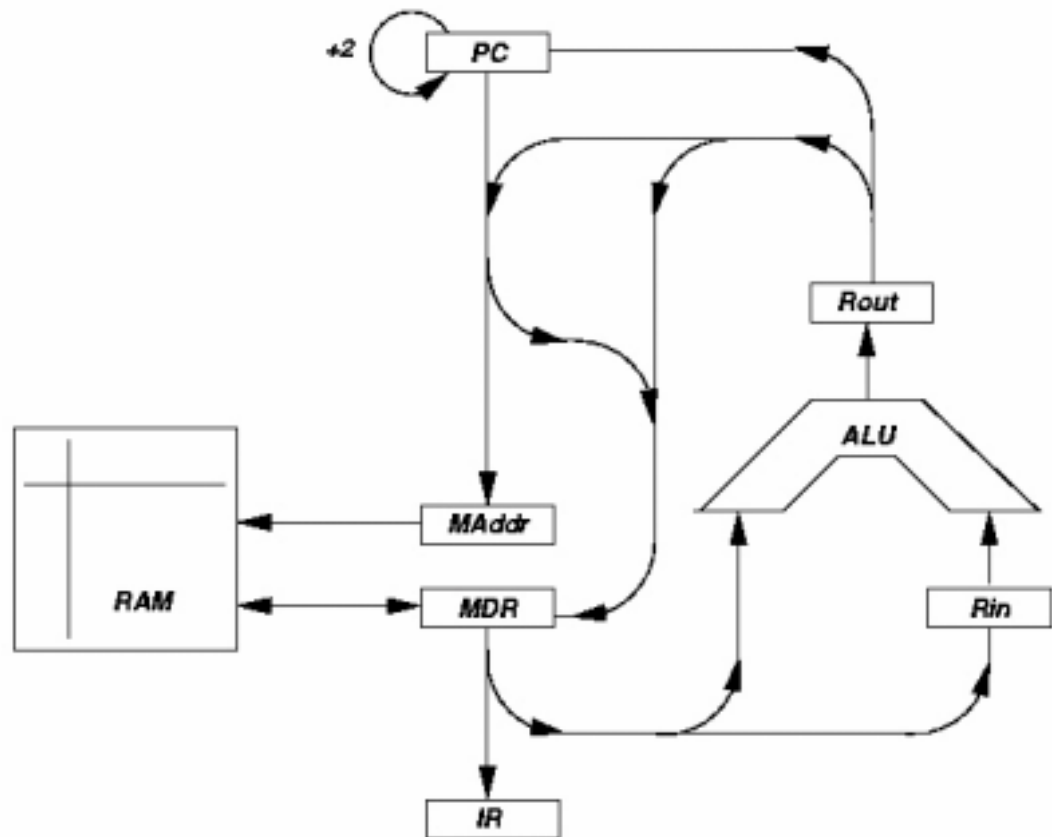


Figure 1