THE BRITISH COMPUTER SOCIETY

THE BCS PROFESSIONAL EXAMINATION
Diploma

ARCHITECTURE

29th April 2004, 2.30 p.m.-4.30 p.m.
Answer FOUR questions out of SIX. All questions carry equal marks.
Time: TWO hours.

*The marks given in brackets are **indicative** of the weight given to each part of the question.*

1. For the function

f = AB'C'D' + ACD' + ABC'D' + ABCD + A'BCD +A'B'CD

a) Construct a Karnaugh map and use it to find a minimum sum of products expression for f. **(4 marks)**

b) Draw a logic circuit for the minimised expression using only AND, OR and NOT gates. (**4 marks)**

c) Manipulate the expression into a suitable form and hence draw a logic circuit using only NOR gates. **(5 marks)**

d) Assuming the the minterms ABC'D and AB'CD represent conditions that can never arise, determine a simpler expression for the minimum sum of products expression for f. **(4 marks)**

e) Manipulate the new expression of part *d)* into a suitable form and hence draw a logic circuit using only NOR gates. **(5 marks)**

f) Compare the relative merits of the logic circuit solutions to parts *c)* and *e).* **(3 marks)**

2. *a)* Discuss the statement that "computer components do not last for ever". **(6 marks)**

b) Consider a computer built from the components shown in **Table 2** below. Calculate its reliability over 750 hours stating any assumptions on which your answer is based and showing your working. **(10 marks)**

Component Type	**Number in System**	**Failure Rate (% per 1000 hours)**
integrated circuits	10	0.0019
Capacitors	27	0.021
resistors	23	0.008
wire wraps	748	0.00001

Table 2

c) Compare the relative merits of different approaches that can be adopted to increase the *reliability* of a computer system. **(9 marks)**

3. *a)* The count sequence for a modulo 5 synchronous counter is shown in **Table 1** below:

State	Q2	Q1	Q0
0	0	1	1
1	1	0	0
2	1	0	1
3	1	1	0
4	1	1	1

Table 1

i) Give a transition table for the counter.

ii) By means of Karnaugh maps, derive the minimised sum of products expressions for each stage of the counter given that it is to be built from JK flipflops. You may assume the unused states will never be entered.

iii) Draw the logic circuit for the counter based on JK flip flops and AND, OR, and NOT gates.

(20 marks)

b) The counter of part *a)* has three unused states. Discuss the possible consequences of simply ignoring these states as you are instructed to do in the question. **(5 marks)**

4. *a)* In respect of computer disks, explain the terms:

i) Sector
ii) Track
iii) Cylinder
iv) Cluster
v) Partition
vi) Partition Table
vii) Extended Partition **(11 marks)**

b) A disk consists of 16838 cylinders, 5 data surfaces and 696 sectors per track. If a sector is 512 bytes, calculate the capacity of the disk. **(5 marks)**

c) Describe how a primary partition is defined in a partition table. Explain what problems arose when disk sizes exceeded 8GB. (**9 marks)**

5. *a)* What is the OSI 7-layer model? Give a brief description of the services provided by each layer of the model. **(12 marks)**

b) With reference to the Data Link Layer, explain what is meant by a frame? What information would you expect to find in a data frame? Use a real protocol, such as HDLC, to illustrate your answer. **(8 marks)**

c) What is meant by *flow control*? Explain how this concept is implemented in the HDLC protocol. **(5 marks)**

6. *a)* Describe the steps in the execution of a computer instruction. **(6 marks)**

b) Figure 1 below shows the register and highway layout of a typical 1980s minicomputer.

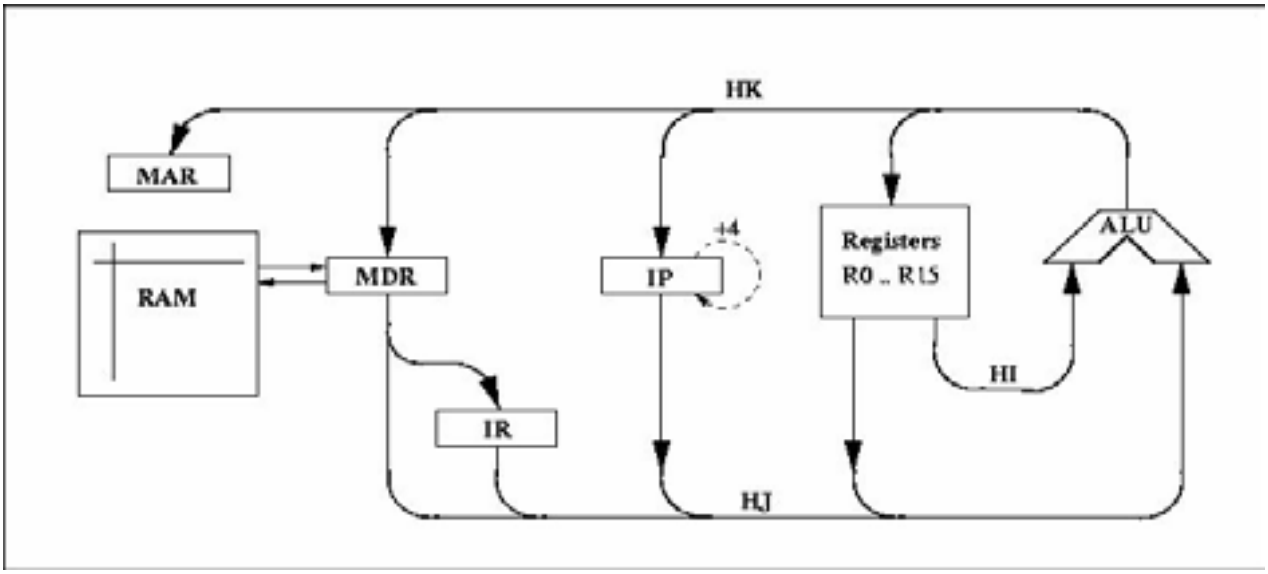
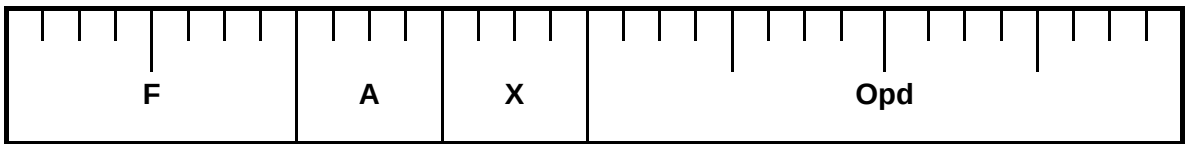


Figure 1

Key:	**RAM**	Main Memory	**IP**	Instruction Pointer
	ALU	Arithmetic & Logic Unit	**IR**	Instruction Decode Reg
	MAR	Memory Address Reg	**HI**	Highway "I"
	MDR	Memory Data Register	**HJ**	Highway "J"
			HK	Highway "K"

The instruction format for this computer is shown below:



Where: F is the opcode
A is the data register (R0..R15)
X is the index register (R1..R15)
Opd is the operand field.

All data instructions are of the form:

<Instr> <Destn Reg>, nnnn[<Index Reg>]

Describe how the bit patterns are moved around this processor during the execution of the instruction:

ADD R4,8[R7]

(Add the contents of the store location, whose address is 8, plus the contents of R7, to the contents of R4)

(14 marks)

c) The cpu data bus is 32 bits wide. If the processor clock speed is 50MHz and the memory cycle time is 33ns, estimate the execution time for the ADD instruction above. **(5 marks)**