THE BCS PROFESSIONAL EXAMINATION
Diploma

April 2003

EXAMINERS' REPORT

Architecture

General

Only 44% of those attempting this examination were successful and the average mark for the module was 35% which is considered to be low.

Question 1

1. For the function:

$$f = \overline{A}\ \overline{C}\ D + \overline{A}\ \overline{B}\ \overline{C} + \overline{A}\ B\ \overline{C}\ \overline{D} + A\ C\ \overline{D} + \overline{B}\ \overline{C}\ D + A\ B\ C\ \overline{D}$$

a) Construct a Karnaugh map and use it to find a minimum sum of products expression for *f*. (4 marks)

b) Draw a logic circuit for the minimised expression using AND, OR and NOT gates. (3 marks)

c) Manipulate the expression into a suitable form and hence draw a logic circuit using only NOR gates. (5 marks)

d) Manipulate the expression into a suitable form and hence draw a logic circuit using only NAND gates. (5 marks)

e) Compare the relative merits of the logic circuit solutions to sections *b, c,* and *d.* (3 marks)

f) Comment on the implications of implementing this function in a full custom VLSI chip. (5 marks)

Answer Pointers

a)

	A'B'	A'B	AB	AB'
C'D'	X	X	0	0
C'D	X	X	0	X
CD	0	0	0	0
CD'	0	0	X	X

Hence the minimum sum of products expression is:

f = A'C' + B'C'D + ACD'

(4 marks)

b) The logic circuit requires 4 NOT gates, 3 AND gates and 1 OR gate. The longest delay path is 3 gates deep (3 marks)

c) Candidates should either use the drop sets or the original minimised expression and de Morgan's law to recast the expression solely in terms of OR operations. Using the drop sets the expression becomes:

$$f = ((A + C')' + (C' + D')' + (A' + B' + C)' + (A' + C + D)')'$$

(5 marks)

d) Candidates should either use the drop sets or the original minimised expression and de Morgan's law to recast the expression solely in terms of AND operations. Using the drop sets the expression becomes:

$$f = ((A'C)' . (CD)' . (ABC')' . (AC'D')')'$$

(5 marks)

e) Comparison should be drawn on the basis of speed (number of gate propagation times) and cost (number of gates and circuit board area). (3 marks)

f) Answers should demonstrate an understanding of the development time, cost and volume considerations of using VLSI. (5 marks)

Examiner's Comments

Most candidates produced a correct Karnaugh map and deduced from it the minimum sum of products expression for the expression f. A few candidates clearly did not understand how to manipulate the expression into suitable forms to enable them to draw the logic circuit using only NOR or only NAND gates. A number of candidates used the conventional symbol for a not gate in their NOR/NAND gate circuits without showing how this could be implemented from NOR or NAND gates. The full implications of creating such a circuit from VLSI in terms of cost and lead time were not generally well understood.

Question 2

2. *a)* Compare the software poll and vectored interrupt approaches for handling requests from device interfaces. Your answer must demonstrate an understanding of the principles of each strategy. (12 marks)

b) Devices such as the hard disk are supported by a strategy called Direct Memory Access. Outline the principles of operation of this technique and compare it with input/output directly programmed in the main system processor. (13 marks)

Answer Pointers

(a) Software Poll. At intervals the processor tests the status of request flags in each device interface. If a flag is found to be set the processor will run the appropriate handling routine to service the request. The order of the poll determines the priority of each device.

Vectored interrupt. A hardwired connection exists between each interface and the main system processor. When a device wants attention it asserts an interrupt request on this line. The processor checks the priority of the currently executing task and if it is lower than that of the requesting device it deals with the interrupt. Interrupting devices may share a common interrupt request line so that the processor now needs to identify the source of the interrupt. It does this by asserting an Acknowledge signal on a second hardware line that is routed through each interface in turn. The first interrupting device to receive this signal intercepts it and responds by placing its

own vector number on the databus. The processor uses this number as the basis of an address which it then uses to access the start of the appropriate service routine.

Comparison. The software poll requires no additional hardware beyond the existence of a status flag in the interface whereas the vectored interrupt requires two additional signal lines and a register in each interface to hold a vector number. Priority is determined by the order of the software poll and can be altered under software control. The order in which the interfaces are visited by the acknowledge signal determines priority in the vectored interrupt. The vectored interrupt is potentially very fast with a delay equivalent to one memory access to get the vector number and a few more cycles to complete the current instruction and change the machine code context. The response time of the software poll depends on the frequency of the poll. The software poll wastes execution cycles checking the status flags even when none are set whereas the vectored interrupt mechanism is only triggered when an interface requires attention.

(b) DMA is used to transfer data between main store and high speed devices such as hard disks. A second processor known as a Direct Memory Access Controller takes control of the system buses from the main system processor for the duration of a DMA operation. A system of handshakes is used to ensure there is no contention for the buses during the DMA operation. The request for transfer from the interface is passed forward by the DMAC to the main processor as a hold request. The main processor disconnects from the buses and acknowledges to the DMAC that it has relinquished control. The DMAC will already have received information about the size, direction and memory addresses for the transfer and now signals to the interface that transfer can start. Once the required number of bytes has been transferred the handshake signals are negated in turn and the main system processor regains control of the system.

Comparison. The key feature of DMA is that the DMAC has internal microcode for the transfer process and does not require an external machine code program. Thus the full bus bandwidth can be devoted to transfer of data.

Examiner's Comments
2 (a) Some candidates answered this question from an operating system perspective but did not get close enough to the distinction between the principles of the two interrupt strategies.

2 (b) There was a good level of understanding about the principles of operation of the Direct Memory Access strategy although some candidates were either unaware of the difference between burst and cycle steal or confused about the distinction. In a few cases DMA was cited as a strategy only for handling slow peripheral devices.

Question 3

3. *a)* Briefly describe the technological limitations which are likely to limit the future development of conventional stored program, digital computers. (7 marks)

b) Outline the principles of operation of:
- *i)* the neural network computer
- *ii)* the quantum computer

In EACH case, highlight the advantages of each of these designs over the conventional, stored program, digital computer. (18 marks)

Answer Pointers
a) Answers should address most of:
- Propagation delays bounded by the velocity of light

- Miniaturisation limited by the ability to draw ever finer structures, quantum mechanical tunnelling between adjacent conductors and the need to remove waste heat
- Reduction of electrons used to store a bit reaching one. (7 marks)

b) There is significant variation in the design approaches for these architectures particularly in the case of the quantum computer but each answer will be marked on its own merits.

(18 Marks)

Examiner's Comments
Very few candidates attempted this question. A few offered good understanding but the majority were more inventive than factual.

Question 4

4. Figure 1 below shows the instruction format of a typical 1980s mini-computer. This mini-computer implements standard 2s complement integer instructions with 16 bit operands and sixteen 16 bit registers. The instruction field definitions are:

The *Function* field (6 bits) determines the format of the rest of the instruction format and the behaviour of the processor as the instruction is executed. The format shown is that for normal arithmetic operations.

The *Rx* field (4 bits) denotes one of 16 general purpose register which contains the first operand and is also the destination register of the result.

The *Ry* field (4 bits) denotes one of 16 general purpose registers which is used in the calculation of the second operand.

The *Mode* field (2 bits) denotes one of 4 address modes for the second operand:

00 direct: the second operand is the contents of the register *Ry*;
01 indirect: the second operand is the contents of the memory location the address of which is held in the register *Ry*;
10 indexed: the second operand is the contents of the memory location the address of which is calculated by summing the *extension field* and the contents of the register *Ry*;
11 immediate: the second operand is the value calculated by summing the *extension field* and the contents of the register *Ry.*

The *Extension* field (16 bits) is a 16 bit 2s complement integer used to calculate the second operand with address modes 2 and 3 (see above).

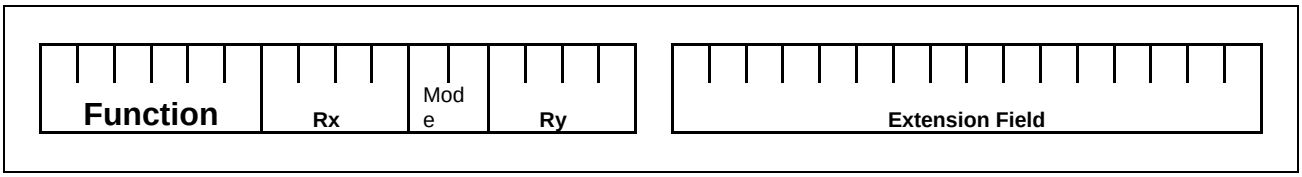

Figure 1 The Computer Instruction Format

a) The cpu data bus is 16 bits wide. If the processor clock speed is 25MHz and the memory cycle time is 66ns, calculate the execution times for each of the four address modes. State clearly, in your answer, any assumptions you have made in your calculations. (11 marks)

b) Explain how a main memory cache would improve the performance of such a processor. (6 marks)

c) If the processor is equipped with a 64kB 5ns cache and the mean cache hit rate is 90%, calculate the revised execution times for the four address modes. (8 marks)

Answer Pointers
(CPU instruction timings) – average mark 25%

a) The cpu data bus is 16 bits wide. If the processor clock speed is 25MHz and the memory cycle time is 66nS, calculate the execution times for each of the four address modes. State clearly, in your answer, any assumptions you have made in your calculations.

(11 marks - 3 marks for identifying the phases of execution; 4 marks for demonstrating understanding that timings will be mode dependent; 1 mark for the time calculation for each mode).

Assumption: Mode 0 ~ Instr Fetch 1 mem cycle, Instr decode 1 cpu cycle, Instr execute 1 cpu cycle;
Mode 1 - as for Mode 0 plus Operand fetch 1 mem cycle;
Mode 2 - Instr fetch 2 mem cycles, Instr decode 1 cpu cycle, operand fetch 1 mem cycle, Instr execute 1 cpu cycle;
Mode 3 - Instr fetch 2 mem cycles, instr decode 1 cpu cycle, instr execute 1 cpu cycle.)
Mode 0: 1 mem + 2 cpu = 66 + 40x2 = I46ns
Mode 1: 2 mem + 2 cpu = 132 + 40x2 = 2I2ns
Mode 2: 3 mem + 2 cpu = 198 + 40 x 2 = 278 ns Mode 3: 2 mem + 2 cpu = 132 + 40x2 = 2I2ns

b) The cache acts as a high speed scratch pad between the main memory and the cpu. When the cpu requests data from the memory via the cache, the cache checks to see if it holds a local copy of the requested data. If the answer is 'yes', then the cache can supply the data without bothering the main memory thus saving time (2 marks)

If the cache fails to find a local copy, it forwards the request to the main memory. When the data is supplied, the cache retains a copy for future use (1 mark)

In retaining the copy of the data, it has to keep both the data itself and the address whence it came. In order to find room for this information, it will have to find an entry which is unlikely to be required in the immediate future - the entry replacement algorithm. (2 marks)

The larger the cache, the greater the likelihood that the required data is to be found in the cache. (1 mark)

When the cpu writes back to the memory, the cache also takes a copy of the data passed through to the main memory (write through cache) (1 mark)

c) If the processor is equipped with a 64kB 5nS cache and the mean cache hit rate is 90%, calculate the revised execution times for the four address modes. (8 marks - 1 mark for each mode **plus** 4 for the effective memory access time calculation) Effective memory access time now (9 x 5 + 1 x 66) 7 10 = II.Ins
Mode 0: 1 mem + 2 cpu = 11.1 + 80 = 9Ins
Mode 1: 2 mem + 2 cpu = 22.2 + 80 = I02ns
Mode 2: 3 mem + 2 cpu = 33.3 + 80 = II3ns
Mode 3: 2 mem + 2 cpu = 22.2 + 80 = I02ns.

Examiner's Comments
Many candidates forgot to include the instruction fetch; in fact very few included a bare instruction cycle definition.

- Only a few had any idea how a cache worked and/or came up with an effective store access time.
- On the other hand, most seemed to know about address modes.

Question 5

5. *a)* In respect of the computer disks, explain the terms:
i) Sector
ii) Track
iii) Cylinder
iv) Partition
v) Directory (7 marks)

b) A disk consists of 11545 cylinders, 5 data surfaces and 498 sectors per track. If a sector is 512 bytes, calculate the capacity of the disk. (5 marks)

c) Describe, with the aid of diagrams, how a file is spatially distributed in a FAT file system. (13 marks)

Answer Pointers
a) i) A sector is the smallest addressable unit of starge on a disk drive, usually 512 bytes. (1 mark)

ii) A track consists of the ring of sectors on one surface of a cylinder. (1 mark)

iii) A track consists of the ring of sectors on one surface of a cylinder. (1 mark)

iv) A partition is a data structure on a disk which supports a file system. A disk may contain one or more partitions. (2 marks)

v) A Directory is a special file which holds a vector of file entries. Each file entry will consist of the file name plus a pointer to a data structure which holds all the necessary system information about the file. (2 marks)

b) Each track contains 498 x 512 bytes = 254,976 bytes Each cylinder then contains 254,976 x 5 = 1,274,880 bytes Hence the disk contains 1,274,880 x 11,545 = 14,718,489,600 bytes (i.e. 14.7GB) (5 marks)

c) Up to 5 marks can be gained by a diagram showing a directory entry, the appropriate FAT chain and pointers to the file data blocks ("clusters" in MS speak).
There should be a description of the information held in the file directory entry – which must include the reference to the first data block. (3 marks)
The FAT table should be described. The description should include that "pointers" have a double use: they point to the actual data blocks and the next FAT entry within the table (2 marks)
The remaining three marks are allocated for other useful items of info such as the value denoting the end of chain, bad blocks etc. Additional credit can be gained by an expla- nation of how the block size ("cluster" size) is determined. (3 marks)

Examiner's Comments
(Disks and file systems) – average mark 37%
Most candidates could calculate the capacity of the disk drive - not many seemed to have calculators.

- Many had a hazy idea what sectors and tracks were; most seemed to know what a cylinder was.
- Very few seemed to know that a directory was a file.
- Only 3 candidates made a serious attempt to describe how a file was laid out in a FAT file system.

Question 6

6. *a)* What is the OSI 7-Layer model? Give a brief description of the services provided by each layer of the model. (10 marks)

b) Describe the format of an HDLC data frame. Explain the function of each field. (9 marks)

c) What is meant by *flow control?* Explain how this concept is implemented in the HDLC protocol. (6 marks)

Answer Pointers
a) (10 marks) in total
Three marks can be earned by explaining that the model is a template for the architecture of a communications system and acts as a functional check list. It does not prescribe how the communication system is to be implemented but it does specify how the various protocol components relate to each other. A bonus mark can be gained for a good clear diagram.
One mark for a sensible description of the services offered by each layer.

b) (9 marks) in total

Flag octet: denotes limits of the frame (1 mark)
Address octet: Ox80 for DTE to DCE, OxcO for DCE to DTE (bonus mark!)
Command Octet: [0 <N(S) 3 bits> P <N(R) 3 bits>] where the N(S) bits denote the current frame sequence number (3 marks);
the N(R) bits denote the last frame acknowledged by the far end (3 marks).
Data Field: up to 1024 bits (1 mark)
FCS (2 octets): (1 mark)
Flag octet: frame terminator

c) (6 marks) in total
Flow control is a mechanism which allows the data recipient to force the data source to hold off transmitting to prevent the recipient from being overloaded (2 marks). There are two HDLC flow control mechanisms:

the use of a supervisory frame (RNR) sent by the recipient to the sender to request the sender to desist and the use of an RR frame to request resumption. (2 marks).

the recipient can refuse to acknowledge frames from the sender who will have to desist from sending when its "credit" runs out. The recipient allows resumption of data transmission by acknowledging more recent data frames. (2 marks)

Examiner's Comments
(OSI 7-layer model) - average mark 34%. This was disappointing as the question is straight forward bookwork.

- Very few candidates mentioned that the model was a template.
- Most seemed to overlook the fact that the prime purpose of a communications system is to move data from the sender to the receiver, particularly at the Transport level and the Data Link level.
- Many confused HDLC with Ethernet
- Many could describe what flow control was all about; very few could describe how it might be implemented.