THE BCS PROFESSIONAL EXAMINATION
Diploma

April 2002

EXAMINERS' REPORT

Architecture

Most candidates seem to be better prepared for the 2002 Architecture Diploma paper than for previous years. There is a very noticeable exception to this with those candidates from Examination Centre 23 (Mauritius). This is illustrated by the effect that their marks have on the average marks for each question.

Question 3 was attempted by everyone (29) candidates: the average mark for this question is 10.8/25. If we ignore the marks from Examination Venue 23, the average is 12.5/25. Question 5 was attempted by every candidate bar one (28); the average mark is 8.8/25. Ignoring EC23 the average rises to 10.9/25. Question 6 was only attempted by just less than half of the candidates (13); the average mark is 8.1/25. Ignoring EC23 the average rises to 13.1/25.

Question 1

1. *a)* For the function:

$$f = \bar{A}\bar{C}\bar{D} + \bar{B}\bar{C}D + \bar{A}BD + A\bar{C}\bar{D} + B\bar{C}\bar{D} + ABCD$$

i) **Construct a Karnaugh map and use it to find a minimum sum of products expression for f.**

ii) **Draw a logic circuit for the minimised sum of products expression for f using AND, OR and NOT gates.** **(10 marks)**

b) **Design a synchronous, modulo eight, binary counter based on JK flip-flops. Your answer must give a state table for the count sequence and Karnaugh maps for each of the J and K inputs to the counter flip-flops.**

(15 marks)

Question 1

Answer Pointer

Part (a) was attempted by most candidates but a common error in simplification was to fail to recognise that map entries could be grouped across the top and bottom boundaries of the Karnaugh map. In some cases the Karnaugh map was drawn correctly but not used to simplify the expression. Simplification was then attempted, usually unsuccessfully, by manipulating the minterms.

Part (b) answers fell into one of two categories. Candidates either understood how to devise a solution and carried it through correctly or did not appear to know where to begin and made no sensible attempt.

Question 2

2. *a)* Explain the principle of operation of the cathode ray tube in the context of screen display for a computer monitor. (7 marks)

***b)* Contrast the relative merits of the cathode ray tube and the liquid crystal display as technologies for the screen of computer monitors. (5 marks)**

***c)* Discuss the specifications you would need to consider in selecting a monitor for a general purpose computer system. Illustrate your answer with numerical values where possible. (8 marks)**

***d)* Contrast the relative merits of a domestic television and a computer monitor as the main display device for computer systems. (5 marks)**

Question 2

Answer Pointers

Use of English is explaining the relevant concepts were a problem for some candidates. Explanations of the principles of operation of the cathode ray tube were somewhat muddled in some cases but generally the question was satisfactorily.

Question 3

3 *a)* What is the OSI layer model? Give a brief description of the services provided by each layer of the model. 10 marks)

***b)* Explain what is meant by a *packet*. What information would you expect to find in a packet header? Explain the purpose of each item of information. (10 marks)**

***c)* Describe the essential differences between a Local Area Network (LAN) and a Wide Area Network (WAN). (5 marks)**

Question 3: (OSI 7-layer model)

Answer Pointers

This question was generally answered better this year than in previous years. There were a number of candidates who thought that *frames* were the same as *packets.* Relatively few candidates knew about the administrative information carried in packet headers – I can only conclude that that most candidates had less than hazy idea as to the mechanics of networking**.**

Question 4

4. *a)* Discuss how the failure rates of components vary with time and in this context explain the significance of the term "burn in".

(5 marks)

b) **Given the table of component data below, calculate the reliability over 1000 hours of a computer built from these components. State any assumptions on which your answer is based and show your working.**

component type	number in system	failure rate (% per 1000 hrs)
integrated circuits	6	0.0027
capacitors	15	0.018
resistors	12	0.009
soldered joints	695	0.0001

(7 marks)

c) **In many contemporary computer systems a fan is used to cool the CPU components. Calculate the revised reliability of the computer system of part *b)* if a fan of failure rate 1.5% per 1000 hours is included in its component list.**

(4 marks)

d) **Briefly discuss the relative merits of the different strategies that can be used to achieve higher levels of reliability for computer hardware.**

(9 marks)

Question 4

Answer Pointers

Very few candidates attempted to answer this question.

Question 5

5. *a)* In respect of computer disks, explain the terms:

i) **Sector**
ii) **Cylinder**
iii) **Track**
iv) **Seek time**
v) **Rotational latency**

(10 marks)

b) **A disk consists of 11545 cylinders, 5 data surfaces and 498 sectors per track. If a sector is 512 bytes, calculate the capacity of the disk.**

(5 marks)

c) **If the disk rotates at 7200 rpm, the time taken for the heads to move from cylinder 0 to cylinder 11544 is 130ms and the time taken for the heads to move between adjacent cylinders is 10ms, estimate the mean latency for this disk. State clearly any assumptions you have made in your calculation.**

(5 marks)

d) **Describe the best way to lay out and maintain files on a disk to minimise the time to access and read the data in the files.**

(5 marks)

Question 5 (Disc Geometry)

Answer Pointers

Most candidates (other than those from EC23) answered most of this question reasonably well.
Most candidates knew who to calculate the capacity of a hard disc – a minority could not be bothered to do the arithmetic.
Very few candidates attempted to estimate the mean latency of the disc. Most of those that tried had got the right idea.
It was obvious from their answers that most candidates had no knowledge of optimal physical layouts of files and directories on a disc. About half made the sensible suggestion that files should be held contiguously, but without knowing why (to allow for long reads/writes from/to disc). Many advocated the use of FAT and frequent use of *DEFRAG*. It is obvious that almost none of the candidates had been exposed to/taught about file systems other than basic FAT systems. There was no evidence of any knowledge of NTFS, Unix file systems, B tree organisation or journaling file systems.

Question 6

6. ***a)*** **Figure 1 below is a simplified diagram of a RISC CPU. The heavy lines represent data highways; the arrows indicate the direction of the flow of data. *Hi*, *Hj* and *Hk* are the main highways. The ALU is the Arithmetic and Logic Unit. The shaded rectangles represent registers:**

PC	**Program Counter (holds the address of the next instruction)**
nPC	**Auxiliary Program Counter (holds the address of the current instruction)**
MAddr	**Memory Address Register**
MDR	**Memory Data Register**
IR	**Instruction Register**
PSR	**Program Status Register**
Register File	**An array of 32 x 32bit general purpose registers**

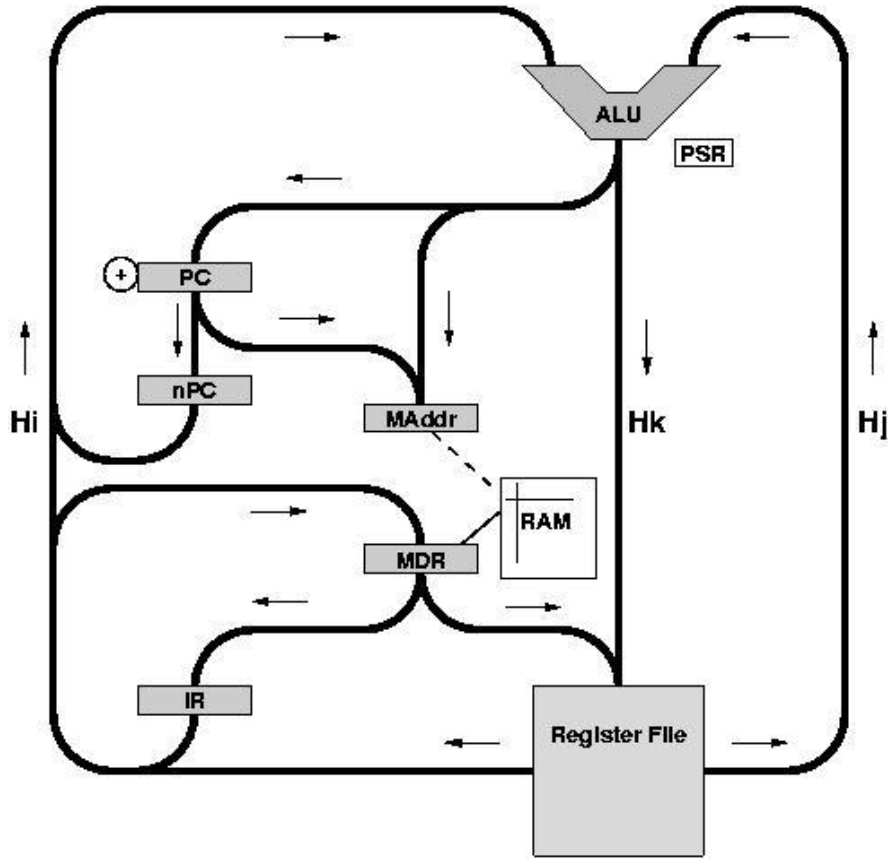

Figure 1

Using this diagram, describe the stages of execution of a simple computer instruction, e.g. ADD r5, r6, r7 (add the contents of r5 to the contents of r6 placing the result into r7).

(10 marks)

b) **If the CPU cycle time is 2ns and the memory cycle time is 10ns, estimate the time of the ADD instruction described in *a)* above.**

(5 marks)

c) **Describe the two ways in which a designer may improve the performance of this CPU without changing the CPU cycle time.**

(10 marks)

Question 6 (The instruction Execution Cycle)

Answer Pointers

It was obvious, from the way that the way this question was attempted, that few candidates had bothered to read the question properly. Just less than half of the candidates seemed to know how the instruction execution cycle worked. Very few, if any, seemed to understand the term *register file.*
About half the candidates made an intelligent estimate of the instruction estimate time.
About half of the candidates put forward sensible ideas for improving the performance of such a CPU: the most popular was *pipelining,* followed by *bus widening* and very few suggested the use of a *cache.*