THE BCS PROFESSIONAL EXAMINATION
Diploma

April 2001

EXAMINERS' REPORT

Architecture

Of the candidates who attempted the examination, only 39% were successful. The examiners were concerned that the performance of candidates this year was much worse than in previous years, whereas the topics identified in the examination questions were similar to those in previous years but with perhaps a different perspective on the detail associated with the question. The examiners' comments associated with each question are as follows:

QUESTION ONE

The controller for a semi-automatic car windscreen wiper system has four inputs. These comprise the state of the car ignition switch, the state of each of two rain sensors and the state of the manual override switch. The wipers will only operate when the car ignition switch is in the ON position and:

EITHER one or both of the rain sensors detects moisture;

OR the manual override switch is in the ON position. In this case the wipers will be activated irrespective of the state of the inputs from the rain sensors.

a) Produce a truth table for the state of the windscreen wipers   (3 marks)

b) Use a Karnaugh map to find a minimised sum of products expression for the state of the windscreen wipers   (4 marks)

c) Draw a logic circuit for the minimised expression using only AND, OR and NOT gates   (5 marks)

d) Manipulate the minimised expression into a suitable form and hence draw a logic circuit using only NAND gates   (5 marks)

e) Briefly discuss the relative merits of implementing the control circuit in a full custom VLSI chip   (4 marks)

f) Assume the manual override switch were a flick switch such that:

1.   moving it briefly to the ON position would start the wipers;

2.   moving it briefly to the ON position a second time would stop the wipers.

**Show how you would modify your circuit to accommodate its action (4 marks)**

Answer Pointers

a) Most candidates gave a correct truth table although a few did not define the alphabetic names they used for the different inputs.

b) Many correct answers, but a failing was not to find the minimum expression as a consequence of grouping into pairs where grouping into fours was possible on the Karnaugh map.

c) Few candidates had any difficulty translating their boolean expression into a logic gate circuit.

d) The question specifically asked for the expression to be manipulated into a suitable form for implementation in NAND gates. In many cases this was not attempted. In a few cases an unnecessarily complex circuit was devisexd by substituting a group of NAND gates for each OR and And gate in the logic circuit of the previous section of the question.

e) This part of the question was not well answered. The economic and development factors surrounding the use of full custom VLSI did not seem to be understood.

f) A few good answers but a significant number of candidates attempted a solution using combinational logic, not recognising the need to store the latest action of the flick switch.

QUESTION TWO

Design a synchronous, up/down counter which follows the count sequence in either direction shown in the state diagram below:

Your solution must show detail of the following design stages:
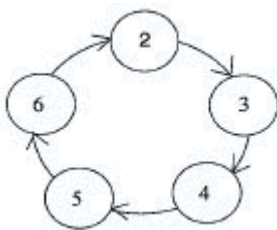
a) A state table showing both the up and down count sequences   (8 marks)

b) Karnaugh maps for each counter stage   (10 marks)

c) A logic circuit for the complete counter based on JK flip-tlops and NOT, AND and OR logic   (7 marks)

The concept of a counter that could count up and down was not widely understood. Some candidates offered only an up counter and others two separate circuits, one each for up and down. A proportion of the marks was awarded for such partial solutions. Candidates did demonstrate a good understanding of the design approach for synchronous counters. In a minority of cases there was uncertainty about the treatment of don't care states.

QUESTION THREE

a) Discuss the assertion that "The drive to produce computers of ever higher performance is pushing the supporting technology towards its limits."

(8 marks)

b) Several alternative architectures have been proposed to overcome the approaching technological limits faced by conventional computer designs. Outline the principles of operation of ONE such architecture and discuss how it may circumvent such limitations. **(17 marks)**

This question was not well answered. The technological limits were not well understood and ideas about alternative architectures were often very incomplete.

QUESTION FOUR
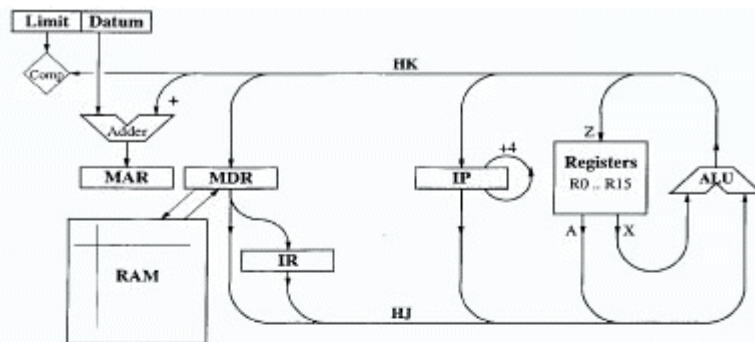
All Data Highways are 32 bits wide

Key:

RAM	Main Memory		**IP**	Instruction Pointer	
ALU	Arithmetic & Logic Unit		**IR**	Instruction Register	
MAR	Memory Address Register		**HJ**	Highway J	
MDR	Memory Data Register		**HK**	Highway K	

The instruction format of this computer is shown below:

Where: **F** is the Opcode
A is the data register (R0 .. R15)
X is the index register (R1 .. R15)
Opd is the Operand field

All date instructions are of the form:

Ra := Ra ⊙ Opd [Rx]

Describe the stages in the execution of the instruction:

Add   R6,4[R7]

a) **A simple computer is shown diagrammatically in the figure above:**

Show how various data items move around the processor during execution
(15 marks)

b) **If the RAM speed is 66MHz and the CPU clock speed is 100MHz, estimate the instruction execution time of the ADD instruction above (4 marks)**

c) **Describe TWO mechanisms commonly used by processor designers to speed up the execution of such an instruction. Estimate by how much you would expect the execution speed to be improved by each of these**
(6 marks)

Whilst more than half of the candidates who attended the examination attempted this question only six candidates achieved the pass mark. It is obvious that the operation of the micro code within a CPU is not well understood by candidates. There is no real understanding of individual timing elements associated with the execution of a relatively simple ADD instruction. Part c) of the question was not at all well understood.

QUESTION FIVE

a) **Explain the terms:**

1. **Sector**
2. **Cluster**
3. **Cylinder**
4. **Partition**
5. **Partition Table**

as applied to hard disk technology (10 marks)

b) **Explain the essential differences between FAT and VFAT file systems. What are the advantages of the VFAT format over the FAT format?**

What file system problems are not solved by VFAT file systems? (10 marks)

c) **Explain why hard disks bigger than 8GB present problems to Personal Computer (PCs) more than three years old. Explain, in simple terms, how modern PCs have overcome this problem (5 marks)**

The responses to this question were extremely disappointing, only one candidate achieved the required pass mark. Section a) was reasonably well answered although few candidates were able to distinguish between partition and partition table with reference to hard disk technology. There was no significant response to parts b and c of the question.

QUESTION SIX

a) What is the OSI 7-layer model. Give a short description of the services provided by each layer of the model **(10 marks)**

b) With reference to the Data Link Layer, explain what is meant by a *frame.*

What information would you expect to find in a data frame?

Use a real protocol, such as HDLC, to illustrate your answer **(10 marks)**

c) Explain what is meant by *bit stuffing* and what it entails. What is its purpose? **(5 marks)**

The candidates who answered this question were able to demonstrate a fairly good understanding of the seven layer model. In some instances the detail associated with the services provided by each layer was minimal.

Part b) was only familiar to four candidates, the idea of a frame and the constituent parts was not at all well understood.

In part c) the concept of bit stuffing and the reason for using this technique was not explained well by any candidate.