SCHOOL OF COMPUTING AND TECHNOLOGY

ELECTRICAL ENGINEERING FIELD

EXAMINATIONS

Programme:	**MSc Computer Systems Engineering**
Module Code:	**EEM111**
Module Title:	**IC Design**
Date:	**Wednesday 30th May 2007**
Time:	**0930-1210**

INSTRUCTIONS TO CANDIDATES:

Answer TWO out of FOUR questions.
All question carry equal marks.

Electronic charge, **q** = 1.6 x 10^{-19} Coulomb, $\boldsymbol{\varepsilon_{Si}}$ = 1.04 x 10^{-12} F/cm permittivity of Si, **kT/q** = $\mathbf{V_T}$ = 0.026V, $\boldsymbol{\varepsilon_{ox}}$ = 3.51 x 10^{-13} F/cm, the permittivity of the SiO_2 gate insulator, $\mathbf{n_i}$ = 1.45 x 10^{10} cm^{-3} (intrinsic carrier concentration)

Q1. The inverter threshold voltage V_{Th} can be defined as $V_{Th} = V_{in} = V_{out}$. In this case both the pMOS and nMOS transistors are in saturation mode and we have:

$$\frac{k_n}{2}\left(V_{GS,n} - V_{T0,n}\right)^2 = \frac{k_p}{2}\left(V_{GS,p} - V_{T0,p}\right)^2$$

where $V_{GS,n} = V_{in}$ and $V_{GS,p} = -(V_{DD} - V_{in})$

and $k_p = \mu_p C_{ox}\left(\frac{W}{L}\right)_{pMOS}$ and $k_n = \mu_n C_{ox}\left(\frac{W}{L}\right)_{nMOS}$

μ_n = electron mobility, μ_p = hole mobility and C_{ox} = gate capacitance
and $V_{GS,n}$ and $V_{GS,p}$ are the gate voltages of the nMOS and pMOS transistors and

a) Show that for a symmetric inverter operation the aspect ratios are given by

$$\left(\frac{W}{L}\right)_{PMOS} = \left(\frac{\mu_n}{\mu_p}\right)\left(\frac{W}{L}\right)_{NMOS} \cong 2.5\left(\frac{W}{L}\right)_{NMOS}$$

and give any other necessary conditions for symmetrical CMOS inverter operation.

(12 marks)

b) The specification below is for a CMOS fabrication process using 1μ technology

L = 1μ	$V_{T,N}$ = 1V
$\mu_n C_{ox}$ = 40μA/V	$V_{T,P}$ = -1V
$\mu_p C_{ox}$ = 16μA/V	V_{DD} = 5V

Apply the technology parameters above in the design of a symmetric operation CMOS inverter by determining the $\mathbf{(W/L)_N}$ and $\mathbf{(W/L)_P}$ ratios for the nMOS and pMOS transistors such that the inverter can meet both the following conditions:

i) the propagation delay must be $\boldsymbol{\tau \leq 1ns}$ for **L = 1μ** and,
ii) the inverter can drive a capacitive load $\mathbf{C_L}$ **= 20pF.**

(13 marks)

Q2. a) Evaluate the two of the technology-scaling methods used namely:

i) constant field scaling and,
ii) constant voltage scaling.

Show using the relevant expressions how the delay time, power dissipation and power density are affected in terms of the scaling factor S, when the design rules change by a factor of 1/S.

(9 marks)

b) Give a brief evaluation of MOSFET scaling effects on the following:

i) short channel effects on the threshold voltage,
ii) sub-threshold conduction for the case $V_{GS} \leq V_{T0.}$

(6 marks)

c) The threshold voltage of a short channel MOSFET transistor is reduced according to the expression:

$$\Delta V_{T0} = \left(\frac{1}{C_{ox}}\right) * \left(\sqrt{2q\varepsilon_{Si}N_A|2\phi_F|}\right) * \left(\frac{x_j}{2L}\right) * \left(\left(\sqrt{\left(1+\frac{2x_{ds}}{x_j}\right)}-1\right)+\left(\sqrt{\left(1+\frac{2x_{dD}}{x_j}\right)}-1\right)\right)$$

Use the above expression and the parameters for an nMOS fabrication process given below to show that the short channel threshold voltage can be expressed as

$$V_{To}(\text{short} - \text{channel}) = 0.855 - \left(\frac{0.19}{L}\right)$$

hence plot the variation of the short-channel threshold voltage V_{T0} against the channel length L for values of L from 0.3μm to 5μm.

(10 marks)

L = channel length in microns (μm),
assume that drain and source voltages are both zero and that

$$x_{dS} = x_{dD} = \left[\frac{2\varepsilon_{Si}\phi_0}{qN_A}\right]^{1/2}$$

The process parameters are:

$N_A = 10^{16}$ cm^{-3} ; the substrate doping
tox = 50 x 10^{-4} m ; the oxide thickness
$x_j = 10^{-6}$m ; depth of source and drain diffusion
ϕ_F = -0.35V ; Fermi Potential
ϕ_0 = +0.76V ; source and drain built in voltage
V_{T0} = 0.855V; long channel threshold voltage

Q3. Accurate estimation of transistor junction capacitance under transient conditions is complicated because the instantaneous values of all junction capacitors will change with the voltages. The problem can however be simplified if the average junction capacitance is determined, given by:

$$C_{eq} = A\ C_{jo}\ K_{eq}$$

where C_{eq} = average junction capacitance
A = cross-sectional area of junction
K_{eq} = voltage equivalence factor
C_{jo} = zero-bias junction capacitance/area

a) Show that the voltage equivalence factor is given by the expression below for the special case of the abrupt junction.

$$K_{eq} = \frac{-2\sqrt{\phi_o}}{(V_2 - V_1)}\left[\sqrt{\phi_o - V_2} - \sqrt{\phi_o - V_1}\right]$$

(11 marks)

b) The process parameters for the nMOS transistor in Figure Q3 are shown as follows:

Substrate doping	$\mathbf{N_A} = 2e10^{15}$ cm^{-3}
Source/drain doping	$\mathbf{N_D} = 10^{20}$ cm^{-3}
Gate Oxide thickness	**tox** = 50nm
Intrinsic carrier concentration	$\mathbf{n_i} = 1.45e10^{10}$ cm^{-3}
Diffusion Overlap	$\mathbf{L_D}$ = 0.5µm

Assuming that the drain voltage is changing from 1V to 5V find the voltage equivalence factor for the bottom drain-substrate junction only and hence the average value of the capacitance.

(14 marks)

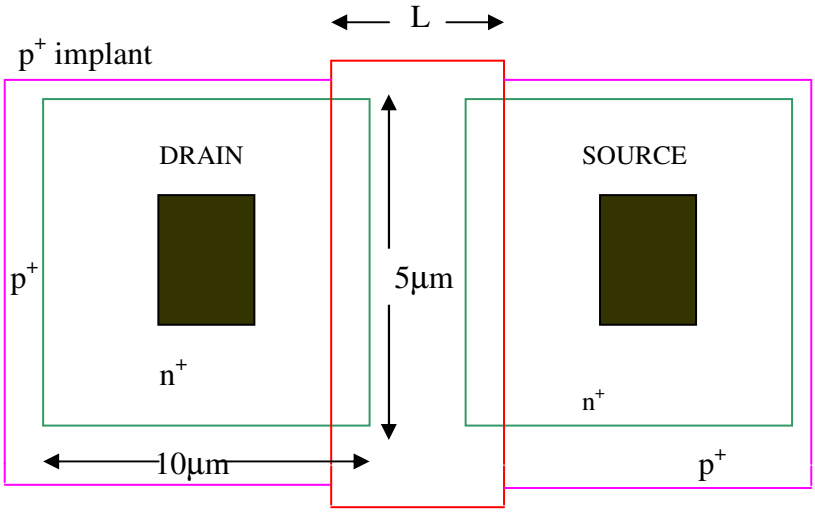

Figure Q3

Q4. The diagram of Figure Q4 is that of an inverter layout with geometry as shown and the channel-width and channel-length dimensions indicated. The SPICE model parameters below are a representation of the pMOS and nMOS transistors used in the design of the inverter.

i) Using the SPICE parameters given below, evaluate the design by determining the capacitive loading at the output of the inverter, given that the wiring has a capacitance of approximately 2fF.

(15 marks)

ii) Obtain an estimate of the delay times for the individual transistors given by $\tau_{PH\text{-}L}$ for the nMOS device and $\tau_{PL\text{-}H}$ for the pMOS device.

(5 marks)

where

$$\tau = \frac{1.6\, C_{LOAD}}{Kp\ (W / L)}$$

iii) Hence evaluate the propagation delay of the inverter

(5 marks)

The SPICE parameters for the inverter are as follows:

PMOS	**NMOS**
Geometric properties:	
$\mathbf{W_p}$ = 15µm	$\mathbf{W_n}$ = 6µm
L = 2µm	**L** = 2µm
AD = AS = 0.7e-10m^2	**AD = AS =** 3.0e-11m^2
PD = PS = 2.8e-5m	**PD = PS =** 1.5e-5m
Electrical properties:	
Gate-drain overlap	Gate-drain overlap
CGDO = 1.7e-10 F/m	**CGDO** = 0.95e-10 F/m
Zero-bias bulk junction-bottom capacitance	
CJ = 0.00018 F/m^2	**CJ** = 7.6e-5 F/m^2
Zero-bias bulk junction capacitance per metre of junction perimeter	
CJSW = 2.8e-10 F/m	**CJSW** = 2.0e-10 F/m
Transconductance	Transconductance
Kp = 1.9e-5 A/V^2	**Kp** = 5.9e-5 A/V^2
Lateral diffusion	Lateral diffusion
LD = 1.8e-7m	**LD** = 1.8e-7m
Gate-oxide thickness	Gate-oxide thickness
tox = 2.2e-8m	**tox** = 2.2e-8m
Permittivity of SiO_2	
$\boldsymbol{\varepsilon_{ox}}$ = 3.51e-13 F/cm	
The voltage equivalence factors:	
$\mathbf{K_{eq}}$ = 0.305 **H-L** pMOS	$\mathbf{K_{eq}}$ = 0.305 **L-H** nMOS
$\mathbf{K_{eq}}$ = 0.187 **L-H** pMOS	$\mathbf{K_{eq}}$ = 0.187 **H-L** nMOS

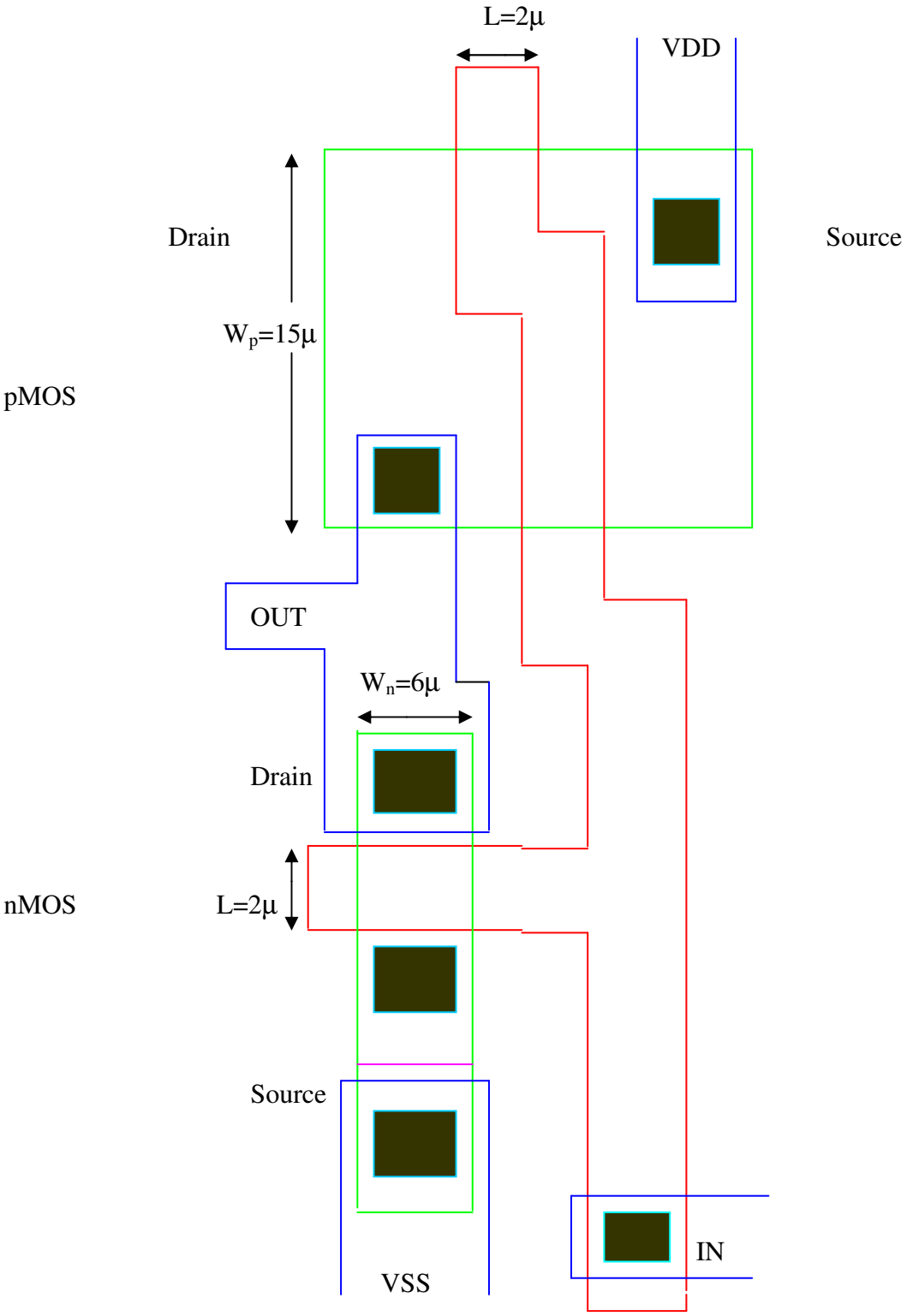

Figure Q4 CMOS Inverter Silicon Floor Layout