## Answer 3 Questions

***The use of Electronic Calculators is not permitted in this examination.***

**Question 1**

(i). Describe in detail how information is stored on a hard disk, in terms of how individual bits of data are stored and also the large scale structuring of the disk. [12 Marks]

(ii). Discuss the factors that control the time it takes to retrieve an item of data from the disk into main memory. [7 Marks]

(iii). How is a disk read transfer set up by the computer and how is the information on where to find the data on the disk located? [7 Marks]

(iv). What is the sequence of events once the transfer has been programmed into the disk interface and how is the data transferred between the main memory and the disk? [7 Marks]

**End of Question 1**

**Question 2**

The diagram on the next page shows the symbolic organisation of a CPU for a RISC architecture with a multi-cycle clocking scheme.

(i). Give an outline description of the operation of this CPU, explaining why there are so many registers and the role of the multiplexers. [12 Marks]

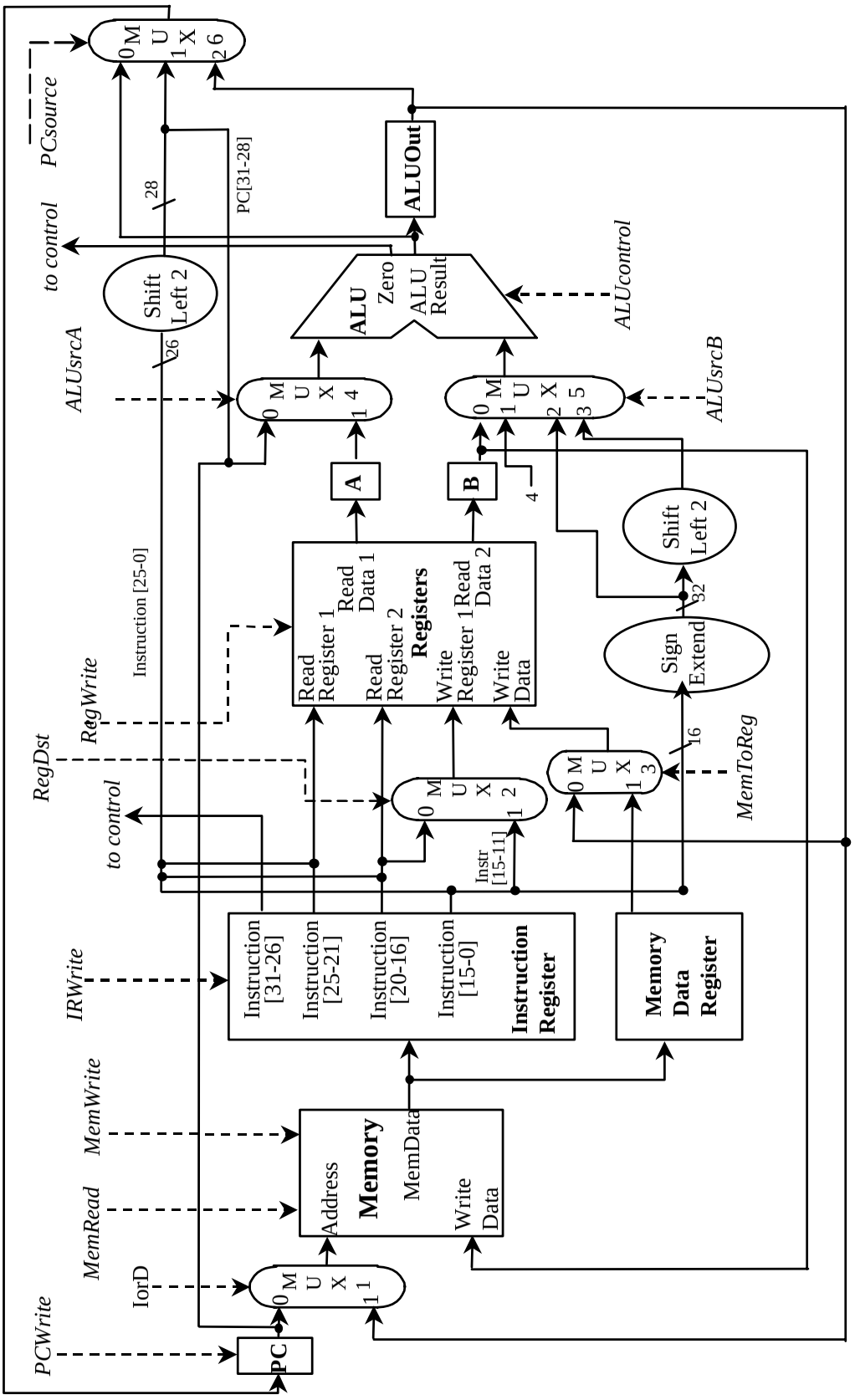
(ii). For multiplexers MUX4, MUX5 and MUX6 explain the purpose of each input and in which operations it is used. [9 Marks]

(iii). The instruction

lw $16, $1234_{16}$($30)

has machine code $9FD01234_{16}$. Explain the encoding of this instruction. [4 Marks]

(iv). Describe the execution of the load instruction of part (iii) by the CPU, identifying the pathways used in terms of the multiplexer ports used, the data values routed on these pathways and the values on the control signals. [8 marks]




**End of Question 2**



**CONTINUE**

**Question 3**

"Dynamic memory needs refresh but static memory does not."

Explain this sentence, describing the two memory types, their access times and their usage. [12 Marks]

Explain how cache memory works and why it is needed?. [8 Marks]

A CPU running in a system with a clock frequency of 1000MHz needs 80 clock cycles to access main memory. It has a 64Kbyte cache with a memory access time of 10ns and a miss rate of 15%.
What is the average memory access time in nanoseconds? State any assumptions made. [6 Marks]

An Intel Pentium processor has separate on-chip code and data caches plus a second level cache between the CPU and the main memory. Why is this arrangement necessary. [7 Marks]

**End of Question 3**

**Question 4**

The following is a function written in MIPS assembler:-

```
mystery:
        add     $sp,  $sp,  -8          // instr 1
        sw      $31,  4($sp)            // instr 2
        sw      $fp,  0($sp)            // instr 3
        move    $fp,  $sp               // instr 4
        add     $sp,  $sp,  -8          // instr 5
        sw      $s2,  4($sp)            // instr 6
        sw      $s1,  0($sp)            // instr 7
        lw      $s0,  8($fp)            // instr 8
        lw      $s1,  12($fp)           // instr 9
        slt     $s2,  $s1,  $s0         // instr 10
        beqz    $s2,  lab1              // instr 11
        move    $s0,  $s1               // instr 12
lab1:
        lw      $s2,  4($sp)            // instr 13
        lw      $s1,  0($sp)            // instr 14
        move    $sp,  $fp               // instr 15
        lw      $fp,  0($sp)            // instr 16
        lw      $31,  4($sp)            // instr 17
        add     $sp,  $sp,  8           // instr 18
        jr      $31                     // instr 19
```

Examine this piece of code and:-

1. describe the operation of the 7 different types of instruction used ; [7 Marks]
2. draw a diagram of the stack at the stage when the program counter holds the address of lab1, and explain its structure and content; [10 Marks]
3. explain the structure of the code, i.e. what do different groups of instructions achieve and to what purpose; [12 Marks]
4. write ‘C’ code equivalent to this program. [4 Marks]

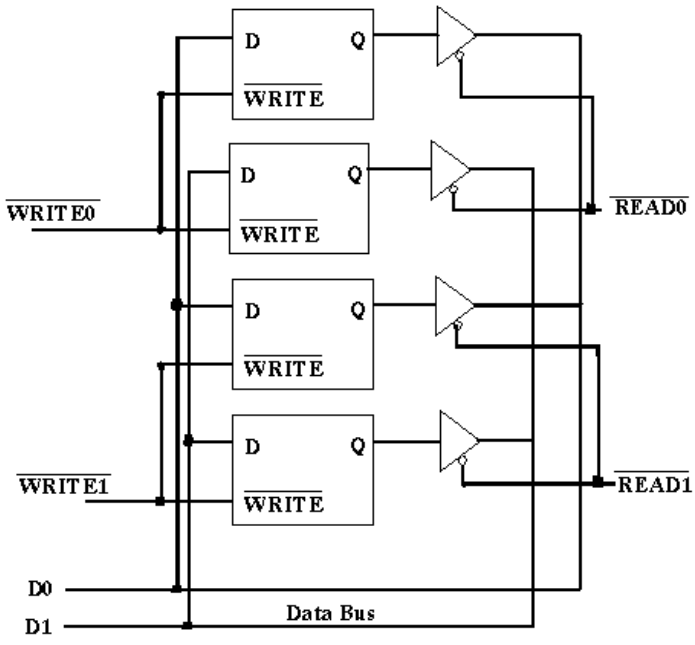
**End of Question 4**

**Question 5**

Describe the operation of the memory circuit in the diagram, giving truth tables for the basic elements.

Explain how the control signals can be generated from address signals from a processor, and why an address is used rather than direct processor control of these signals.

[10 Marks]



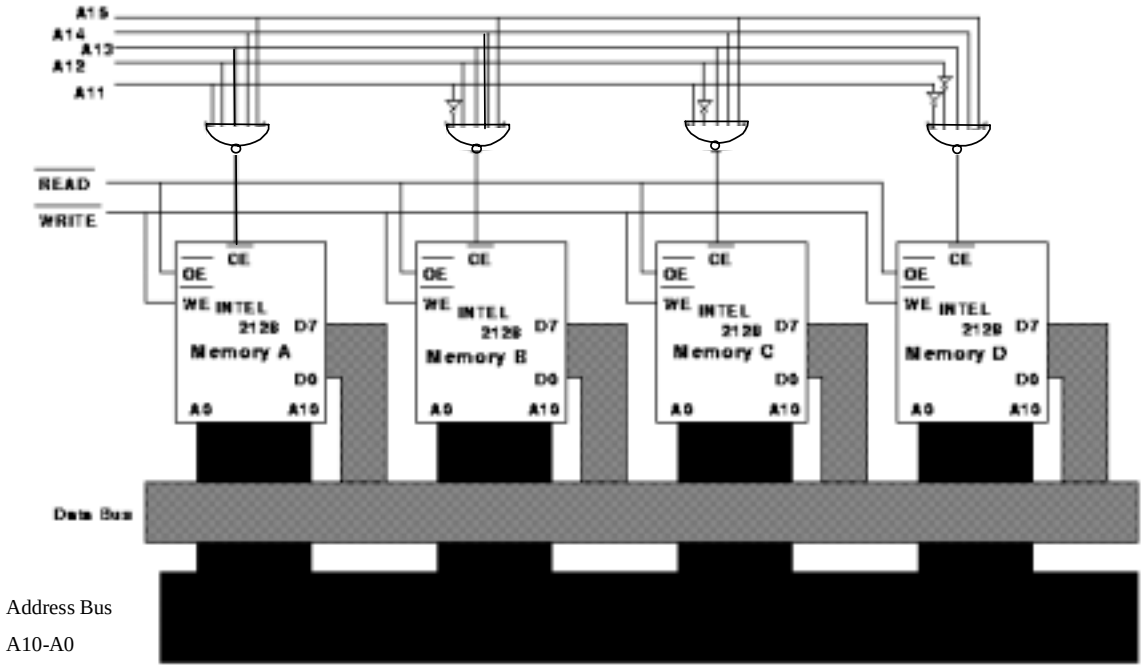

Answer the following questions on the memory circuit below:-

i. How much storage is there at each memory address? [2 Marks]

ii. How many storage locations are there in each of the memory chips? [2 Marks]

iii. What address range does each memory chip cover? [8 Marks]

iv. Describe in detail the changes that must be made to the circuit for the memories to be addressed in the address range $A000_{16}$ to $BFFF_{16}$. [6 Marks]




Describe the signal and operational sequence when a write is performed on chip C?

[5 Marks]

**End of Question 5**



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