## B116 QUESTION PAPER

# DUMMY COVER ORIGINAL <br> EXAMINERS COPY 

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## Answer 3 Questions <br> The use of Electronic Calculators is not permitted in this examination.

## Question 1

(i) What is the role of the interface in performing Input and Output transfers.
(ii) The diagram to the right shows a simple 1-bit input interface in a computer system. Identify the components and signals in the interface and describe what the interface does.

Explain how the interface operates by discussing what happens when the CPU in the system executes a load instruction addressing the interface.
[12 Marks]

(iii) Explain the role and operation of status registers and flow control signals in I/O interfaces.
(iv) Discuss the use of polling, interrupts and DMA in performing I/O transfers.

## Question 2

The diagram on the next page shows the symbolic organisation of a CPU for a RISC architecture with a multi-cycle clocking scheme.
(i) With respect to this diagram, describe the sequence of operations performed by this CPU in fetching and executing a conditional branch instruction, identifying the pathways and multiplexers ports used and the values on the control signals. [assume that the condition tested by the instruction compares the contents of two registers for equality]
[16 Marks]
(ii) Explain how the control logic works to provide for the sequencing of the CPU operations and execution of individual instructions.
(iii ) What is pipelining? Explain why it is used and what limits its effectiveness.
Outline the modifications needed to pipeline the multi-cycle CPU of the diagram.

## Question 3

Answer 2 out of (a), (b) or (c)
a) i) Explain the meaning of the following sentence "The magnetic disk drive has 8 surfaces, 1000 tracks per surface, 50 sectors per track and 1Kbytes per sector".
ii) Why are tracks divided into sectors?
iii) The disk in (i) has an average seek time of 10 ms and rotates at 6000 r.p.m. Estimate the average rotational latency and explain why it is beneficial to store all the data from a file in a single cylinder.
iv) A file occupies 40 sectors on the disk of (iii) and these sectors are randomly distributed over the disk. Calculate the time to read all the file.

The disk is re- organised so that sectors are allocated in blocks of 4 sequential sectors within a cylinder. How long does it now take to read the file, assuming blocks used are randomly distributed over the disk?

What are the possible disadvantages of this re- organisation?
(b) Why are i nterrupts useful and how does the interrupt system work?

A CPU running at 100Mhz performs an instruction every 2 clock cycles on average. On an interrupt, there is a hardware overhead of 8 clock cycles.

An interrupt service routine has been written that transfers one item of data to an output interface. This routine requires 5 instructions to transfer a data item to the interface, but needs an additional 16 instructions for interrupt handling purposes. Calculate the maximum average data transfer frequency.

The interface hardware can be replaced with an improved design that allows several data items to be buffered in the interface and for an interrupt to be generated when the interface buffer becomes empty. This allows several data items to be transferred to the interface for a single interrupt.

What is the minimum size of the interface buffer to achieve an average data rate of 8Mhz?

## Question 3 continued

(c) Many CPUs have a stack. What is the stack and why is it useful? Explain how it is accessed.

A C compiler for a CPU with 32-bit addresses and registers :-

- maps integers, pointers and floats on to 4 bytes of memory
- uses 2 registers for function parameters on a function call
- and uses 2 registers for local variables within a function.

Draw a diagram of the stack frame created on a call to the function insert_record below, explaining its structure and calculate the amount of memory occupied.

```
struct record {
        struct record * next ;
        int reference ;
        int value ;
    };
int insert_record(struct record *ptr, int ref, int val, int count) {
struct record *np = ptr->next ;
    int nr = np->reference;
    struct record *tp ;
    if(ref > nr) {
        return insert_record(np, ref, val, count++) ;
        } else {
            tp = (struct record *)malloc ( sizeof( struct record));
            tp->next = np;
            tp->reference = ref ;
            tp->value = val;
            ptr->next =tp ;
    }
        return count ;
    }
```


## Question 4

(i) A multi-process Operating Systems has a scheduler with the following properties:-

- it is pre-emptive
- it has a round-robin dispatch policy
- the maximum time slice for a process is 2 ms .

Discuss the above with respect to the scheduler model of a process shown in the
 diagram to the right. In your answer, explain the scheduler model including the transitions that a process can make between states of the model.
(ii)) At some time $\boldsymbol{t}$, the Operating System of part (i) has a process X that has been executing for 1 ms , a $2^{\text {nd }}$ process $Y$ is ready for execution, and a $3{ }^{\text {rd }}$ process Z has made a system call to read some data from a file.

The following events occur at the specified times:-

| time $\mathrm{T}+1 \mathrm{~ms}$ | - | a timer interrupt occurs |
| :--- | :--- | :--- |
| time $\mathrm{T}+2 \mathrm{~ms}$ | - | interrupt occurs signalling completion of read of <br> from disk of data for process Z |
| time $\mathrm{T}+3 \mathrm{~ms}$ | - | executing process makes a system call to write to <br>  <br> afile |
| time $\mathrm{T}+4 \mathrm{~ms}$ | - | executing process terminates |
| time $\mathrm{T}+5 \mathrm{~ms}$ | - | executing process forks |

Explain what happens to the processes in the system in response to these events, and the state of each process after $\mathrm{T}+5 \mathrm{~ms}$.

## Question 5

Several forms of storage can be identified in typical computer systems:-
registers, main memory, cache memory, read-only-memory, magnetic disk and tape storage Briefly describe each of these with particular reference to its access time, the lifetime of the data it stores, its typical usage and frequency of access.

Explain why a CPU with a clock frequency of 500 MHz would typically have 2 cache memories, one inside the CPU chip and one external to the CPU chip.

A CPU has 32-bit registers, a 32-bit data bus, and byte-addressable memory (i.e. each memory location holds a byte). Describe the typical main memory organisation for such a system and discuss how 32-bit transfers are performed between registers and memory, with particular reference to the addresses (odd \& even) output by the CPU.

