Computer Science Department
1999 Examinations

B116
QUESTION PAPER

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CONTINUE

Answer 3 Questions

The use of Electronic Calculators is not permitted in this examination.

Question 1

(i) Draw a block diagram showing the typical structure and components of a general-purpose computer system. Explain the role of each element in your diagram and how each is controlled. [12 Marks]

(ii) Give a detailed list of the activities that take place in the system of (i) from when a user starts to type the name of a program file for execution to when the first instruction of the program is executed. [15 Marks]

(iii) In what circumstances and why would cache memory be an advantage in this system? [6 Marks]

End of Question 1

Question 2

(i) Explain the structure, contents, access and reason for use of a stack frame by a high level language. [10 Marks]

(ii) Draw the stack frame that you might expect for the C language function below, assuming that only 2 of the local variables can be held in registers. [6 Marks]

```
int cutdown (int threshold, int *data, int dsize) {
        int i, j ;
        int sum ;
                sum = 0 ;
                if (threshold > 0) {
                        for (i=0 ; i < dsize ; i++) {
                            j = data[i] - threshold ;
                            data[i] = j ;
                            sum = sum + j ;
                        }
                }
                return sum ;
}
```

(iii) Write an assembler language implementation for the C code of (ii). [17 Marks]

[This should be written in a representative assembly language. You will not be marked on the accuracy of your use of any particular language, however, you must restrict yourself to typical assembly language constructs and must make clear the meaning of any novel notations you introduce].

End of Question 2

Turn Over

Question 3

Diagram 5.33 on Page 383 of the course text book shows the symbolic organisation of a CPU for a RISC architecture with a multi-cycle clocking scheme.

(i) With respect to this diagram, describe the sequence of operations performed by this CPU in fetching and executing a single instruction along with the pathways and multiplexor ports used.
[assume that the instruction fetched adds the contents of two registers together and puts the result in a 3rd register] [12 Marks]

(ii) In each of (a) and (b) below, the semantics of an instruction is given. For each of them describe in detail those stages in their execution that are different from the add instruction of (i), detailing as above the routing of data values.

(a) the contents of register 3 + bits 0-15 of the instruction provides the address of the memory from which data is read into register 6. [6 Marks]

(b) bits 0-15 of the instruction multiplied by 4 are added to the PC register if the contents of register 2 is equal to the contents of register 3. [6 Marks]

(iii) Discuss the control logic for this CPU and its sequencing. [9 Marks]

End of Question 3

Question 4 B116 1999

(i) Operating systems play an important role in computer systems. Explain why this is, describing what they provide. [13 Marks]

(ii) Give a detailed explanation of the Process Life Cycle. [12 Marks]

(iii) Multiple processes running on a multi-processed, pre-emptive operating system all access a single resource. The code for each process includes the code fragment below which is intended to ensure that just one process may access the resource at any time. In this code *sleep()* is a system call which asks the operating system to suspend the current process until some other process executes a *wakeup()* system call: *Flag* is a shared memory location.

```
while (flag = 0)   sleep();
flag = 1;
access_shared_resource();
flag = 0;
wakeup();
```

Explain why this code does not perform as intended. [8 Marks]

End of Question 4

Question 5

(i) Interrupts, polling and DMA are different methods for performing I/O. Explain how each of these operates, and their hardware requirements. [15 Marks]

(ii) Discuss the strengths and weaknesses of interrupts, polling and DMA. [8 Marks]

(iii) A CPU running at 100Mhz performs an instruction every clock cycle. On an interrupt, there is a hardware overhead of 8 clock cycles. An interrupt service routine has been written that transfers one item of data to an output interface, and this routine has a 20 instruction overhead and requires 12 instructions to transfer the data item to the interface. Calculate the maximum average data transfer frequency. [4 Marks]

(iv) The interface hardware of (iii) can be replaced with an improved design that allows several data items to be buffered in the interface and for an interrupt to be generated when the interface buffer becomes empty. This allows several data items to be transferred to the interface for a single interrupt. What is the minimum size of the interface buffer to achieve an average data rate of 6Mhz? Assume the instruction overhead and the instructions to transfer a data item stay the same. [6 Marks]

End of Paper