Answer 3 Questions

The use of Electronic Calculators is not permitted in this examination.

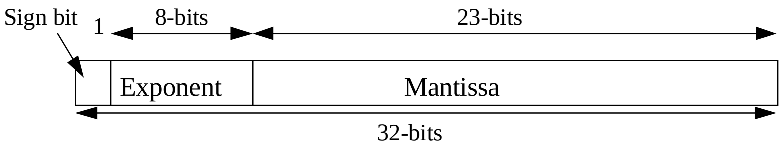
Question 1: answer all parts (i), (ii), (iii)

(i)

(a) Explain the 2’s complement method used to represent signed integers in computer systems and why it is used. Illustrate your answer with examples. [8 Marks]

(b) Find the result of subtracting 1E90 from 38B7 where both numbers are hexadecimal representations of 16-bit 2s-complement binary numbers. [3 Marks]

(ii) The figure shows the fields for a 32-bit representation of a floating point number.



Explain how the IEEE single precision floating point number standard makes use of these fields to represent numbers, giving a formula for the relationship between the number represented and the fields in the representation, and explaining the difference between normalised and un-normalised numbers.

What are the largest and smallest (non-zero) positive numbers represented in this format?

What are the advantages of the field encoding over other possibilities?

[11 Marks]

(iii) Give the result in IEEE single precision format of subtracting **C2A2C000** from **44F5D400**, where both numbers are hexadecimal representations of IEEE single precision format numbers. [11 Marks]

End of Question 1

Question 2

(i) A CPU has a byte-addressable memory, 32-bit registers, and a 32-bit data bus. Describe the typical memory organisation for such a system. A single *move* instruction for this system contains a single memory address and yet may transfer 1, 2 or 4 bytes from the CPU into memory. Explain how this is achieved. [12 Marks]

For this system what memory locations are accessed and how many transfers are made for the following *move* instructions specified in Register Transfer Language:-

(a) $12345678_{16} \xrightarrow{32} (ABCDEF02_{16})$

(b) $2345_{16} \xrightarrow{16} (ABCDEF03_{16})$

[4 Marks]

What organisation, big-endian or little-endian, have you assumed in your answers to (a) and (b)? What difference would it make if you had assumed the opposite assumption.

[3 Marks]

(ii) In this question you are asked to write a small assembler program to demonstrate your understanding of CPU operation. The program should be written in a representative assembler language. You will not be marked on the accuracy of your use of any particular language. However, you must restrict yourself to typical assembler language constructs and must make clear the meaning of any novel notations you introduce.

A character string is stored as a byte-array of ASCII codes starting at location 0x40002000. The string is terminated by a zero byte. Write an assembler language program to search the array for a character whose ASCII code is stored in register D3. The program should terminate with 1 stored in register D0 if the character is present, 0 otherwise. [14 Marks]

End of Question 2

Question 3

Stacks and queues are examples of dynamic data structures. Explain fully the operation and use of both of these in computer systems and discuss their implementation.[10 Marks]

Describe the hardware support for a stack to be found in a typical modern microprocessor CPU and detail the operation of the *subroutine call* and *return* instructions. How can a stack be used to support recursive subroutine calls? [8 Marks]

```
void mystery(int* a, int* b, int c){
int x, i, j ;
    for (i = 0; i < c; i++){
        x = 0;
        for (j = 0; j < c; j++){
            if (a[j] < a[i]){
                x += 1;
            }
        }
        b[x] = a[i];
    }
}
```

Draw the stack frame for the above C function just prior to the execution of the instruction **x=0** and give example assembler code for this instruction. [8 Marks]

How would the stack frame differ if the variable **x** was held in a register, and how would this affect the execution of the function? Is there a better choice of variable to hold in a register? [7 Marks]

End of Question 3

Question 4

Write fully on **2** of the following:-

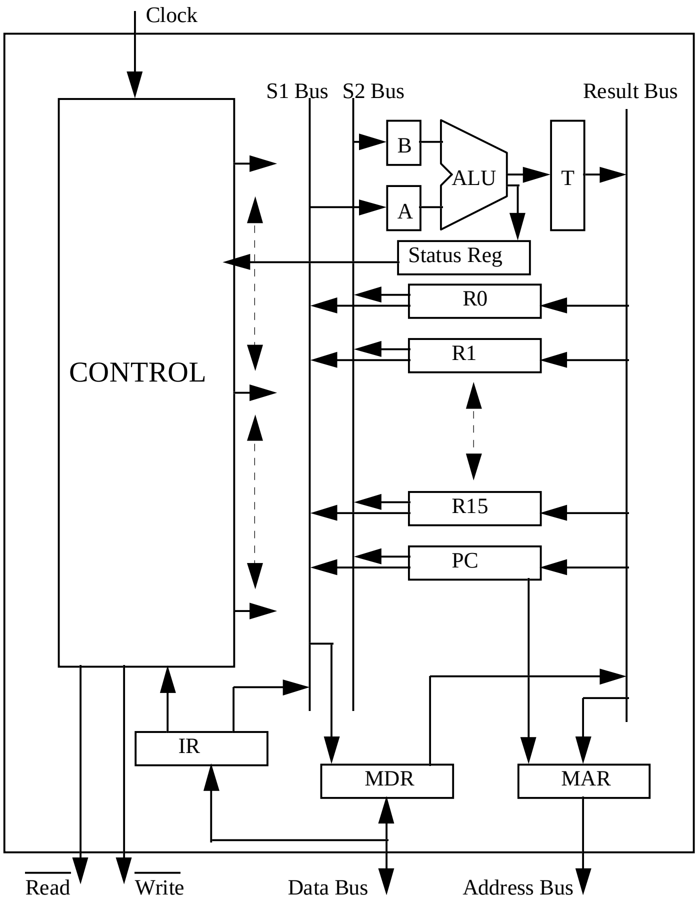
i) DMA versus an interrupt per data item for input-output. [16 Marks]

ii) Paging. [16 Marks]

iii) The role of the I/O interface and its logical structure from a programmer's perspective. [16 Marks]

iv) Superscalar & VLIW architectures. [16 Marks]

End of Question 4



(a) The diagram shows the internal architecture of a CPU. It has 5 busses. Explain the role of each of the busses. [6 Marks]

(b) What are tri-state drivers? Why would they be needed on the outputs of the registers connected to the S1 and S2 Busses? [4 Marks]

(c) Describe the sequence of events that occur from the moment when the CPU moves into its instruction fetch phase until the end of the execution phase of the instruction that is fetched, assuming that the instruction fetched adds the content of register ***R1*** to register ***R15***. [10 Marks]

(d) Give a timing diagram for the machine cycle that accesses the memory during the fetch phase of part (c). [5 Marks]

(e) Give a detailed explanation of pipelining and explain why the CPU in the diagram has been designed to be pipelined. [8 Marks]

End of Question 5

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