Answer QUESTION ONE and TWO other questions.

1.

a) Briefly explain the most important points of **eight** of the following terms in the context of computer architecture

a. Instruction execution cycle
b. Exception
c. Register
d. Pipeline
e. Subroutine linkage
f. Bus
g. Memory-mapped input/output (I/O)
h. Interrupt
i. Direct memory access (DMA)

[3 marks each; 24 in total]

b) Identify the main factors which affect the structure and size (number of bits) of instructions in digital computers.

[9 marks]

2.

a) Briefly explain what you understand by the terms *Complex Instruction Set Architecture (CISC)* and *Reduced Instruction Set Architecture (RISC)*, indicating their advantages and drawbacks.

[8 marks]

b) You are asked to advise on buying a fast computer for a friend. They are considering either a 166MHz Pentium Pro (CISC) or a 160MHz Apple machine (RISC). What are the main factors that affect the performance of computers? What advice would you give to your friend and why?

[12 marks]

c) What are *temporal locality* and *spatial locality*? Explain how these concepts are used to improve the performance of computers.

[13 marks]

TURN OVER

3.

a) Why is memory management needed in modern computer systems?

[5 marks]

b) Explain how *paging* works, using as an example a byte addressed machine with a 32-bit address space and pages 64k bytes long.

[12 marks]

c) Explain the difference between *primary memory* and *secondary memory*. Describe the types of data storage technology used in these areas, and explain why they are appropriate to these parts of the computer system.

[16 marks]

4.

a) Explain why *2's complement* is the preferred system for representing signed binary numbers.

[4 marks]

b) Consider the 8-bit binary number

10110101

Calculate its decimal value if it is interpreted as

(i) an unsigned integer

(ii) an integer in sign-and-magnitude format

(iii) a 2's complement integer

(iv) an excess-127 biased exponent

[8 marks]

c) Write out the above 8-bit number in *hexadecimal* notation.

[2 marks]

[Qu.4 cont. over page]

[Qu.4) continued]

d)

(i) Complete the truth table below for a *full subtractor*, ie a device that subtracts the binary digit a_2 from the binary digit a_1 to give another binary digit, the difference d, taking into account a 'borrow in' b_{in} from a previous subtraction step and passing a 'borrow out' b_{out} to the next step

a_1	a_2	b_{in}	**d**	b_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[6 marks]

(ii) Write down an algebraic expression for b_{out} as a function of a_1, a_2 and b_{in} in *first canonical form*.

[3 marks]

(iii) Simplify the expression you have obtained using a *Karnaugh map*.

[4 marks]

(iv) Implement your simplified expression as a combinatorial circuit using AND, OR and NOT gates.

[6 marks]

5.

a) What is meant by a *bistable*?

[4 marks]

b) Why are the ranges of input voltages defined as 'logical 0' and 'logical 1' greater than the corresponding output voltage ranges?

[4 marks]

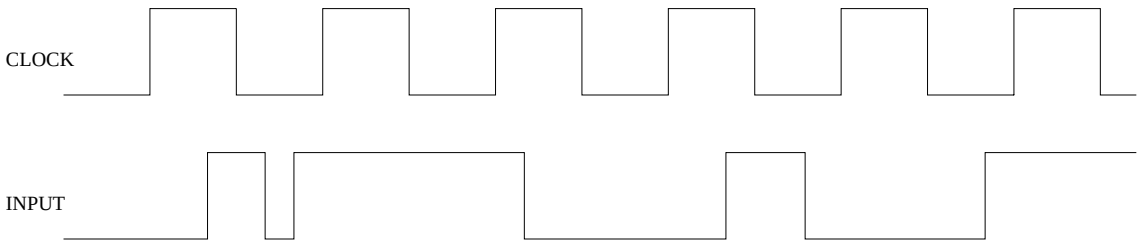
c) What happens when both the R ('reset') and S ('set') inputs to an RS flip-flop are simultaneously equal to 1?

[3 marks]

d) Explain the advantages of the D-type flip-flop in comparison to the RS flip-flop. Refer to truth tables defining their operation as necessary .

[6 marks]

e) Consider the clock and input waveforms below.



Provide a timing diagram for the Q output of a D flip-flop. Assume that the flip-flop is

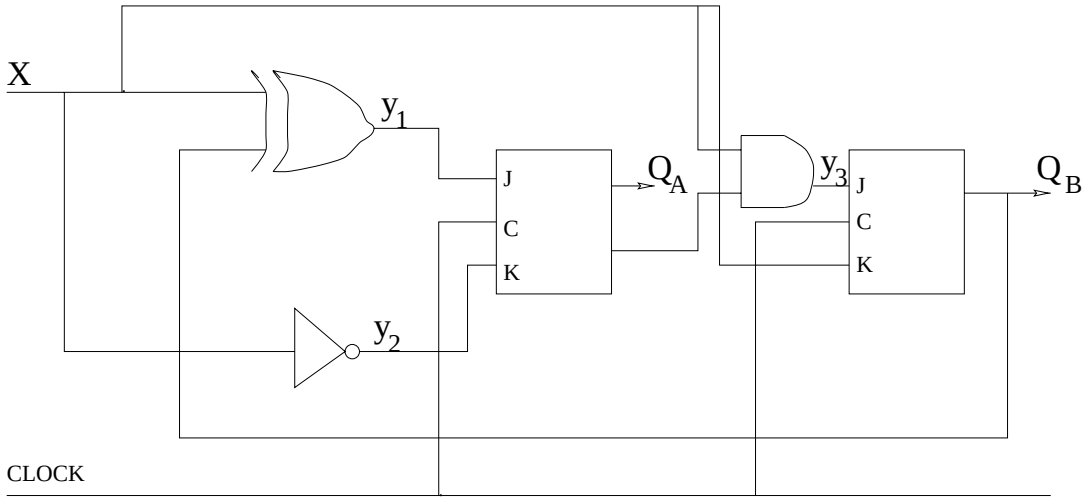
(i) level sensitive
(ii) rising edge triggered
(iii) falling edge triggered

[6 marks]

[Qu.5 cont. over page]

[Qu.5) continued]

f) Consider the sequential circuit below



Assuming that all flip-flops are reset to Q = 0 at t = 0, investigate the behaviour of the above circuit by copying and completing the table below

Time	**X**	y_1	y_2	Q_A	y_3	Q_B
0	-	-	-	0	-	0
1	1	1	0	1	0	0
2	1					
3	1					
4	1					
5	1					
6	0					
7	1					
8	0					
9	0					
10	0					
11	0					
12	0					
13	1					
14	1					
15	1					

[10 marks]

END OF PAPER