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B.Sc. inComputer Science, 2000 1B10

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EXAMINATION QUESTIONS

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QUESTION 1

a) Outline, with diagrams if necessary, the instruction fetch and execute cycle of a conventional modern computer. Your answer should make reference to the Program Counter, the ALU, the clock, general registers, and memory access. **[13 marks]**

b) If you were designing a new computer with a new instruction set, what are the tradeoffs between code size and CPU complexity that would influence your choice of whether to use 0-operand, 1-operand, 2-operand or even 3-operand instructions. Use examples of code fragments to illustrate your points. **[13 marks]**

c) Java is normally compiled into a form of assembler called byte code. Byte codes are often the type of instruction set known as a "stack machine" – explain what this sort of machine if like with reference to the kind of instructions, operands and memory model that it might have. [**7 marks]**

QUESTION 2

a) The instruction set of a typical computer has some support for subroutine linkage. Explain how control is passed to a subroutine, and return is made. Your answer should cover the use of the registers and the stack in providing for parameter passing, return values and return addresses. **[21 marks]**

b) Why is it not sufficient to store parameters and return values and addresses in fixed memory locations? **[6 marks]**

c) What are "register conventions" and why are they important? **[6 marks]**

QUESTION 3

a) Explain the structure and purpose of cache memory systems. **[12 marks]**

b) Qualitatively, what is the tradeoff between cache size and cache block size and performance? Make use of a rough graph if it will help. **[6 marks]**

c) Outline the reason for and structure of Virtual Memory Systems. Your answer should include an explanation of the way that a simple direct mapped page table works.

[15 marks]

END OF PAPER

QUESTION 4

a) Modern CPUs are "pipelined". What does this mean, and how does it achieve a performance improvement? **[9 marks]**

b) What are "hazards" to pipelining? Give 3 examples. [**12 marks]**

c) How can hazards be avoided or circumvented. Give a method for each of the cases in b).

[12 marks]

END OF PAPER

QUESTION 5

a) Explain how input and output are achieved using

i) special instructions

ii) memory mapped I/O

[6 marks]

b) Outline the mechanisms of polled and interrupt driven input and output.

[9 marks]

c) Why is polled input not used for high speed devices such as disks?

[6 marks]

d) What is DMA? **[6 marks]**

e) What is a bus? Explain why there may be as many as 3 (or more) in a modern computer.

[6 marks]

END OF PAPER