## 2 HOURS 30 MINUTES

## ANSWER ALL 3 QUESTIONS

## Electronic calculators are not permitted.

Each question carries a mark of 25 . The total mark will be scaled to a percentage.

## Question 1 Answer all parts (a) -(e).

(a) Explain what we mean by a polynomial-time reduction of a decision problem $A$ to a decision problem $B$.
(b) Define the satisfaction problem for propositional logic (PSAT).
(c) Consider the following graph colouring problem (3GCOL). An instance of 3GCOL is any undirected, finite graph $G . G$ is a yes-instance if it is possible to colour each edge of $G$ either red ( $r$ ), yellow ( $y$ ) or blue ( $b$ ) (but no edge must be coloured by two distinct colours) in such a way that two incident edges are never given the same colour. If $G$ cannot be coloured in this way, it is a no-instance.

Which graphs (below) are yes-instances of 3GCOL and which are no-instances?


(iv)

(ii)
(iii)


(v)
(d) Let $G$ be any undirected, finite graph. Write a formula $\phi(G)$ which is satisfiable if and only if $G$ is a yes-instance of 3GCOL. [Hint: for each edge $e$ of $G$ and for $c=r, y, b$ define a proposition $p_{e, c}$. The idea is that $p_{e, c}$ should be true if the edge $e$ is coloured by c.] Deduce that 3GCOL reduces to PSAT in polynomial time.
(e) Given that PSAT is NP-complete, what can you deduce about the complexity of 3GCOL?

## Answer both parts, a and b.

(a) Consider the $\mathrm{C} / \mathrm{C}++$ statement
do
sum = sum $+100 ;$
while (sum <= 1000);
(i) By reference to the above example, explain the terms
lexeme, keyword, token, token type, and token value.
(ii) Show the kind of code which a simple compiler might generate for a stack machine from the statement.
(b)
(i) Draw a syntax diagram for the (generic) $\mathrm{C} / \mathrm{C}++$ do-while statement. You may assume that syntax diagrams for statement and expression (including truth-valued expressions) exist.
(ii) Suppose that the existing syntax diagrams for expression do not cover the boolean operators \| (or) and \&\& (and). Show how, using the diagrams defining expression, you would incorporate the boolean operators with their $\mathrm{C} / \mathrm{C}++$ priorities into expressions. State any assumptions you make.
(iii) Annotate your syntax diagrams so as to generate code for a simple stack-based machine.
(iv) Sketch an implementation of your syntax diagrams as procedures (functions) in a recursive-descent compiler. Briefly describe the purpose of any other procedures or variables to which your implementation refers. In the case of variables, for each one you should make it quite clear whether it is local or global, and explain why. You may refer to newlabel(), a function which returns a unique label each time it is called.

Your implementation should work with nested constructs, and you should indicate how your design allows this.


## Answer part (a):

(a) With regard to the CPU in the figure above, describe the sequence of events that occur from when the CPU moves into its instruction fetch phase until the end of the execution phase of the instruction that is fetched, assuming that the instruction fetched adds the content of register $\boldsymbol{r} \mathbf{1}$ to register $\boldsymbol{r} 15$.

## Answer any 2 parts from parts (b)-(e):

(b) Discuss the organisation of a register for the CPU in the figure above, explaining in detail how bits of information are stored.
(c) Draw a 3-input NAND gate using resistors and simple electronic switches. Discuss the operation of the circuit in terms of changes in voltage, current flow and power consumption, when the inputs go through the sequence 00 -> 10 -> 11 -> 01 . Explain the role of any resistors and explain the factors affecting the decision on the magnitudes of their resistance.
(d) Draw a diagram of an MOS n-transistor and briefly explain its operation. What happens if the substrate is connected to the 5 V side of the power supply rather than the 0 V one as is usual?
(e) Draw the truth table for the Finite State Machine (FSM) with the following State Diagram:


Use Karnaugh maps or other technique to derive the equations for the next state bits.
Draw the final circuit for the finite state machine using AND, OR and INVERTER gates and flip-flops for the state store.

