Answer ANY THREE questions.
If you answer more, the best three answers will be taken into account.

1. (a) Give the truth table that describes the operation of a NOR (Not OR) logic gate.

[4 marks]

(b) What is a gate diagram and what does it typically represent?

[2 marks]

(c) Draw the gate diagram for the circuit described as follows:
There are two circuit inputs named R and S and two circuit outputs named P and Q. The outputs P and Q are additionally fed back into the circuit, so that P depends on Q and Q depends on P. The circuit implements the following Boolean logic expressions:

P = R NOR Q
Q = S NOR P

[6 marks]

(d) Assume that at time t = 0, P = 0 and Q = 1. Copy and complete the table below by calculating the values of the outputs P and Q at each of the times t = 2, t = 3, ..., t = 10, using in each case the tabulated input values R and S at time t, and the values of P and Q at time (t - 1).

Time	R	S	P	Q
0	-	-	0	1
1	0	0	0	1
2	0	1		
3	0	0		
4	1	0		
5	0	0		
6	1	0		
7	0	0		
8	0	1		
9	0	0		
10	0	1		

[12 marks]

(e) From the values calculated in the above table, how would you describe (in general terms) what this circuit does (i.e. what useful property or properties does it have)?

[9 marks]

[Total 33 marks]

[TURN OVER]

2. (a) Explain what is meant by the “principle of locality” in memory systems, and why it is important. What is meant by the terms “cache hit” and “cache miss” in the context of memory hierarchy?

[10 marks]

(b) There is an 8 word direct mapped cache, with a word length of 8 bits. The cache block size is one word. Initially the cache is empty, and the following sequence of memory addresses are referenced for reading: 17, 6, 22, 8, 17, 24. Show the state of the cache after each read, using this to explain how such a system works. How would such a system need to be amended to fully take account of the principle of locality?

[15 marks]

(c) Explain what is meant by “virtual memory” and in particular how a virtual address is mapped to a physical address.

[8 marks]

[Total 33 marks]

[CONTINUED]

3. (a) When a MIPS program is running, where in the main memory are different kinds of information stored, and what are those different kinds of information? As part of your answer you should provide a diagram illustrating the layout of information in main memory and you should give examples of how MIPS instructions correspond to the use of each different kind of information.

[12 marks]

(b) What is the primary danger inherent in the memory layout that you have described in the previous part to this question? How might this danger be resolved, and what is the disadvantage of your solution?

[9 marks]

(c) For what purposes is a “stack” used in a MIPS program?

[8 marks]

(d) What is a recursive procedure, and how might a recursive procedure encounter a problem related to the stack?

[4 marks]

[Total 33 marks]

[TURN OVER]

4. (a) Draw a diagram of the main functional components of a computer system. Your diagram should include any necessary communications lines and should include the floating point co-processor.

[11 marks]

(b) Explain, *with examples,* the internal representation of a floating point number. You should include in your explanation (i) how many bits are used for the various components (ii) how both negative and positive exponents are expressed, and (iii) both *how* and *why* part of the number is regarded as "implied" rather than directly expressed. Do *not* attempt to explain overflow.

[10 marks]

(c) What are the largest and smallest floating point numbers that can be represented using the IEEE 32 bit floating point standard?

[4 marks]

(d) If **x** and **y** are two floating point variables in a C++ program, what is potentially dangerous about the following C++ expression:

```
if (x == y) {
    cout << "x and y are equal";
}
```

[2 marks]

(e) Explain with an example how to perform addition on two floating point numbers using the IEEE 32 bit floating point standard.

[6 marks]

[Total 33 marks]

[CONTINUED]

5. (a) Associate each of the registers shown below, labelled (1) to (5), with the description that best fits taken from the sentences labelled (i) to (v). Each description can be used with only one of the the registers. Write your answer in the form "(a) means (b)" where (a) is the number of one of the registers (i.e. 1 to 5) and (b) is the number of the description (i.e. i to v).

(1) register 0	(i) used to provide additional data to a sysop command
(2) register 2 ("v0")	(ii) holds the stack pointer
(3) register 4 ("a0")	(iii) tells the sysop assembler command what operation to perform
(4) register 29	(iv) holds the return address
(5) register 31	(v) always holds the value zero

[5 marks]

[QUESTION 5 CONTINUED ON NEXT PAGE]

[TURN OVER]

[QUESTION 5 CONTINUED]

(b) Explain both in detail and in general terms what the following MIPS code does, and illustrate your explanation with an example C++ procedure that mimics the functionality of the MIPS code.

```
copy:   addi $29, $29, -4
        sw   $31, 0($29)
        addi $29, $29, -4
        sw   $4,  0($29)
        addi $29, $29, -4
        sw   $5,  0($29)
        addi $29, $29, -4
        sw   $6,  0($29)
        addi $29, $29, -4
        sw   $7,  0($29)
        addi $29, $29, -4
        sw   $8,  0($29)
        li   $4, 0
        lw   $5,  32($29)
loop:   bge  $4, $5, return
        mul  $6, $4, 4
        lw   $8, 28($29)
        add  $8, $8, $6
        lw   $8, 0($8)
        lw   $7, 24($29)
        add  $7, $7, $6
        sw   $8, 0($7)
        addi $4, $4, 1
        j loop

return: lw   $8, 0($29)
        addi $29, $29, 4
        lw   $7, 0($9)
        addi $29, $29, 4
        lw   $6, 0($29)
        addi $29, $29, 4
        lw   $5, 0($29)
        addi $29, $29, 4
        lw   $4, 0($29)
        addi $29, $29, 4
        lw   $31, 0($29)
        addi $29, $29, 4
        addi $29, $29, 4
        addi $29, $29, 4
        addi $29, $29, 4
        jr $31
```

[28 marks]
[Total 33 marks]

[END OF PAPER]