PAPER CODE NO. COMP303	EXAMINER : **Dr Dave Jackson** DEPARTMENT : Computer Science Tel. No. **43678**

JANUARY 2001 EXAMINATIONS

Bachelor of Arts : Year 3
Bachelor of Engineering : Year 3
Bachelor of Science : Year 3
Bachelor of Science : Year 4

COMPUTER SYSTEMS AND ARCHITECTURE

TIME ALLOWED : Two Hours and a Half

INSTRUCTIONS TO CANDIDATES

Answer **four** questions

If you attempt to answer more than the required number of questions (in any section), the marks awarded for the excess questions will be discarded (starting with your lowest mark).

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1. (a) Describe what is meant by the Principle of Locality. What is the explanation for this phenomenon?

Explain how the Principle extends to the notion of the working set W(T,s). Give the formula for estimating the working set at a future time interval.

(7 marks)

(b) In an operating system that makes use of paging, page references are made in the following sequence (assume references are made at unit time intervals):

```
page  |A|B|C|B|B|B|A|C|C|B|
time  0 1 2 3 4 5 6 7 8 9 10
```

What are the values of the following (explain your answers):

(i) W(0,4)
(ii) W(3,3)

By using the formula you gave in part (a), predict the working set W(10,3)

(9 marks)

(c) Using the same sequence given in part (b), assume that page D now arrives, and that one of the pages A,B,C must be discarded to make room.
For each of the page replacement policies below, say which page must be replaced and give your explanation.

(i) LRU
(ii) FIFO
(iii) LFU

(9 marks)

2. A given computer uses 32-bit addressing. The computer uses direct cache mapping, for which a block size of 16 bytes has been selected. In addition to storing tag fields, the cache memory is capable of holding 32Kbytes of data.

(a) Give the values of the following for this machine, explaining your answers:

(i) the size in bits of the *offset* field of an address
(ii) the size in bits of the *line no*. field
(iii) the size in bits of the *tag* field

(12 marks)

(b) Describe the direct cache mapping process for this machine.

(8 marks)

(c) What are the disadvantages of the direct mapping approach, and how are these disadvantages overcome in alternative mapping schemes?

(5 marks)

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3. The diagram overleaf shows the microarchitecture of the hypothetical Mic-1 computer.

(a) Describe the data path of this architecture, paying particular attention to the way in which the microcode controls the data path logic.

(12 marks)

(b) Below is the microcode that implements one of the macroinstructions on this machine. Explain what each line of microcode does. Hence, summarise the effect of the macroinstruction.

```
INSTR:  A=SP, B= -1, ADD, C=SP
        A=PC, B=SP, LDMAR, LDMBR, WR
        A=IR, B=AMASK, AND, C=PC, WR, JMP START
```

(13 marks)

4. One of the attributes of a RISC processor is that it should provide support for the implementation of high-level languages. With the aid of suitable diagrams, explain in detail how:

(a) the Berkeley RISC provides support for efficient procedure call and return (14 marks)

(b) the Transputer supports concurrent processing (11 marks)

5. (a) In a small-scale multiprocessor system, 4 processors are to be connected to 4 memory modules. Explain with the aid of diagrams how each of the following connection strategies could be used for this.

(i) bus system
(ii) crossbar
(iii) omega network

(12 marks)

(b) How many switches would be required to connect 64 processors to 64 memory modules using

(i) crossbar
(ii) omega network

(5 marks)

(b) Describe what is meant by a NUMA multiprocessor system, and explain what operational characteristic of such systems gives them their name. What is one of the biggest problems associated with NUMA systems?

(8 marks)

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