| PAPER CODE NO. COMP303 | EXAMINER : **Mr PH Leng, Mr M Zito**<br>DEPARTMENT : Computer Science Tel. No. **3673** |
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# JANUARY 2000 EXAMINATIONS

Degree of Bachelor of Engineering : Year 3
Degree of Bachelor of Science : Year 3

## COMPUTER SYSTEMS AND ARCHITECTURE

**TIME ALLOWED : Two Hours and a Half**

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**INSTRUCTIONS TO CANDIDATES**

All questions carry equal marks. Questions are marked out of 25.

**ANSWER FOUR QUESTIONS ONLY**

If you attempt to answer more than the required number of questions, the marks awarded for the excess questions will be discarded (starting with your lowest mark).

**1.** Modern large-scale computer systems are expected to provide, amongst other features, (1) dynamic memory allocation to multiple processes, (2) information sharing between processes, and (3) support for structured high-level-language programming.

(a) What problems are encountered when trying to support these features within a simple linear-memory architecture?

**(10 marks)**

(b) Discuss the contribution that can be made by
(i) segmentation and
(ii) paging
to solving these problems.

**(10 marks)**

(c) What new problems may be introduced by these more complex memory organisations?

**(5 marks)**

**2.**(a) Outline the principle of a pipelined computer. Explain what is meant by a pipeline hazard, and describe the three kinds of hazard which may be encountered.

**(8 marks)**

(b) A hypothetical computer has a regular instruction set, with the typical form of instruction being, for example:

ADD A, B, RES

interpreted as RES := A+B
The processor executes these instructions using a pipeline of six stages, namely: fetch instruction, decode, fetch first operand, fetch second operand, execute instruction, store result. Each stage is of equal duration.
Consider the following sequence of instructions:

```
ADD A, B, TEMP1
ADD P, Q, TEMP2
SUB TEMP1, TEMP2, TEMP3
BLT TEMP3, 0, OUT ; (IF TEMP3 < 0then GOTO OUT)
ADD 1, COUNT, COUNT
BLT COUNT, LIMIT, LOOP
```

(i) Identify the hazards which might be encountered in this pipeline, explaining how they would occur.

**(8 marks)**

(ii) Briefly discuss possible solutions for each type of hazard.

**(9 marks)**

**3.**(a) Explain what is meant by a cache memory. What general principles are used to make effective use of cache memory?

**(8 marks)**

(a) Outline the three cache mapping policies: direct mapping, associative mapping, and set associative mapping. Briefly discuss the advantages and disadvantage of each.

**(8 marks)**

(b) Use an example of an instruction cache to describe the operation of a direct-mapped cache in detail.

**(9 marks)**

**4.**(a) Describe the four major security threats to a distributed system.

**(3 marks)**

(a) Describe four methods by which security violations can be perpetrated in distributed systems.

**(3 marks)**

(b) Cryptography is one possible way of protecting the information in a system. Describe the two most important types of encryption system. Draw a diagram inn each case.

**(7 marks)**

(c) Assume the code for the $i$-th letter of the alphabet is the number $i$ - 1: the code for "a" is 0, the code for "b" is 1 and so on. These numbers are represented as 5 bit binary strings in the computer's memory. English words are encoded as sequences of integers: the code for the word "dog" is "3 14 6" (represented in binary as "00011 01110 00110"). Compute the sequence of integers encrypting the code for the word "cat" using Rivest Shamir and Adleman's algorithm (use the following values for the parameters related to the algorithm

$$P = 13 \quad Q = 17 \quad K_D = 5 \quad K_E = 77$$

and assume that the input sequence is subdivided in blocks of bits of length $k = 5$).

**(12 marks)**

**5.**(a) List the design and implementation issues involved in processor allocation in distributed systems.

**(8 marks)**

(a) Describe the main features of Mutka and Livny centralised algorithm for processor allocation.

**(8 marks)**

(b) Assume 5 processors $P_1$, $P_2$, $P_3$, $P_4$, $P_5$ are given. The following two sequences represent the estimated completion time (in milliseconds) of 16 processes to be executed in this system.

(i) 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 40

(ii) 10 10 40 10 10 10 10 10 10 10 10 10 10 10 10 10

Using a graph in each case, show the load of each of the five processors after the allocation is completed using the greedy algorithm for dynamic load balancing.

**(4 marks)**

(c) If all processes have similar completion times, an alternative allocation heuristic is obtained by choosing the processor on which a given process will be executed uniformly at random from the set of available processors.
Using the sequence of random choices in the set $\{P_1, P_2, P_3, P_4, P_5\}$ given below, simulate this algorithm with the sequences of job sizes above.

Random processor choices: $P_4\ P_5\ P_5\ P_2\ P_4\ P_2\ P_1\ P_1\ P_1\ P_2\ P_3\ P_3\ P_3\ P_4\ P_1\ P_3$.

**(5 marks)**