PAPER CODE NO. COMP303	EXAMINER : **Dr Dave Jackson** DEPARTMENT : Computer Science Tel. No. **43678**

THE UNIVERSITY
of LIVERPOOL

JANUARY 2002 EXAMINATIONS

Bachelor of Arts : Year 3
Bachelor of Engineering : Year 3
Bachelor of Science : Year 3
Bachelor of Science : Year 4

COMPUTER SYSTEMS AND ARCHITECTURE

TIME ALLOWED : Two Hours and a Half

INSTRUCTIONS TO CANDIDATES

Answer ***four*** question

If you attempt to answer more than the required number of questions (in any section), the marks awarded for the excess questions will be discarded (starting with your lowest mark).

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Answer **four** questions

1.
(a) With the aid of a diagram, explain what is meant by the storage hierarchy.

(6 marks)

(b) A computer uses 24-bit addressing, and for the purposes of caching the memory is considered as being divided into 4-byte blocks. If the CPU needs to access address 00001D (hex),
(i) what block number should it access? Explain your answer.
(ii) what is the value of the offset into this block? Explain your answer.

(6 marks)

(c) If the machine described in (b) uses a direct-mapping strategy for caching, and the cache can hold up to 16K bytes of data (excluding tags), give the values of the following, explaining your answers:
(i) the size in bits of the *line no.* field
(ii) the size in bits of the *tag* field

(8 marks)

(d) What is the chief disadvantage of the direct-mapping approach?

(5 marks)

2.
(a) Give two advantages and two disadvantages of using microprogramming to implement a processor's control logic.

(4 marks)

(b) The diagram overleaf shows the microarchitecture of the hypothetical Mic-1 computer. Below is microcode that implements a part of the Mic-1's fetch-decode-execute cycle. Explain in detail what each line of code is doing.

```
START:      B=PC, LDMAR, RD
            A=PC, B=+1, ADD, C=PC, RD
            A=MBR, C=IR, JMP DECODE1
```

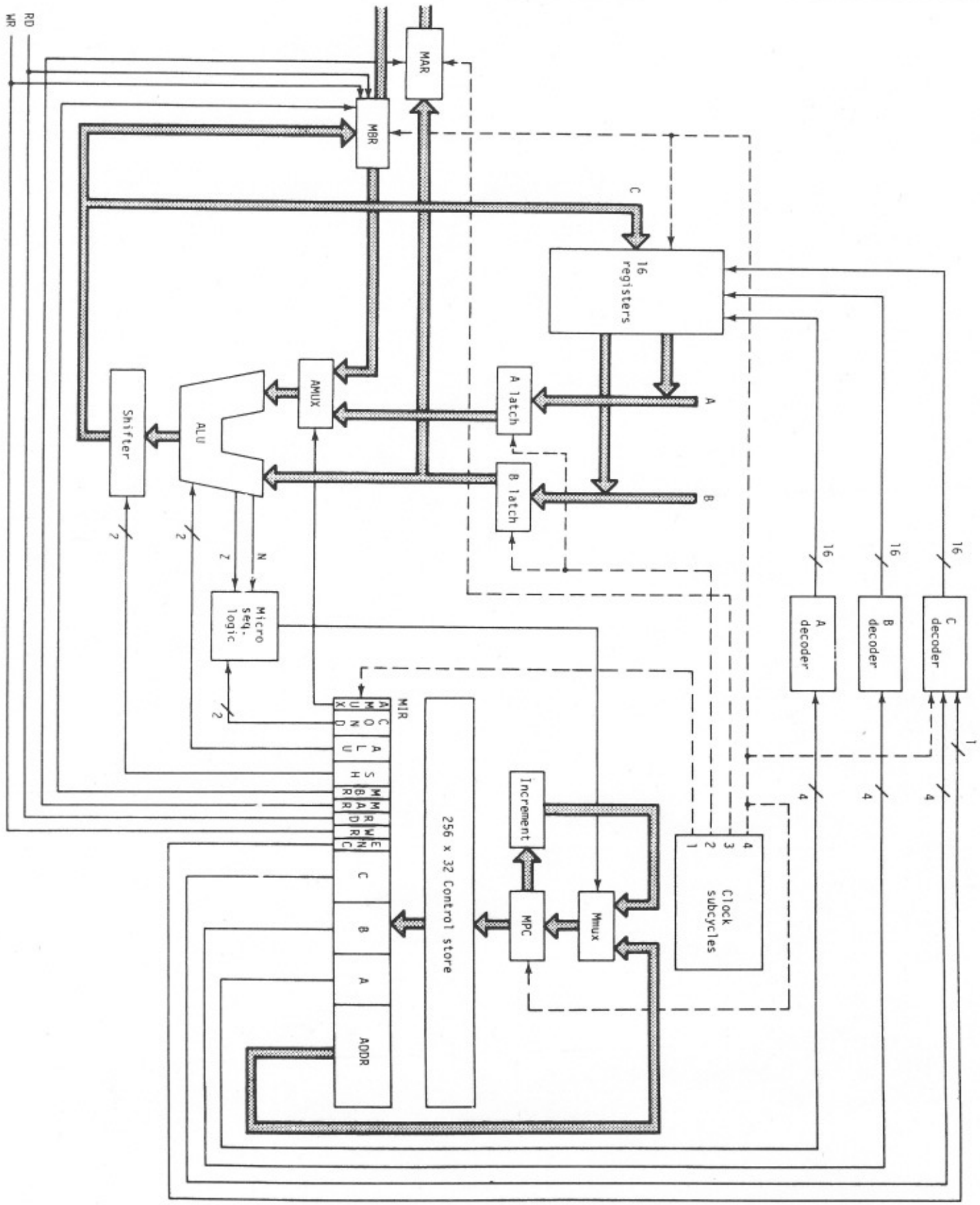
(12 marks)

(c) On the Mic-1, the INSP instruction contains in its lower 8 bits a value to be added to the stack pointer SP. This can be implemented in just two microinstructions as follows:

INSP: mask off the lower 8 bits of the instruction register IR, and transfer the result to temporary register RA
Add the contents of RA to SP, storing the result back in SP; go back to the start of the fetch cycle

Show how you might write these two microinstructions.

(9 marks)


RD
WR
MAR
MBR
C
16 registers
AMUX
ALU
Shifter
A latch
B latch
A
B
16
16
16
A decoder
B decoder
C decoder
Z
N
2
2
2
Micro seq. logic
MIR
MUX
COND
ALU
SH
MBR
MAR
WEN
C
B
A
ADDR
256 x 32 Control store
Increment
MPC
Mmux
Clock subcycles
1
2
3
4
4
4
4
1

3.
A hypothetical computer has a regular instruction set, with the typical form of instruction being, for example:

```
ADD A, B, RES
```

interpreted as RES := A + B.
The processor executes these instructions using a pipeline of six stages, namely:
fetch instruction; decode; fetch operand 1; fetch operand 2; execute; store result.
Consider the following instruction sequence:

```
ADD A, B, T1
ADD P, Q, T2
SUB T1, T2, T3
BLT T3, 0, OUT          // if T3 < 0 then GOTO OUT
ADD 1, NUM, NUM
BLT NUM, LIM, LOOP
```

(a) Draw a diagram showing the above instruction sequence as it moves through the pipeline. Describe any assumptions you have made regarding the branch instructions.

(7 marks)

(b) What is meant by a structural pipeline hazard? Identify two structural hazards in the sequence diagram you have drawn. Briefly describe a possible solution for handling these hazards.

(6 marks)

(c) What is meant by a data hazard? Identify two data hazards in your diagram. Briefly describe a possible remedy.

(6 marks)

(d) What is meant by a control hazard? Identify two control hazards in your diagram. Again, offer a way of dealing with these.

(6 marks)

4.
(a) What are the central aims of the RISC philosophy?
How effectively were these aims realised on the Berkeley RISC? Explain your answer.

(9 marks)

(b) A hypothetical computer executes machine instructions which contain opcodes of 8 bits, address fields of 24 bits, and register specification fields of 8 bits. All data words are 32 bits long. By considering how the computer would execute the code generated by an optimising compiler for the sequence of high-level statements

```
A := B - C
C := C - D
D := A + B
```

explain which of the following models of program execution is most appropriate to the RISC philosophy:
(i) memory-to-memory
(ii) register-to-register with program variables held in main memory
(iii) register-to-register with variables maintained in registers

(16 marks)

5.

(a) Why is the presence of cache memory important in shared memory multiprocessor systems?

(4 marks)

(b) Suppose the CPU in a uniprocessor computer wishes to alter the value of a variable held in cache. What two policies may be adopted for dealing with this? What are their relative advantages and disadvantages?

(6 marks)

(c) How effectively do the policies given in your answer to (b) apply to the following:
(i) local memory multiprocessor systems
(ii) shared memory multiprocessor systems

(7 marks)

(d) In the case of shared memory systems, describe two hardware solutions to the cache update problem.

(8 marks)