

PAPER CODE NO.
COMP203

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THE UNIVERSITY
of LIVERPOOL

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Degree of Bachelor of Arts : Year 2
Degree of Bachelor of Science : Year 2

COMPUTER LOGIC AND ARCHITECTURE

TIME ALLOWED :Two Hours

INSTRUCTIONS TO CANDIDATES

Answer **FOUR** Questions.

If you attempt to answer more than the required number of questions (in any section), the marks awarded for the excess questions will be discarded (starting with your lowest mark).



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- Q1.(a) Figure 1 illustrates the logic diagram of a Boolean function $F(A,B,C)$. State the Boolean equation describing this function. Expand this equation to develop the '**canonical sum of products**' form. Then construct the truth table for the function and develop the '**canonical product of sums**' form. (10 marks)

Figure 1: Logic Diagram

- (b) A combination logic circuit has four signal line inputs A,B,C and D, and a single output signal line Z. The list of minterms describing the output function Z set to logic 1 is as follows:

$$Z = m_2 + m_4 + m_5 + m_6 + m_8 + m_9 + m_{11} + m_{12} + m_{13} + m_{14} + m_{15}$$

Where m_i is minterm i with A as the least significant bit, e.g., $m_0 = \bar{A} \bar{B} \bar{C} \bar{D}$, $m_1 = A \bar{B} \bar{C} \bar{D}$, etc.

Use the Karnaugh map method to design a combinational circuit which will produce the function Z. Develop a '**minimum sum of products**' expression and show how this may be realised in **NAND** form.

Draw the corresponding **NAND** logic diagram.

- Q2.(a) What is multiplexer? (15 marks)

Give the block diagram and truth table of a 2 to 1 line multiplexer. Derive the describing logic equation and draw the corresponding logic diagram using **NAND** and **Inverter** gates.

(10 marks)

- (b) A parallel adder has two 8-bit inputs for the operands and an 8-bit output for the sum. '**Carry in**' and '**Carry out**' digits are also provided.

Give examples to explain how overflow or sign bit inversion may occur in the result from the adder with 2's complement operands. How is the corresponding result interpreted?

Show how a logic circuit may be described by a Boolean equation to produce an overflow flag which indicates that overflow has occurred. Draw a block diagram of the adder unit showing the connections of the overflow detection circuit.

(15 marks)



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- Q3.(a) Produce the state diagram of the clocked S-R flip flop. Then develop a table which illustrates the operation of the S-R flip flop describing what happens under various input conditions.

Explain how the clocked S-R flip flop may be modified to become a D type flip flop.

(10 marks)

- (b) The state diagram of a two bit synchronous binary counter is shown in Figure 2 where A and B are the logical names for the flip flop outputs. Construct a table which describes the 'present count' to 'next count' transitions.

Design this synchronous binary counter using J-K flip flops. Your design should show the excitation table and derivation of the flip flop excitation equations.

Draw the logic diagram of your resultant circuit.

(15 marks)

Figure 2: State Diagram

- Q4.(a) Explain the principles of operation of a tristate gate.

Explain how it is possible to share a data highway between a number of data sources and destinations. What is the mechanism of data transfer between a source and destination?

(10 marks)

- (b) Draw a block diagram of a register array consisting of four 12-bit registers having a single shared input/output data highway, and explain the corresponding structure. Explain in detail the processes of reading from and writing to particular register in the array. Do not include timing diagrams in your explanation.

(15 marks)

- Q5.(a) With reference to the 'generalised von Neumann machine', state the meaning and function of the following:

- (i) PC
- (ii) MAR
- (iii) MDR
- (iv) ALU
- (v) IR
- (vi) CC
- (vii) CPU bus
- (viii) DATA bus

(10 marks)



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- (b) Use the register transfer description to describe a list of statements for the **'generalised von Neumann machine'** which define an **'unconditional register - indirect branch'**, where the operational code occupies one memory location and register RO holds the address of the memory location which contains the branch address.

Explain in detail the function of each register transfer and assume it is necessary to use the ALU for PC increment operations.

Explain how your register transfer list describing the branch may be modified to become conditional on the status of a single condition status bit from the ALU. Assume status bit set (logic 1) will cause the branch to occur.

(15 marks)

- Q6.(a) Draw a block diagram to illustrate the processor - memory signal connection structure and explain the function of the various signals.

How many address signal lines does a 4 K byte static memory component have?

(10 marks)

- (b) A processor has a 16 bit address highway and other suitable signals for connection to memory .

What is the address space of a processor?

Draw a memory map of the address space partitioned into 8K byte blocks and explain in detail how suitable address decoding would effect the physical memory partitioning. Further explain in detail how an 8K byte block could be further partitioned into 2K byte sub blocks.

(15 marks)

