Master version -- 3.6.03

Model Solutions - Synthesis of Digital Architectures 2003

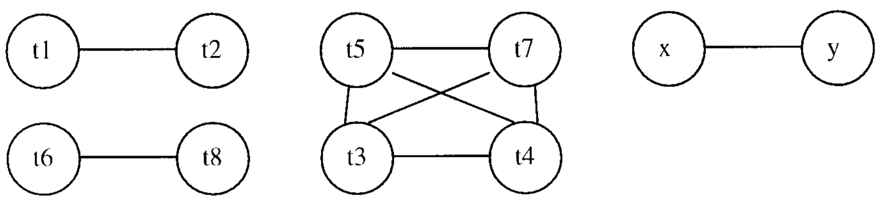
1.

a) [new computed example]

Variable	Produced	Consumed
t1	0	1
t2	0	1
t3	1	2,3
t4	1	2,3
t5	2	3
t6	3	4
t7	2	3
t8	3	4
x	4	Not Consumed (output)
y	4	Not Consumed (output)

[6]

b) [new computed example]



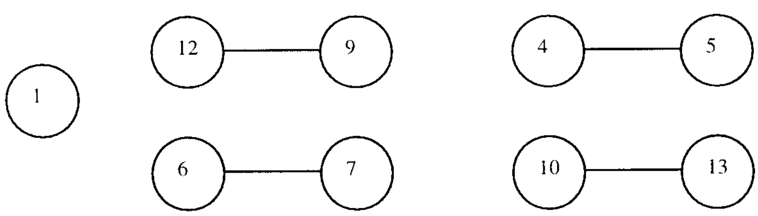
[5]

c) [bookwork]

Register conflict graphs in non-hierarchical CDFGs are interval graphs
[2]

d) [new computed example]

In the answer below, nodes are labelled by line number in the original code



[5]

e) [new computed example]

2 adders
[2]

2. [bookwork]

a)

"NP" stands for nondeterministic polynomial. NP consists of all the problems whose solution is checkable in polynomial time. [1]

NP-complete. This class consists of all problems in NP and at least as hard as any other problem in NP. [1]

NP-hard. This class consists of all problems at least as hard as an NP-complete problem. [1]

b)

This tells us that ILP is an NP-hard problem. [1]

c)

$$\forall v \in V, \sum_{t=ASAP_v}^{ALAP_v} x_{vt} = 1 \quad [4]$$

d)

$$\forall (v', v) \in E, \sum_{t=ASAP_{v'}}^{ALAP_{v'}} t x_{v't} + d_{v'} \leq \sum_{t=ASAP_v}^{ALAP_v} t x_{vt}$$

[4]

e)

$$\forall r \in R, \forall t \in \{0,1,\ldots,\lambda-1\}, \sum_{v \in V : T(v)=r} \sum_{t' \in \{ASAP_v,\ldots,ALAP_v\} \cap \{t-d_v+1,\ldots,t\}} x_{vt'} \leq a_r$$

[5]

f)

Let us label the CDFG sink node as z. Then the desired objective function is

$$\min : \sum_{t=ASAP_z}^{ALAP_z} t x_{zt}$$

[3]

3.

a) [bookwork]

Latency-constrained list scheduling [2]

b) [new computed example]

t=0: {y_2} (bound = 1)
t=1: {y_3} (bound = 1)
t=2: {y_5} (bound = 1)
t=3: {y_4} (could be y_6 or y_7 instead) (bound = 1)
t=4: {y_6, y_7} (answer will vary depending on t=3) (bound expanded to 2 due to zero slack)

ALAP times (used to obtain above answers):

y2: 1, y3: 2, y4: 4, y5: 3, y6: 4, y7: 4

[14]

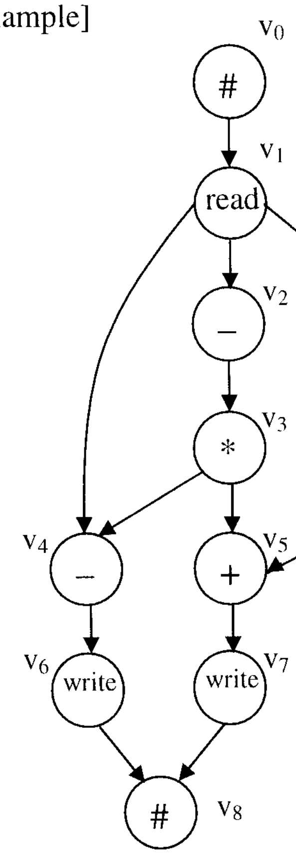
c) [new computed example]

Two adders are required

[4]

4.

a) [new computed example]



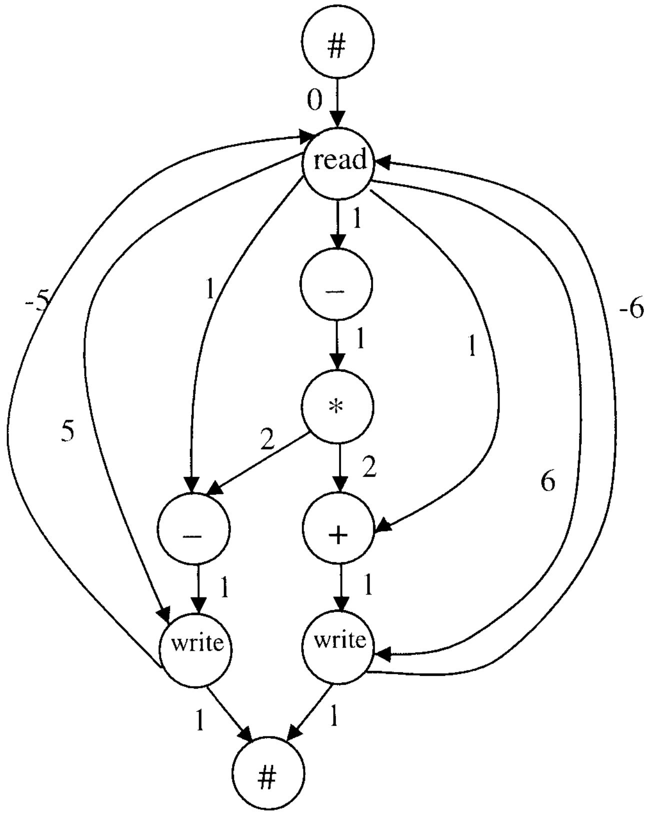
[4]

b) [new computed example]

Operation	ASAP	ALAP	Mobility
v_0	0	1	1
v_1	0	1	1
v_2	1	2	1
v_3	2	3	1
v_4	4	5	1
v_5	4	5	1
v_6	5	6	1
v_7	5	6	1
v_8	6	7	1

[6]

c) [new computed example / theoretical application]



[4]

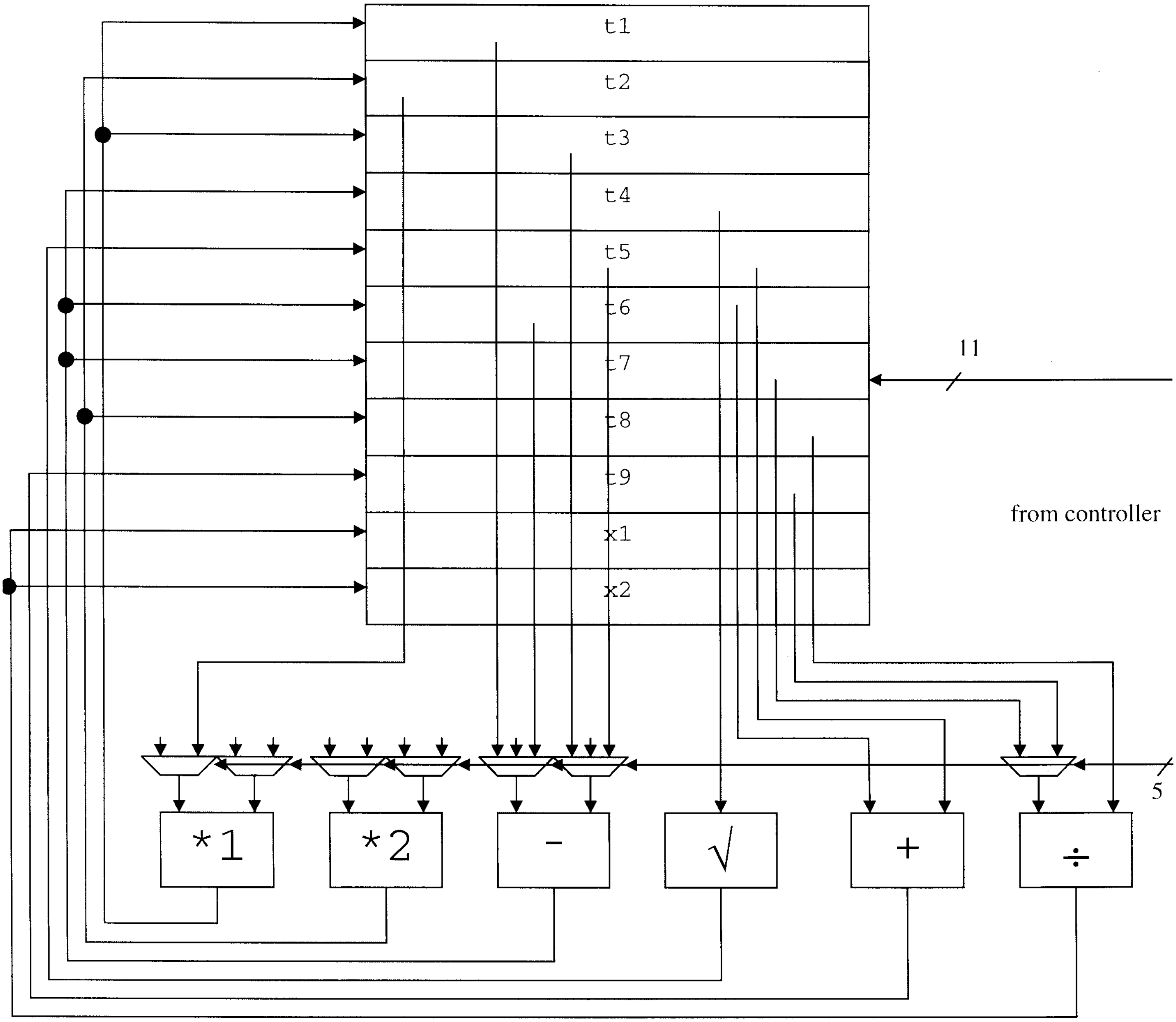
d) [new computed example / theoretical application]

Operation	ASAP	ALAP	Mobility
v_0	0	0	0
v_1	0	0	0
v_2	1	1	0
v_3	2	2	0
v_4	4	4	0
v_5	4	5	1
v_6	5	5	0
v_7	6	6	0
v_8	7	7	0

[6]

5.

a) [new computed example]



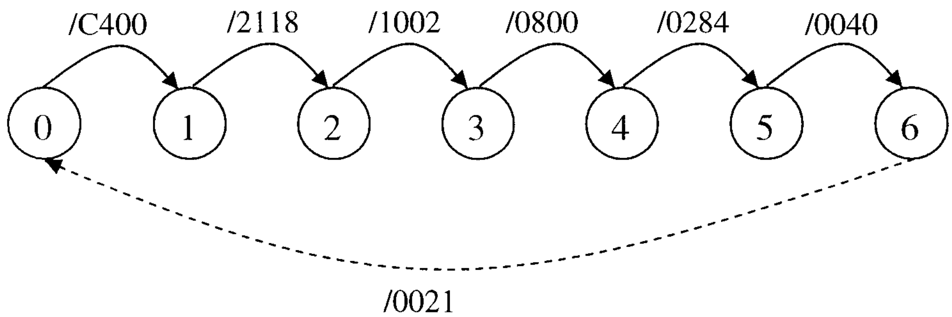
[7]

b) [new computed example]

16 control signals (11 enables, *1 select, *2 select, - select (two), div select) [2]

c) [new computed example]

Answer below is for MSB to LSB ordering: t1, t2, t3, t4, t5, t6, t7, t8, t9, x1, x2, *1 sel, *2 sel, - sel, div sel, and for all don't cares set to 0.

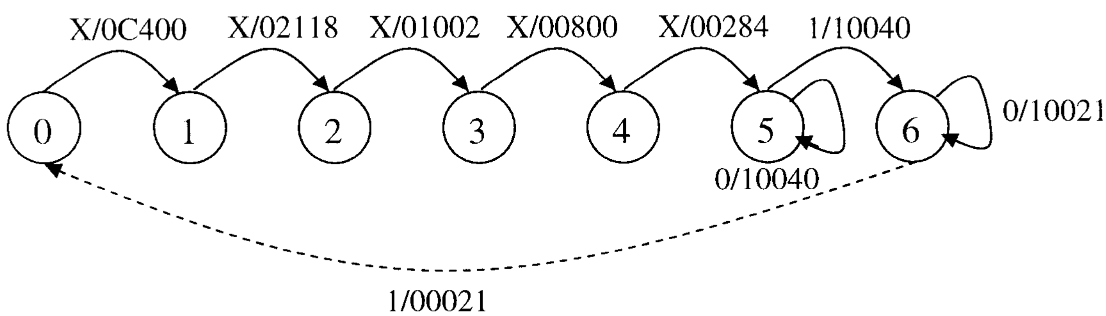


For other orderings or d/c settings, consult the table below (X=don't care).

Cycle	t1	t2	t3	t4	t5	t6	t7	t8	t9	x1	x2	*1	*2	–	÷
0	1	1	0	0	0	1	0	0	0	0	0	0	0	00	X
1	0	0	1	0	0	0	0	1	0	0	0	1	1	XX	X
2	0	0	0	1	0	0	0	0	0	0	0	X	X	01	X
3	0	0	0	0	1	0	0	0	0	0	0	X	X	XX	X
4	0	0	0	0	0	0	1	0	1	0	0	X	X	10	X
5	0	0	0	0	0	0	0	0	0	1	0	X	X	XX	0
6	0	0	0	0	0	0	0	0	0	0	1	X	X	XX	1

[6]

d) [new computed example / theoretical application]



[5]