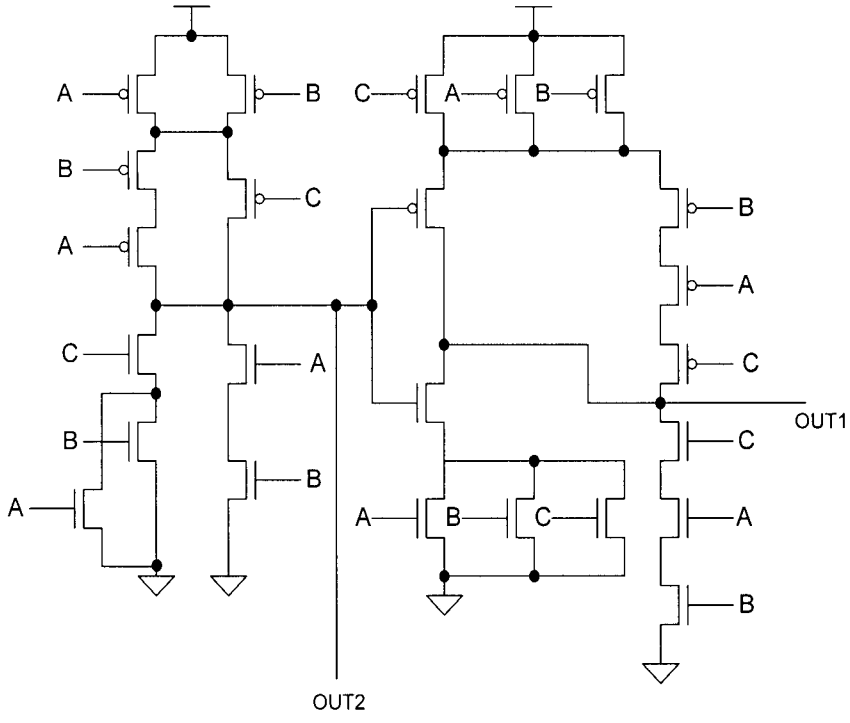
§4.20, ACJ, Ie 4.19

Solution to Question 1

a) This question tests student's ability to understand a full custom layout. This circuit is actually relatively hard to extract due to the large number of transistors. However, if student notice the symmetry in the circuit, it makes it a lot easier.

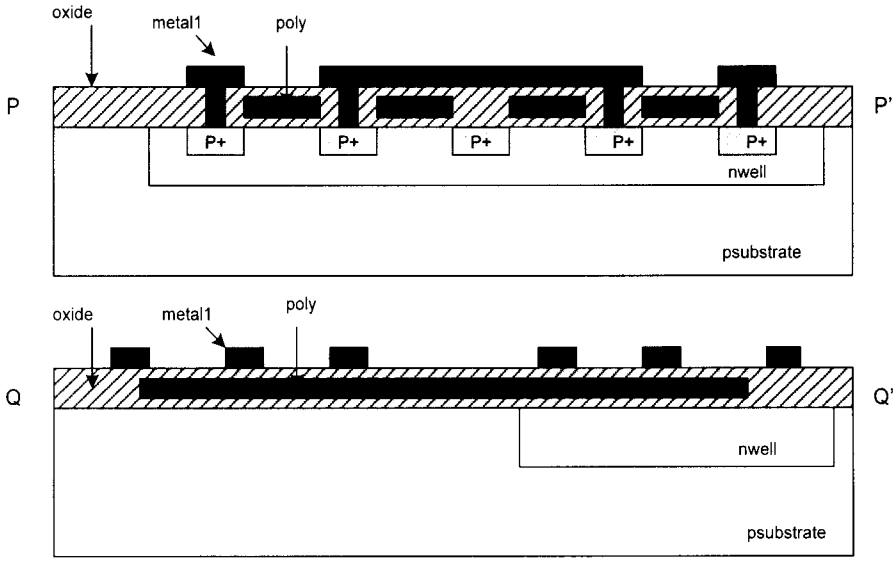


[10 marks]

b) This is a combinatorial full adder giving ~SUM and ~CARRY.

[2 marks]

c) This part of the question tests student's ability to relate the layout to the physical layout on the chip.



[8 marks]

Solution to Question 2

Each student was involved in a group design project to design a full-custom integrated circuit during the course. Since they were learning while doing the project, a number of mistakes were made. The four parts of this question are intended to test how much each student learned through this experience.

a) The following are some of the points expected to be discussed:
- Clarify specification of project right from the start, avoid chaning spec during design
- Adhere to top down design approach as much as possible. Model chip behaviourally to verify chip function
- Careful floorplanning early on for the entire chip
- For cell based designs, define cell boundary size and terminal location
- Use autoplace & route tools if possible
- Consider test right at the beginning of the design cycle. Design a good test vectore file, and use it for regressive verification and testing
- Maximize regularity and minimize different types of cell designs
- Pitch-match cells where possible
- Hierarchical design, both simulation and layout. Avoid excess use of hierarchy

I also expect more individual answers depending on student's chip design.

[4 marks]

b) This part depends on student's chip.

[4 marks]

c) This part of the question allows for recognition of individual understanding of, and contribution to, the project. In particular students are expected to learn from what they have done and suggest improvements to both the tools they used and the nature of project undertaken.

[8 marks]

d) I expect students to have at least a high level model of the chip to generate test vectors. I also expect them to consider test coverage and possibly some of design for test such as scan registers or even built-in self tests.

[4 marks]

Solution to Question 3

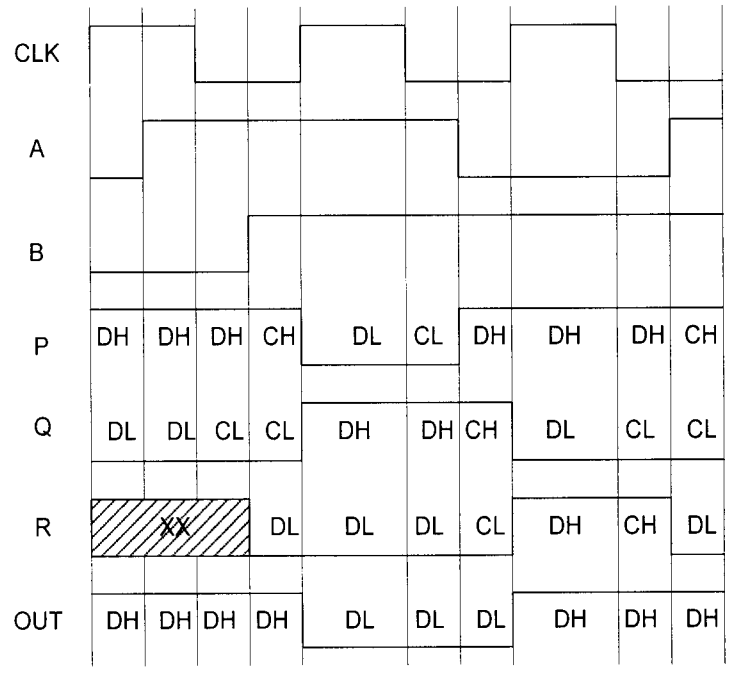
(a) Additional factors affecting decision:

Factors	Cell based or Gate array	FPGA
Available design time	1 Year or more	Short
Experience of members in the team	Moderate to good	Weak to moderate
How fixed is the specification?	Completely	Not completely
How sure is the volume of 1 million parts?	Very	Reasonable
Available development budget	High	Limited
How high is performance required?	V. High	Up to 100MHz clock
Sensitivity to part cost	High	Moderate

I will not even contemplate full custom chip. 50,000 gates is not a large enough chip to justify a full custom design. Either a gate array or cell based (with full mask set) could be justified. FPGA would however be my choice.

[5 marks]

(b)



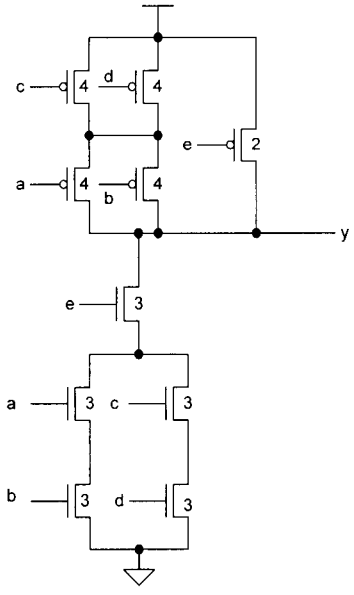
[12 marks]

(c) This is a positive edge triggered NAND gate.

[3 marks]

Solution to Question 4

(a) The circuit could be:



[4 marks]

(b) See relative transistor sizing in (a)

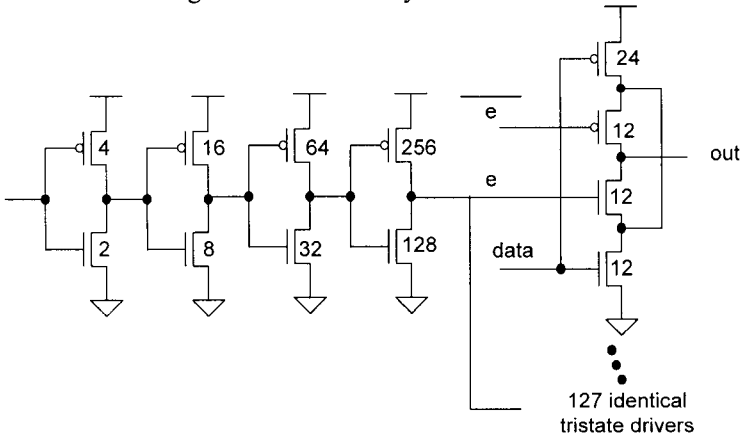
[3 marks]

(c) Layout depends on student's design. Full marks for topologically correct design with sensible layout. Deduce marks for poor layout of transistors that potentially takes lots of room.

[5 marks]

(d) The theory of Logic Effort is developed by Ivan Sutherland and is taught to our students as ways of sizing transistors.

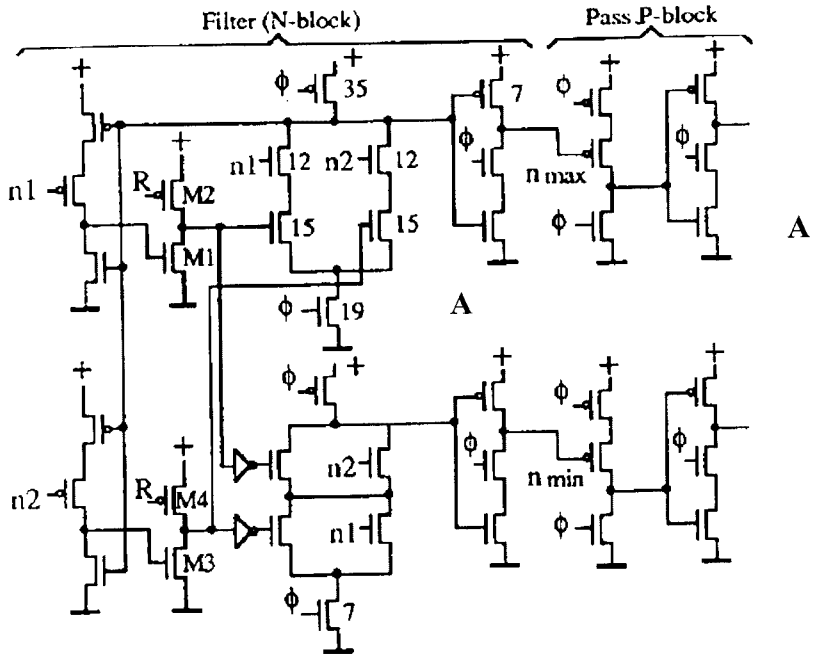
- Electrical Effort F = (no of drivers) X (input load to enable signal) / input capacitance
  = 128 X 12/6 = 256.
- Optimal no of stages N = $\log_4 F$ = 4.
- Each stage increase in size by 4th root of 256 = 4. Hence the design is:



[8 marks]

Solution to Question 5

This question tests student ability to design a relatively complex transistor level circuit from specification. A possible solution using single phase clocking (only one clock signal):



A

A

A

H

L

The solution is taken from M. Afghahi, "A 512 16-b Bit-Serial Sorter Chip", IEEE JSSC, Vol 26, No 1 1991. The P blocks are inserted to allow domino circuit where N and P blocks must alternate. Therefore the double P-block inverters is really an all pass circuit.

[8 marks]

Solution to Question 6

(a) (i)

Pass transistor logic relies on passing logic level as well as gate control.

Advantages: More efficient in transistor count (especially for XOR functions)
Lower power

Disadvantages: Difficult to simulate with logic simulators
Charge sharing problems
No restoring logic, therefore pass either weak '1' or weak '0'

[3 marks]

(ii) Dynamic logic (as oppose to static logic).

Advantages: Generally smaller (only need n-tree or p-tree)
Can be very fast

Disadvantages: Needs to distribute clock – possible skew problem
Only work with part of a clock cycle, tighter timing constraints

[3 marks]

(b)

P	Q	R	Y	Z
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

[12 marks]

(c) This is obviously a full adder circuit Y= SUM, Z= carry.

[2 marks]