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IMPERIAL COLLEGE LONDON

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DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2004

MSc and EEE/ISE PART IV: MEng and ACGI

INTRODUCTION TO DIGITAL INTEGRATED CIRCUIT DESIGN

Friday, 7 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P.Y.K. Cheung
Second Marker(s) : T.J.W. Clarke

Information for Invigilators:

Students may bring any written or printed aids into the examination.

Information for Candidates:

Students may need red, green, blue, yellow and black coloured pens.

1. a) Figure 1 (See the colour supplementary sheet) shows the layout of an n-well CMOS circuit with two inputs `A` and `B`, and three outputs `OUT1`, `OUT2` and `OUT3`. Extract and draw the transistor-level schematic diagram.

[10 marks]

b) Write down the Boolean equations that describe the function of this circuit.

[2 marks]

c) Draw the vertical cross sections of the chip along the lines `PP'` and `QQ'`. Label your diagram indicating the n-well region and the different types and levels of doping (e.g. p^-, n^+ etc).

[8 marks]

2. a) Figure 2 shows a dynamic differential flip-flop circuit. Explain how this circuit works.

[5 marks]

b) Design a symbolic layout for this circuit for use as a standard cell. Justify any specific decisions made in your layout design.

[15 marks]

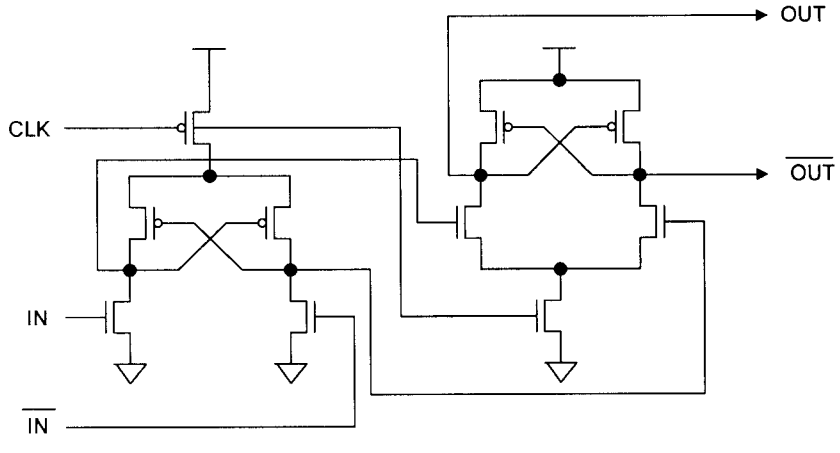


Figure 2

3. a) Figure 3.1 shows a double-bit binary adder circuit, which takes two 2-bit numbers *A1:A0* and *B1:B0* and a carry input C_{-1}, and produces a 2-bit sum *S1:S0* and a carry output C_1. Derive a Boolean expression for the carry output C_1 of the double-bit binary adder shown *in* Figure 3.1 in terms of its inputs A_0, A_1, B_0, B_1 and the input carry C_{-1}.

Hence, or otherwise, show that the carry output of a double-bit adder C_{i+1} is given by

$$C_{i+1} = G^*_{i+1} + P^*_{i+1} \bullet C_{i-1}$$

where G^*_{i+1} and P^*_{i+1} are respectively the double-bit generate and propagate signals given by:

$$G^*_{i+1} = G^*_{i+1} + P_{i+1} \bullet G_i \quad \text{and} \quad P^*_{i+1} = P_{i+1} \bullet P_i .$$

[6 marks]

b) Figure 3.2 shows the implementation of a circuit to produce the signals G_i and G^*_{i+1}. This circuit uses a variation of Domino Logic called Multiple-Output Domino Logic (MODL). Based on the principle of Domino Logic, explain how this circuit evaluates G_i and G^*_{i+1}.

[6 marks]

c) Design a circuit using the same MODL technique to produce the signals P_i and P^*_{i+1}.

[8 marks]

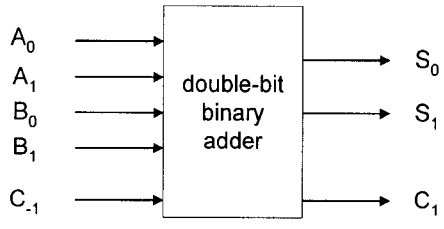


Figure 3.1

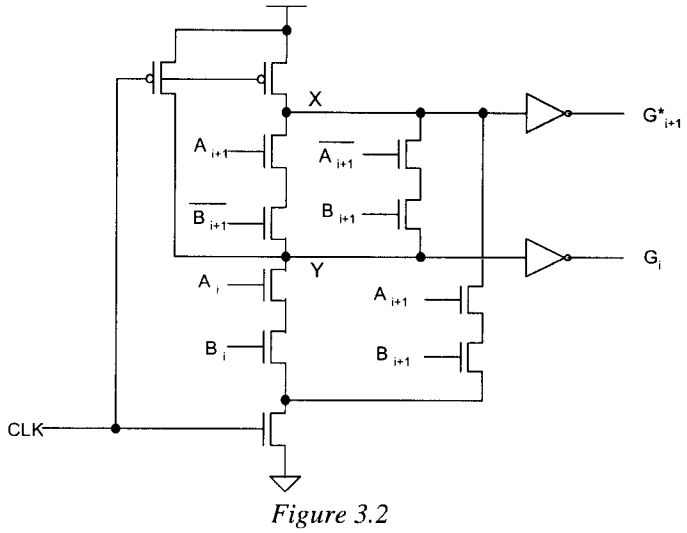


Figure 3.2

4. a) Using the method of logical effort, design the size of all the transistors in the circuit shown in Figure 4.1 to obtain minimum delay. You may assume that the logic effort and the parasitic delays of the gates are as shown. State any other assumptions used. Estimate the delay from A to Z.

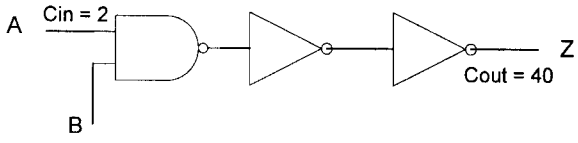
[8 marks]

b) Assuming that the logical effort and parasitic delay for rising and falling inputs are different as shown in Figure 4.2, calculate the rise and fall delays at the output.

[6 marks]

c) Figure 4.3 shows a circuit driving the selection inputs s and $\bar{s}$ of 64 identical tristate buffer circuits. The sizes of all the stages are also shown. Using the method of logic effort, or otherwise, calculate the delay d_1 and d_2 using logical effort and parasitic delay values in Figure 4.1.

[6 marks]



Gate	Logical Effort	Parasitic Delay
INV	1	1
2-NAND	4/3	2

Figure 4.1

Gate	Logical Effort		Parasitic Delay	
	Rising g_r	*Falling* g_f	*Rising* p_r	*Falling* p_f
INV	6/5	4/5	6/5	4/5
2-NAND	24/15	16/15	12/5	8/5

Figure 4.2

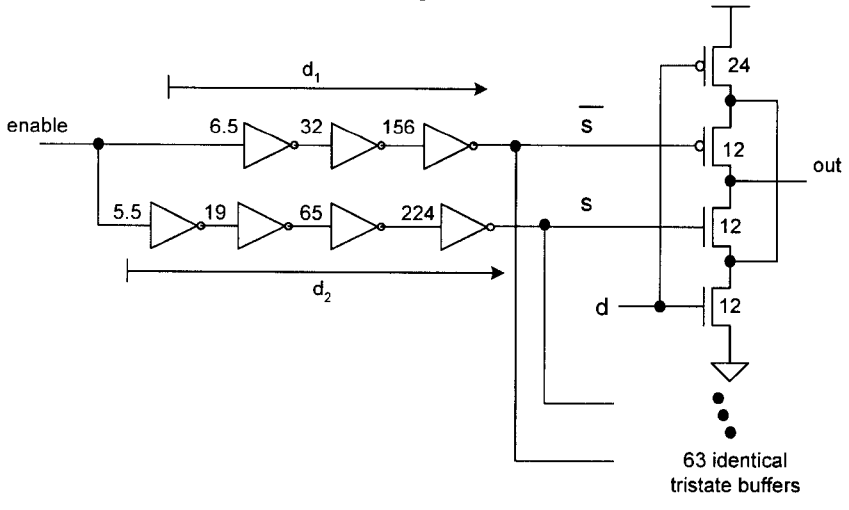


Figure 4.3

5. a) Figure 5.1 shows the transistor-level schematic diagram of a latch circuit. Given that the timing diagram for the input signals CLK and IN is as shown in Figure 5.2, draw the timing diagram for the signals at X, Y, Z and D. Label your timing diagram indicating the various states of the signal nodes as:

driven low (DL) - a path to ground exists,
driven high (DH) - a path to VDD exists,
charged low (CL) - high impedance with no stored charge at ground, and
charged high (CH) - high impedance with stored charge at VDD.

You may assume that initially both Y and Z are charged high.

[8 marks]

b) By considering the high and low phases of the clock signal, explain the function of this circuit.

[6 marks]

c) What is the effect of adding the shaded circuit to the latch as shown in Figure 5.3?

[6 marks]

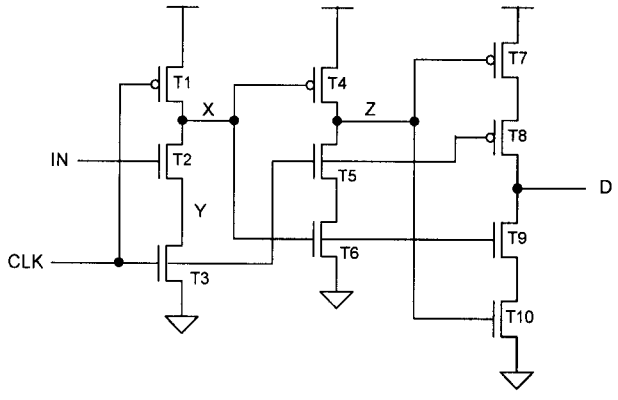


Figure 5.1

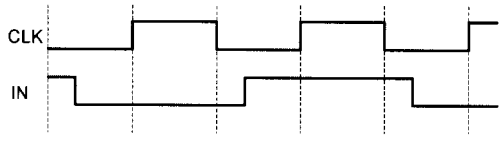


Figure 5.2

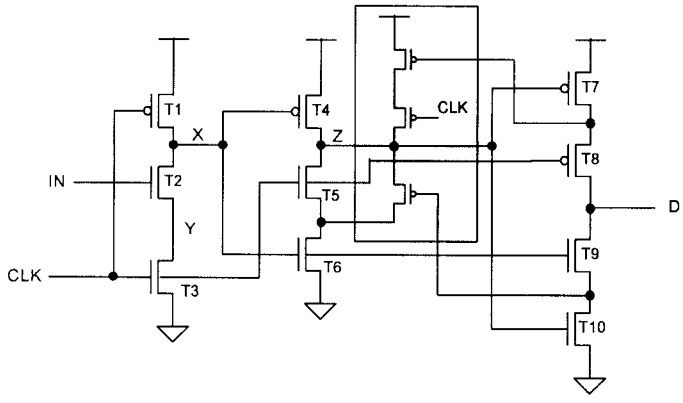


Figure 5.3

6. a) Explain briefly advantages and limitations of the "stuck-at" model used in digital test.

[4 marks]

b) Figure 6.1 shows the layout of a two-input gate with a manufacturing defect manifested as a break in the signal track as shown. Explain why this fault cannot be represented as a stuck-at fault. Derive the faulty behaviour of this circuit.

[6 marks]

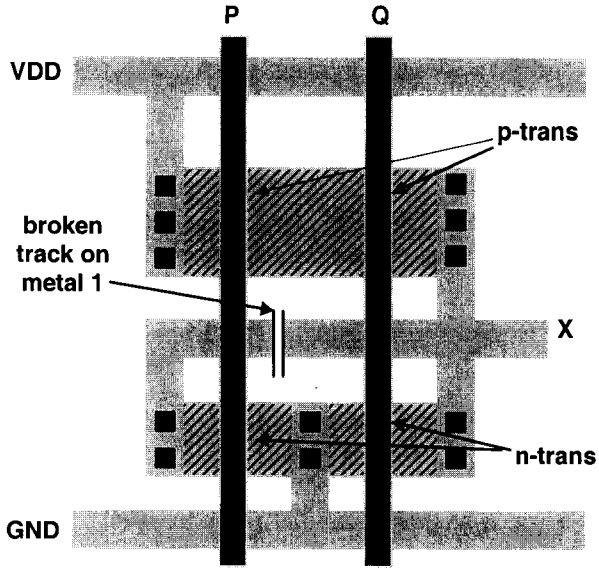


Figure 6.1

c) By applying the principle of path sensitisation to the circuit shown in Figure 6.2, generate the test vectors for detecting: i) a *stuck-at-0* fault at node *F*, ii) a *stuck-at-1* fault at node *G*.

If `GateP` is replaced by a two-input AND gate, why do these two faults become undetectable?

[10 marks]

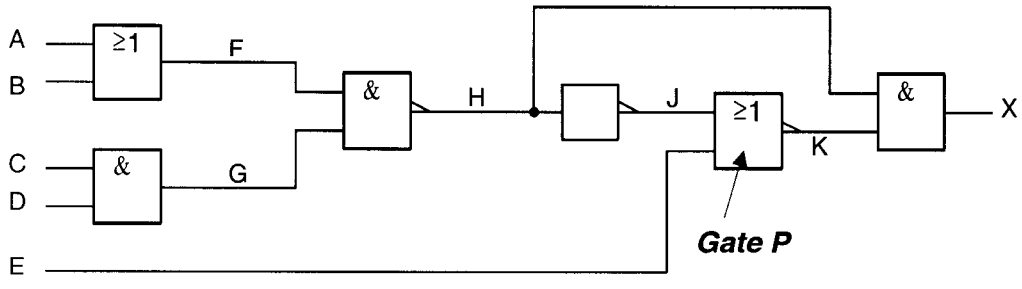


Figure 6.2

Colour Supplementary Sheet

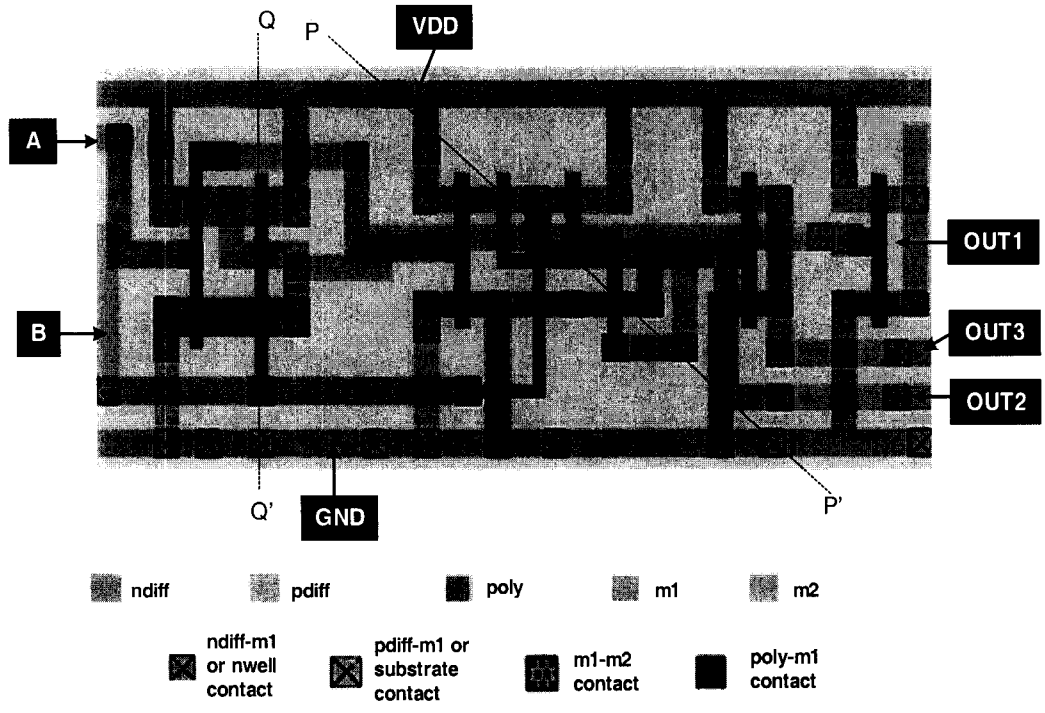


Figure 1 Layout of a full-custom cell for Question 1

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IMPERIAL COLLEGE OF SCIENCE TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
M.Eng. and A.C.G.I. EXAMINATIONS 2004

PART IV

INTRODUCTION TO DIGITAL IC DESIGN

SOLUTIONS

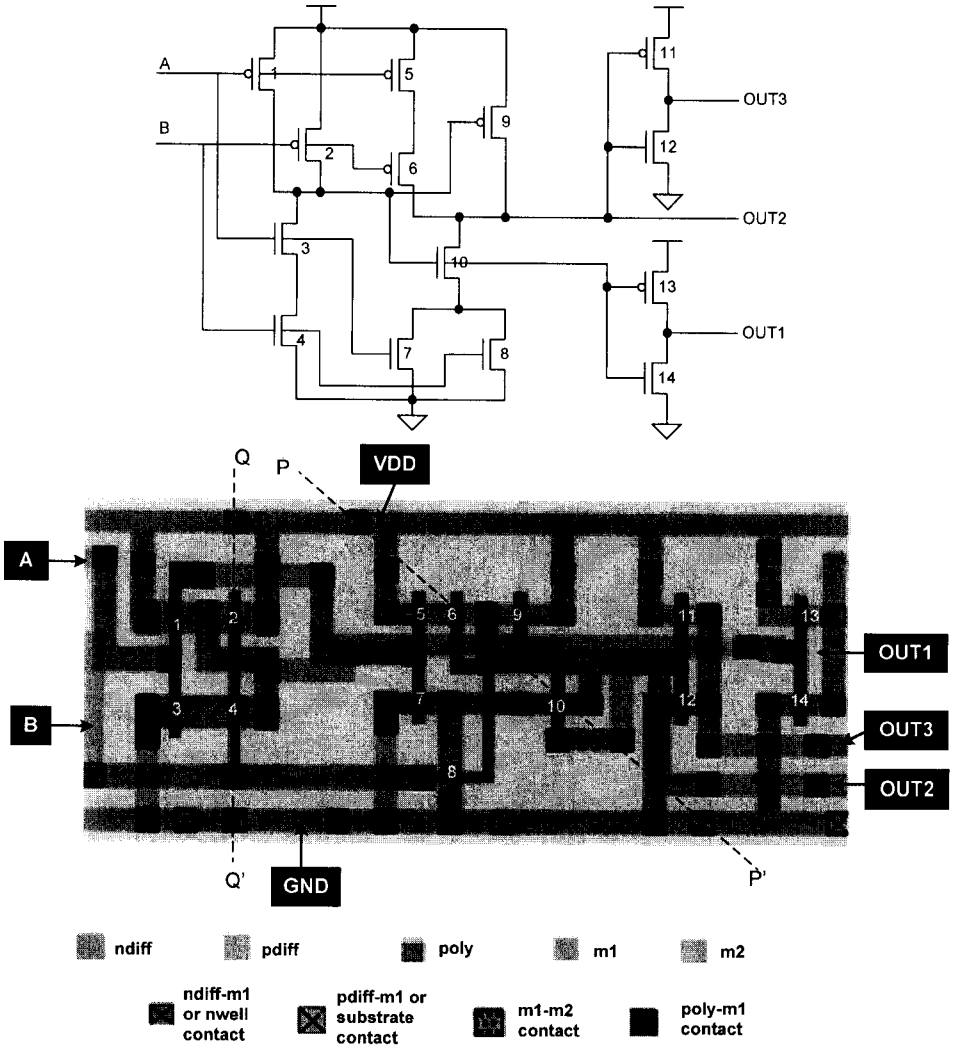
This is an open-book examination.

You may need red, green, blue, yellow and black coloured pens.

First Marker: *Peter Cheung*
Second Marker: *Thomas Clarke*

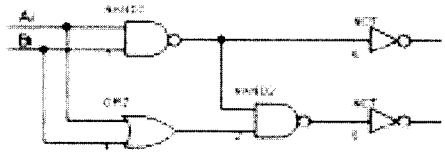
Solution to Question 1

a) This question tests student's ability to understand a full custom layout.



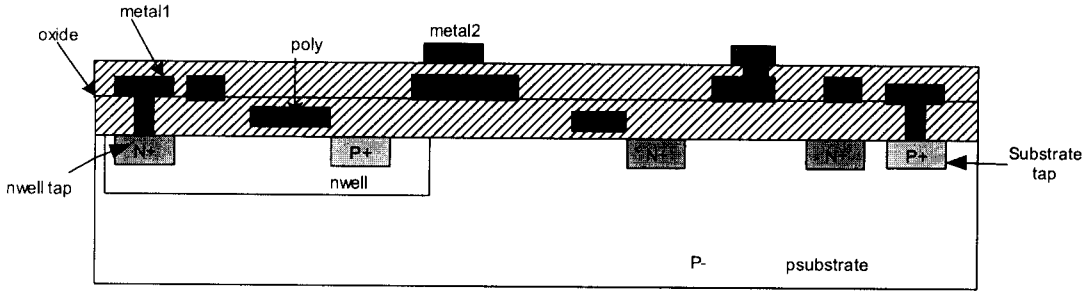
[10 marks]

b) $OUT1 = A \bullet B, \quad OUT2 = \overline{A} \bullet \overline{B} + A \bullet B, \quad OUT3 = \overline{OUT2}$



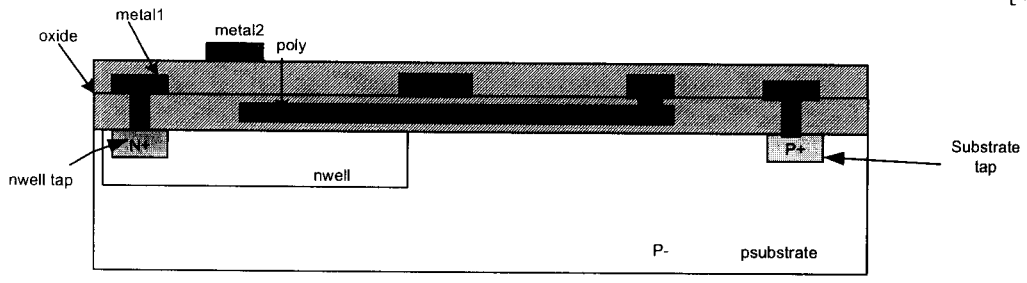
[2 marks]

c) This part of the question tests student's ability to relate the layout to the physical process and different layers on the chip.



P - P'

[4]



Q - Q'

[4]

[8 marks]

Solution to Question 2

(a)

This is a master-slave type of flip-flop based on differential latch circuits. When CLK is high, the first stage is in storage state. As soon as the clock goes from high to low, the first stage switches to reflect the values on the inputs and the second stage is in storage state.

[5 marks]

(b)

The layout depends on the student's design. However, I would expect the student to follow these rules because the cell is used in a standard cell environment:

1) It should have a fixed defined height.
2) The control signals CLK should run from top to bottom.
3) The IN/OUT signals should also run from top to bottom for easy channel routing.

[15 marks]

Solution to Question 3

a) $C_0 = G_0 + P_0 \bullet C_{-1}$

$C_1 = G_1 + P_1 \bullet C_0 = G_1 + P_1 (G_0 + P_0 \bullet C_{-1})$

Therefore $C_1 = \underbrace{(G_1 + P_1 \bullet G_0)}_{G_1^*} + \underbrace{(P_1 \bullet P_0)}_{P_1^*} C_{-1}$

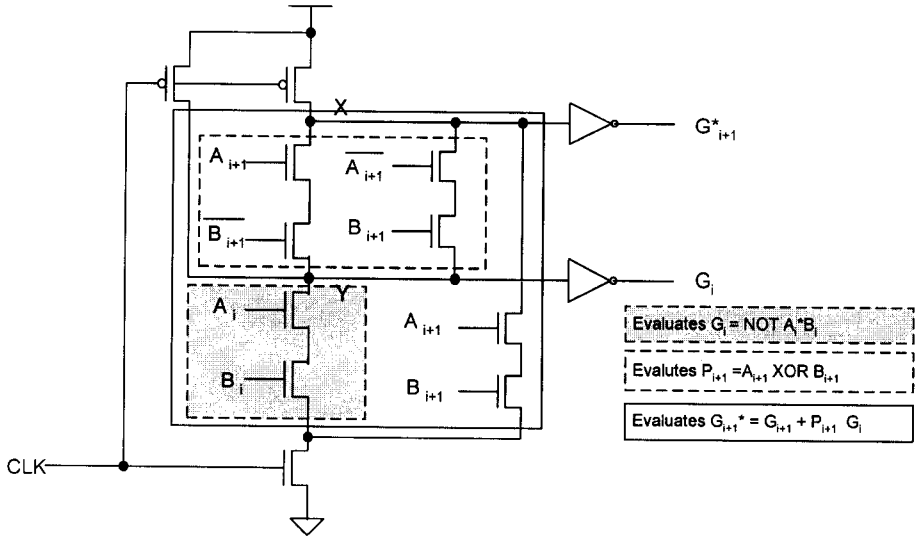
where $G_1 = A_1 \bullet B_1$; $G_0 = A_0 \bullet B0$; $P_1 = A_1 \oplus B_1$; $P_0 = A_0 \oplus B_0$.

Hence generalise to:

$C_{i+1} = G_{i+1}^* + P_{i+1}^* \bullet C_{i-1}$, where $G_{i+1}^* = G_{i+1} + P_{i+1} \bullet G_i$ and $P_{i+1}^* = P_{i+1} \bullet P_i$

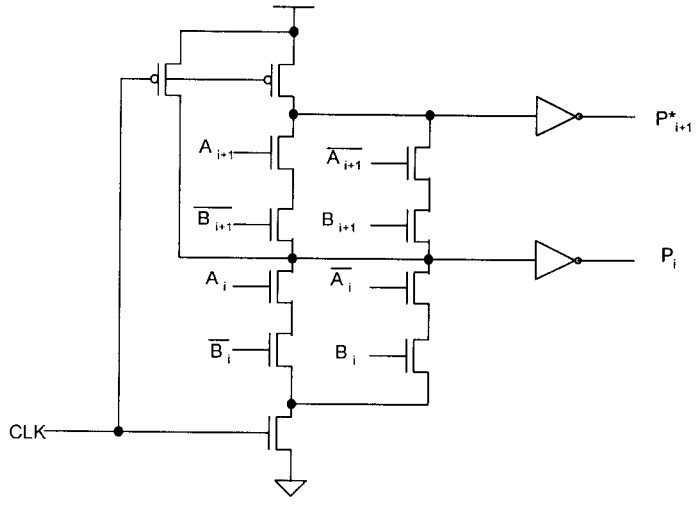
[6 marks]

(b) X and Y are precharged nodes. The remaining circuit works according to:



[6 marks]

(c)



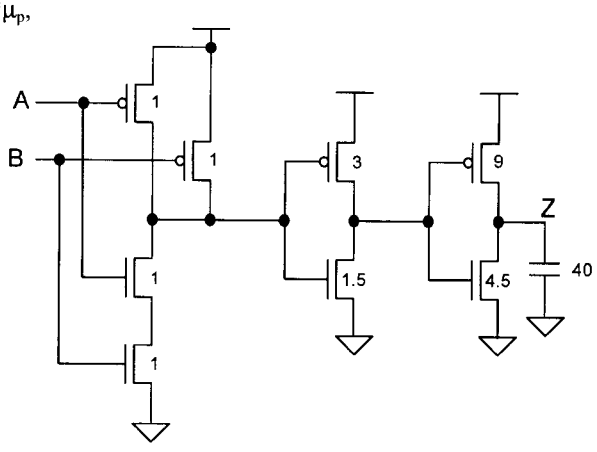
[8 marks]

Solution to Question 4

(a) Logic effort is a method to estimate delay in CMOS circuits "on the back of an envelop". It also provides a quick way of sizing transistors for optimal speed. The method was invented by Ivan Sutherland and is described in the book "Logical Effort" by Sutherland, Sproull and Harris.

G = 4/3 and H = 20, therefore F = 80/3. Best speed achieved when each stage effort
$F = (80/3)^{1/3} \approx 3$.

Assuming $\mu_n = 2*\mu_p$,



$g_1 = 4/3$; $g_2 = g_3 = 1$; $h_1 = 4.5/2$; $h_2 = 13.5/4.5$; $h_3 = 40/13.5$; $p_1 = 2$; $p_2 = p_3 = 1$

$\text{Delay} = (g_1h_1 + p_1) + (g_2h_2 + p_2) + (g_3h_3 + p_3)$
$= (4/3) \times (4.5/2) + 2 + (13.5/4.5) + 1 + (40/13.5) + 1$
≈ 13 (unit delays)

[8 marks]

(b)

$\text{Delay}_r = (g_{r1}h_1 + p_{r1}) + (g_{f2}h_2 + p_{f2}) + (g_{r3}h_3 + p_{r3})$
$= (24/15) \times (4.5/2) + 12/5 + (4/5) \times (13.5/4.5) + 4/5 + (6/5) \times (40/13.5) + 6/5$
$= 13.96$

$\text{Delay}_f = (g_{f1}h_1 + p_{f1}) + (g_{r2}h_2 + p_{r2}) + (g_{f3}h_3 + p_{f3})$
$= (16/15) \times (4.5/2) + 8/5 + (6/5) \times (13.5/4.5) + 6/5 + (4/5) \times (40/13.5) + 4/5$
$= 11.97$

[6 marks]

(c) F = no of drivers x i/p load / Cin

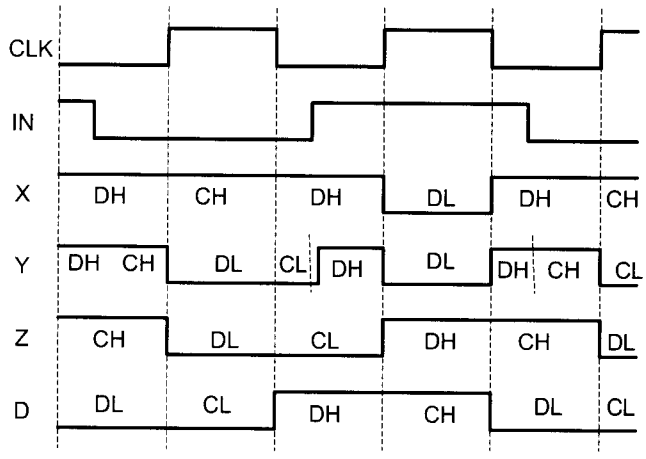
For D1, F = 64 x 12 /6.5 = 118.2
$f = F^{1/3} = 4.9$, D1 = 3 x f + 3 x para. Delay = 17.7 τ

For D2, F = 64 x 12/5.5 = 139.6
$f = F^{1/4} = 3.44$, D2 = 4 x 3.44 + 4 x 1 = 17.8 τ

[6 marks]

Solution to Question 5

a) This circuit is taken from "New Single-Clock CMOS Latches and Flipflops with Improved Speed and Power Savings" by Yuan and Svensson, IEEE JSSC vol 32, no 1, Jan 97.



[8 marks]

b) The circuit can be viewed as three stages: 1st stage has CLK driving p- and n-transistor (known as PN). This is a precharge circuit. 2nd stage has CLK driving a n-transistor only (known as SN). Together with 1st stage, it evaluates IN to yield Z when CLK goes high. The 3rd stage is a full latch (FL(P)) similar to the C^2MOS circuit except that we only use CLK and not CLK_bar. Instead, the precharge node X is used in place of CLK_bar. This is clever because when CLK is low (precharging), X is always high. Therefore during evaluation phase (CLK='1'), the 3rd stage is in storage state. During precharge phase (CLK='0'), the 3rd stage is sampling the data input at Z since it works just like an inverter. Therefore this is working as a single-phase clocking latch.

[6 marks]

c) Z is a dynamic node such that during precharge phase (CLK='0'), it always is a charge node. The circuit in the shade box provide feedback to turn Z into a static node. Note that the output of 3rd stage remains a dynamic node – it becomes tristate when CLK is high. This is actually an advantage when this is driving a bus. (See Yuan's paper.)

[6 marks]

Solution to Question 6

a)

Advantages:
- Can represent many physical faults such as shorts to Vdd & ground
- Easy to handle and simulate
- Many other fault can be mapped to stuck-at faults

Disadvantages:
- Cannot represent some bridging faults and some open-faults
- Cannot handle transient and delay faults

[4 marks]

b)
The broken track fault cannot be represented by stuck-at model because it exhibits the behaviour of a sequential circuit. The faulty behaviour is:

$$X = \overline{(P + \overline{Q})} + (P \bullet \overline{Q} \bullet X_{previous})$$

[6 marks]

c)

Test vector to test Stuck-at-0 at node F:
{ABCDEX} = {1x1100}

Test vector to test stuck-at-1 at node G:
{ABCDEX} = {1x0x01}

If Gate P is replaced with a two-input AND gate, the reconvergent fan-out will mask the fault effect and therefore the two faults become undetectable.

[10 marks]