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IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2007

MSc and EEE PART IV: MEng and ACGI

Corrected Copy

HIGH PERFORMANCE ANALOGUE ELECTRONICS

Thursday, 10 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : E. Rodriguez-Villegas
Second Marker(s) : D.G. Haigh

1. (a) Figure 1.1 shows the block diagram of a superheterodyne receiver. Describe briefly the function of the different filters within the receiver.

[4]

(b) Explain the reason to downconvert the RF signal to an intermediate frequency band instead of directly using just an antenna and a bandpass filter.

[4]

(c) Explain the function of the mixer in the superheterodyne receiver.

[4]

(d) What would be the advantages and disadvantages of mixing your RF signal with a square wave instead of a purely sinusoidal signal?

[4]

(e) In the mixer in Figure 1.2, explain the functionality of the inductor and capacitor.

[4]

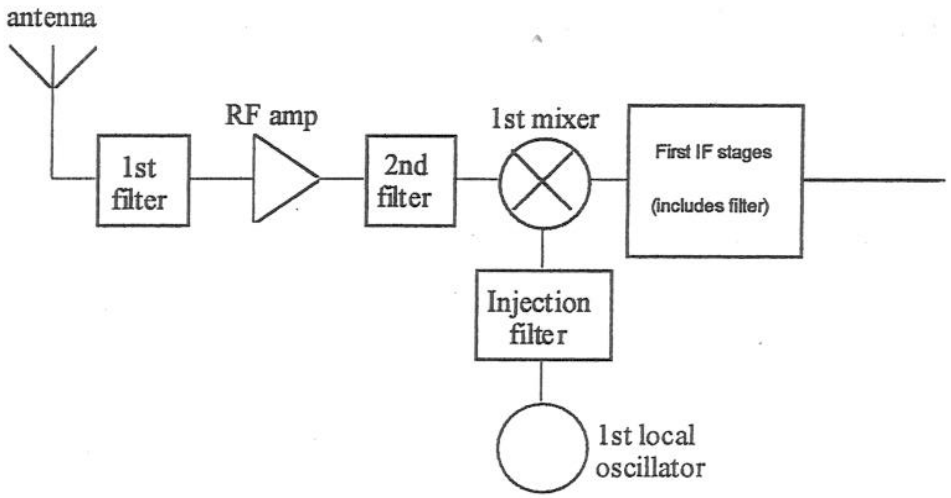

Figure 1.1

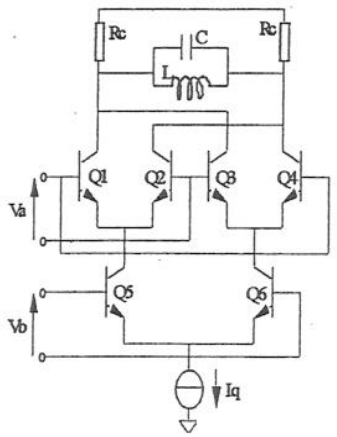

Figure 1.2

2. (a) In a cascade of systems with gains higher than one, what is the most critical one in terms of noise? Explain the reason with equations.

[10]

(b) Figure 2.1 shows the schematic and equivalent symbol of a FGMOS transistor. Ignoring parasitic effects the voltage at the floating gate, V_{FG}, is given by:

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i$$

where C_T is the total capacitance seen by the floating gate, C_i are the capacitive inputs and V_i are the voltages at the effective inputs. Find expressions for the transconductance of the FGMOS transistor referred to the effective input V_1, in the different operating regions.

[4]

(c) Draw a small signal model for noise in this device, giving expressions for the power spectral densities of the different noise sources.

[3]

(d) Find an expression for the equivalent noise at the input V_1 and at the output (drain) as a function of the equivalent power spectral density of noise in the MOS transistor M1 and the capacitive ratios. From those expressions, is it advantageous or not from the point of view of noise to use FGMOS instead of MOS devices within a design?

[3]

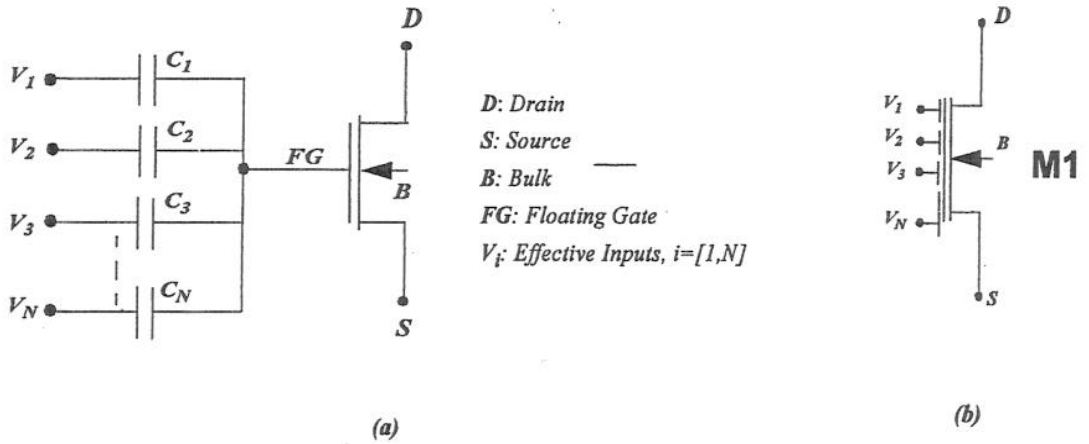

Figure 2.1

3. (a) For the MOS transistor in Figure 3 (a), find an expression for the minimum V_{out} voltage required to keep the device operating in the strong inversion saturation region for a maximum input signal $V_{in(max)}$ as a function of the threshold voltage.

[2]

(b) For the circuit in Figure 3(b), what is the minimum V_{DD} value required for it to operate correctly as a function of the threshold voltage? (Note: The transistors should not leave the strong inversion region)

[2]

(c) For the same circuit, in which operating region would you bias transistor M1 to minimize the power requirement?

[2]

(d) Find an expression for the output current I_{out} in Figure 3(c) (assuming the transistors are biased in the region you choose in (c)). What is the function of the amplifier?

[5]

(e) What is the advantage of using configuration (c) instead of (d)?

[5]

(f) Draw an integrator built with the topology in Figure 3(c) (Note: Do not forget that the first requirement for a circuit to work is to make sure all the devices are biased properly, so you need to have current paths in all the nodes!!)

[4]

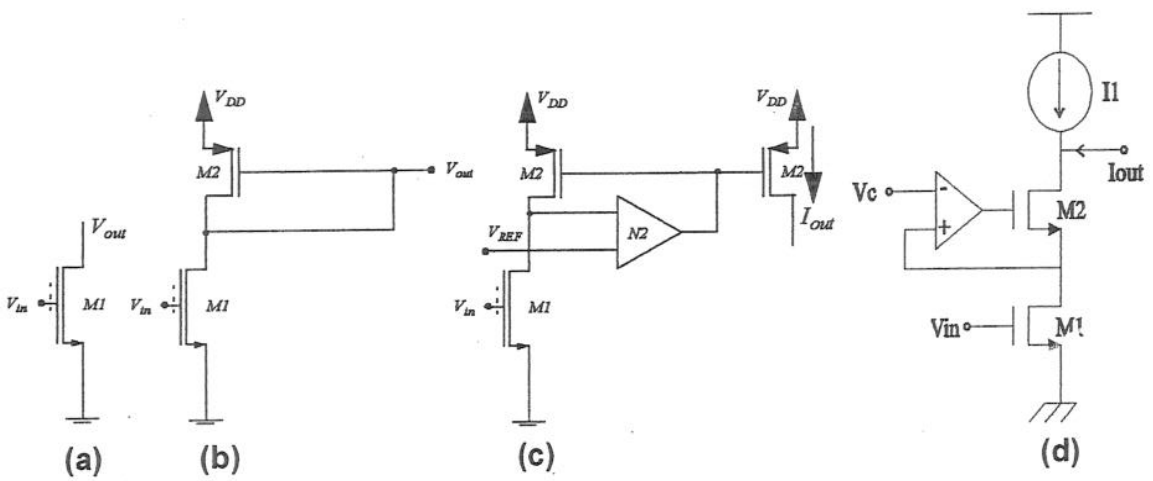

Figure 3

4. (a) For the circuit in Figure 4, find the transfer functions. What kind of system they correspond to?

[4]

(b) Draw approximate Bode plots for the transfer functions obtained in (a) and give expressions for two characteristic parameters in them.

[4]

(c) What are the main reasons to use transconductors as building blocks instead of amplifiers?

[4]

(d) Propose a transconductor topology to implement the previous system with a maximum of five transistors (other components are allowed). Why did you choose that specific topology? What would be the advantages and disadvantages of that topology? How would you improve it if you could double the number of transistors?

[4]

(e) Give an approximate expression for the transconductance of the topology you first chose in (d), explaining the assumptions you made to approximate it that way. If all the transconductor blocks are equally designed, the sizes of the transistors are fixed and the maximum bias current is such that the maximum transconductance is g_{max}, what would be the minimum value of the integrating capacitance you would need to realize a time constant of τ.

[4]

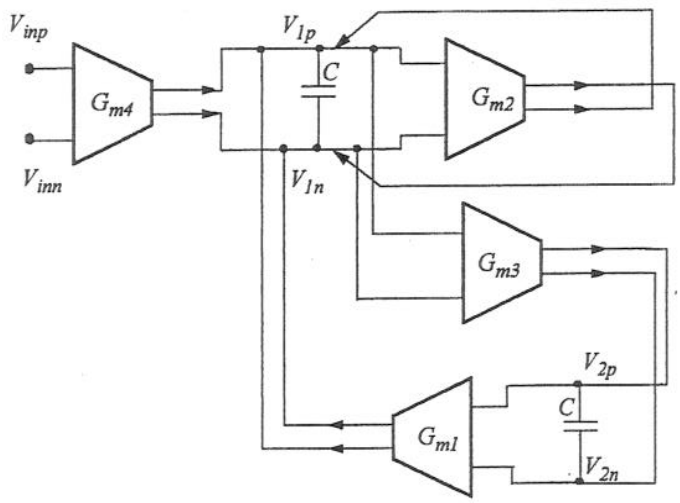

Figure 4

5. (a) Figure 5.1 shows the schematic and equivalent symbol of a FGMOS transistor. Ignoring parasitic effects and assuming that all the capacitances connected to the floating gate have the same value C_{in}, the voltage at the floating gate is given by:

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i$$

where C_T is the total capacitance seen by the floating gate. For the circuit in Fig 5.2, find an expression for the output current as a function of β and (Vb2-Vb1). (Hint: I_{out}=~~(I2-I1)/2~~). What kind of circuit is it?

$= (I_1 - I_2)/2$ [10]

(b) How would you implement an integrator with that block?

[5]

(c) How would you choose the capacitive input ratios (C_i/C_T) of the FGMOS devices to be able to tune a filter built with the block in (b) down to values of 100Hz? Give an equation as a function of the integrating capacitance (C), β and (Vb2-Vb1).

[5]

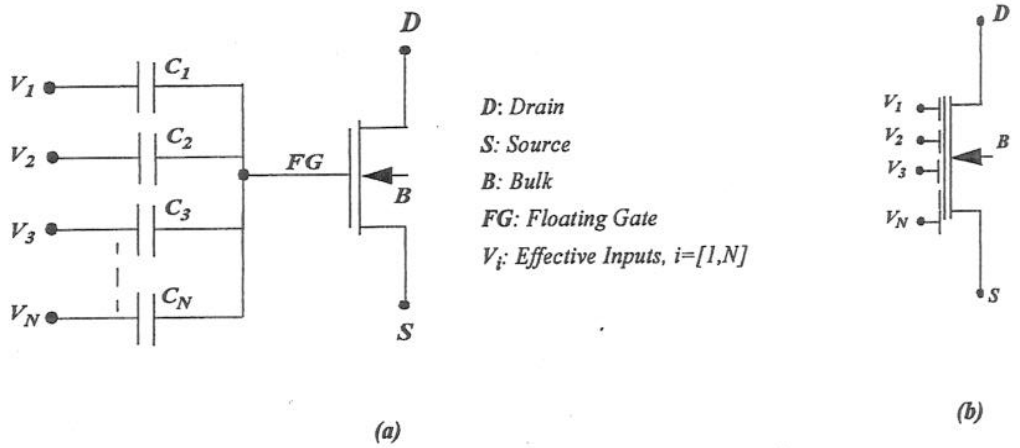

Figure 5.1

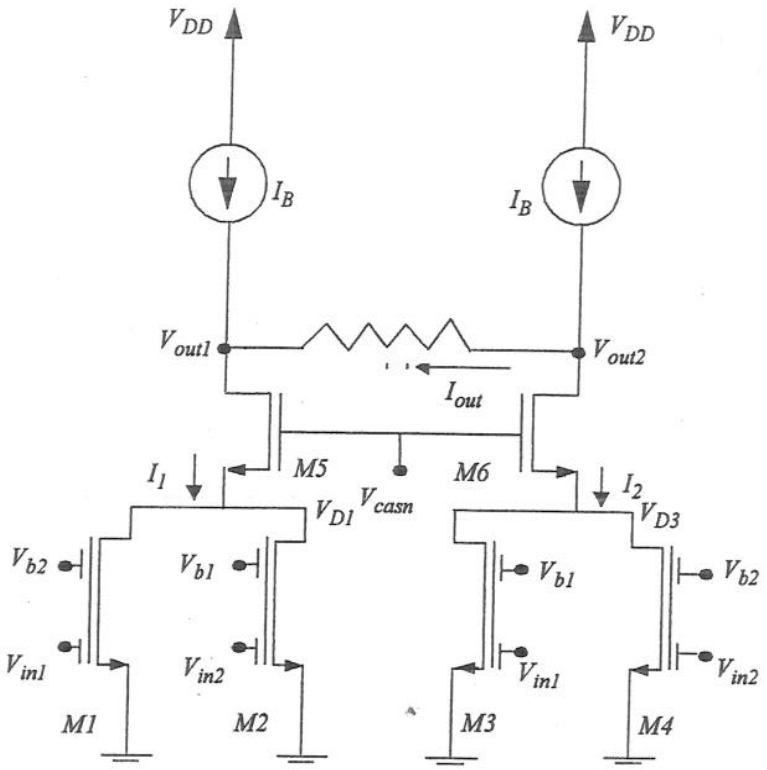
V_{DD}
V_{DD}
I_B
I_B
V_{out1}
V_{out2}
I_{out}
I_1
M5
M6
I_2
V_{D1}
V_{casn}
V_{D3}
V_{b2}
V_{b1}
V_{b1}
V_{b2}
V_{in1}
V_{in2}
V_{in1}
V_{in2}
M1
M2
M3
M4

Figure 5.2

6. (a) The current for n-channel MOS transistor biased in the weak inversion saturation region with its source and bulk grounded and its drain voltage $V_D > 4U_T$ is approximately given by:

$$I_D = I_S exp\left(\frac{V_{GS}}{nU_T}\right)$$

Find an expression for the output current in a differential pair designed with MOS devices in the weak inversion saturation region as a function of the differential input voltage, n, U_T and the bias current. Find also an expression for the same block implemented with bipolar transistors instead. What is the difference between the two equations? Why would you opt for weak inverted MOS devices instead of bipolar to design the differential pair?

[4]

(b) Give one advantage and a disadvantage of biasing the MOS transistors in weak inversion instead of strong inversion.

[4]

(c) If noise is an issue, but not area, how would you improve the previous design?

[4]

(d) After simulating the previous circuit you notice that something is not working as expected. When checking the transistor's operating points, you see the following (the threshold voltage is 0.5V):

M1: V_{GS}=0.6V, V_{DS}=0.1, V_{BS}=0
M2: V_{GS}=0.5V, V_{DS}=0.4 V_{BS}=0

Are those data giving you any hint of something that could be causing the circuit not to work as expected?

[4]

(e) If the transconductor in Fig.6 is designed with the transistors biased in the strong inversion region, how would you choose β_1 and β_2 to minimize distortion.

[4]

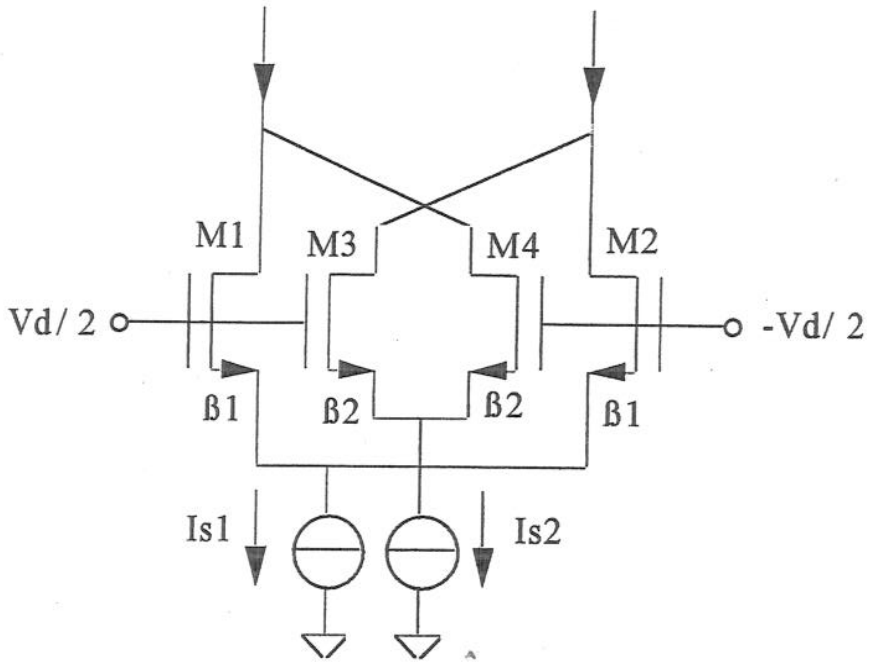

Figure 6

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1.

(a) (theory)

- First filter (preselector): Limits bandwidth of spectrum reaching the RF amplifier (to reduce IM distortion); attenuates receiver spurious responses (esp. image frequency); attenuates oscillator and first IF re-radiation which may be picked up by the antenna.
- Second filter: Attenuates noise at the image frequency, and second harmonics which may originate in the RF amplifier.
- Injection filter: Attenuates wideband noise around the LO frequency, and attenuates oscillator harmonics
- IF stages: The IF filter determines adjacent channel selectivity. This is often a crystal filter (narrowband). Crystal filters are available only in certain centre frequencies, which will constrain the choice of IF. Often the second-image requirement is more stringent on the design of this filter.The IF amplifier is usually a high gain stage.

(b) (theory)

If we are trying to select one particular frequency channel from the complete RF spectrum we need a bandpass filter to reject any unwanted frequencies. Generally this filter has to be narrowband, and high Q filters are difficult to design at high frequencies. This problem is compounded if the input signal frequency is variable. A tuneable, high Q bandpass filter with a constant bandwidth is now required.
A solution is to use a superheterodyne receiver (supersonic heterodyne). This system downconverts the input signal to an intermediate frequency (IF), and a bandpass IF filter is then used to select the wanted signal. The design of the bandpass IF filter is eased since it doesn't have to be tuneable, and the IF frequency is much lower than the input RF signal.

(c) (theory)

In the superheterodyne receiver the downconversion is performed by "mixing" (multiplying) the RF input signal with a local oscillator signal, such that the resulting output is at the required frequency.

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(d) (application of theory)

Advantage: The generation of a purely sinusoidal signal is impossible. It can only be approximated with a certain level of distortion. The lower this level is the more difficult it becomes, whereas a square wave can just be generated with a clock.
The linearity of the mixer block is not as important anymore, since the signal itself is non-linear.,
Disadvantage: Distortion. The output of the mixer has now many other frequency components that need to be eliminated with filtering.

(e) (theory)

They constitute a bandpass filter to filter out the undesired distortion components of the signal which are generated if the latter is mixed with a signal that is not a pure sinewave.

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2.

(a) (new application of theory)

The first one. The full derivation is as follows:

- Considering the first stage alone:

$$F1 = \frac{veq1^2}{vns^2}$$

Thus the equivalent input noise voltage $veq1^2 = F1 vns^2$
This equivalent input noise $veq1^2$ consists of the received (source) input noise, plus internal noise $vn1^2$ contributed by the first stage:

$$veq1^2 = vns^2 + vn1^2$$

$$vn1^2 = veq^2 - vns^2 = (F1-1)\, vns^2$$

- Considering the second stage alone, $vn2^2 = (F2-1)vns^2$

And the same for the N stages: $vnN^2=(FN-1)vns^2$

The total power of noise will then be:

$$vnt^2 = \prod_{i=1}^{N} Gi \cdot vns^2 + \prod_{i=1}^{N} Gi \cdot vn1^2 + \prod_{i=2}^{N} Gi \cdot vn2^2 + \ldots + GN \cdot vnN^2 =$$

$$= \prod_{i=1}^{N} Gi \cdot vns^2 + \prod_{i=1}^{N} Gi \cdot (F1-1) \cdot vns^2 + \prod_{i=2}^{N} Gi \cdot (F2-1) \cdot vns^2 + \ldots + GN \cdot (FN-1) \cdot vnN^2$$

$$F = \frac{vnt^2}{\prod_{i=1}^{N} Gi \cdot vns^2} = F1 + \frac{(F1-1)}{G1} + \ldots + \frac{(FN-1)}{\prod_{i=1}^{N-1} Gi}$$

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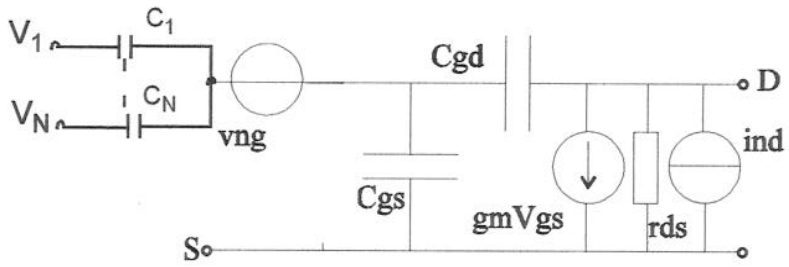
(b) (new application of theory)

In all the regions:

$$g_{mi} = \frac{C_i}{C_T} g_m \qquad \text{for} \qquad i = [1, N]$$

where g_m stands for the transconductance of the constituent MOS device in the specific region.

(c) (application of theory)



$$ind^2 = \frac{8kTgm\Delta f}{3} A^2$$

$$vng^2 = \frac{k_f \Delta f}{CoxWLf} V^2$$

(d) (new theory)

$$\left.\frac{\overline{v_{in}^2}}{\Delta f}\right|_{\text{effective input}} = \left(\frac{1}{w_i}\right)^2 \cdot \left.\frac{\overline{v_{in}^2}}{\Delta f}\right|_{FG} \qquad (1)$$

The noise at the output is the same as in the MOS transistor.

where w_i is the capacitive weight corresponding to the input i and $\left.\frac{\overline{v_{in}^2}}{\Delta f}\right|_{FG}$ is the noise power spectral density at the FG. Equation (1) shows how the equivalent noise increases at the effective input of an FGMOS device, since the factor $(1/w_i)$ is greater than 1. However, in the worst case scenario, the dynamic range (DR) will not be affected because the maximum allowable input signal for a certain level of distortion will also be increased by the same factor $(1/w_i)$. The reason for this is the following: if the input capacitances are assumed to be linear, the signal seen by the FG is actually the signal at the effective input of the FGMOS attenuated by a factor w_i.

In general though, the DR will even improve since, for example, from the system level point of view, the use of the FGMOS will greatly simplify the circuit structure. This will consequently reduce the distortion as well as the noise levels since the number of devices and hence the number of noise contributors will be smaller.

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3.

(a) (new computed example)
Strong inversion saturation:
$V_{out} > V_{in(max)} - V_T$

(b) (application of theory)
$V_{DD} > V_{out} + |V_{Tp}|$

$V_{out(min)} = V_{in(max)} - V_T$

Therefore:
$V_{DD(min)} = V_{in(max)} - V_T + |V_{Tp}|$

(c) (application of theory)
In the ohmic region, the V_{DD} constraint would be:
$V_{DD(min)} = |V_{Tp}|$

(d) (application of theory)
$I_D \approx \beta_n[(V_G - V_{Tn})V_{REF}]$

To keep the drain voltage fixed to a certain voltage, so the topology is linear and also to guarantee the bottom transistor does not leave the strong inversion ohmic region.

(e) (application of theory)
Lower V_{DD} requirement.

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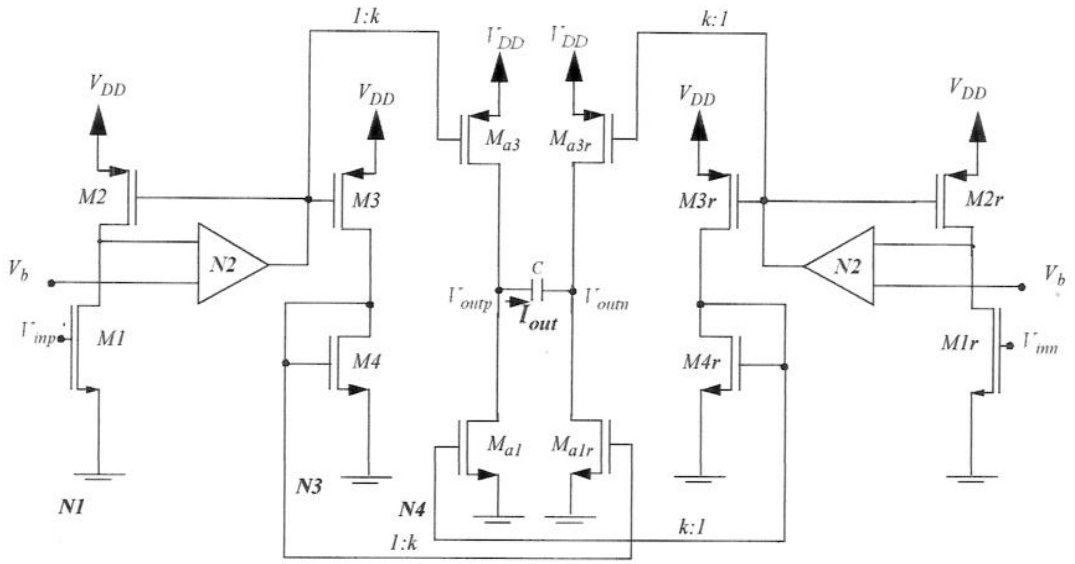
(f) (application of theory)



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4.

(a) (application of theory)

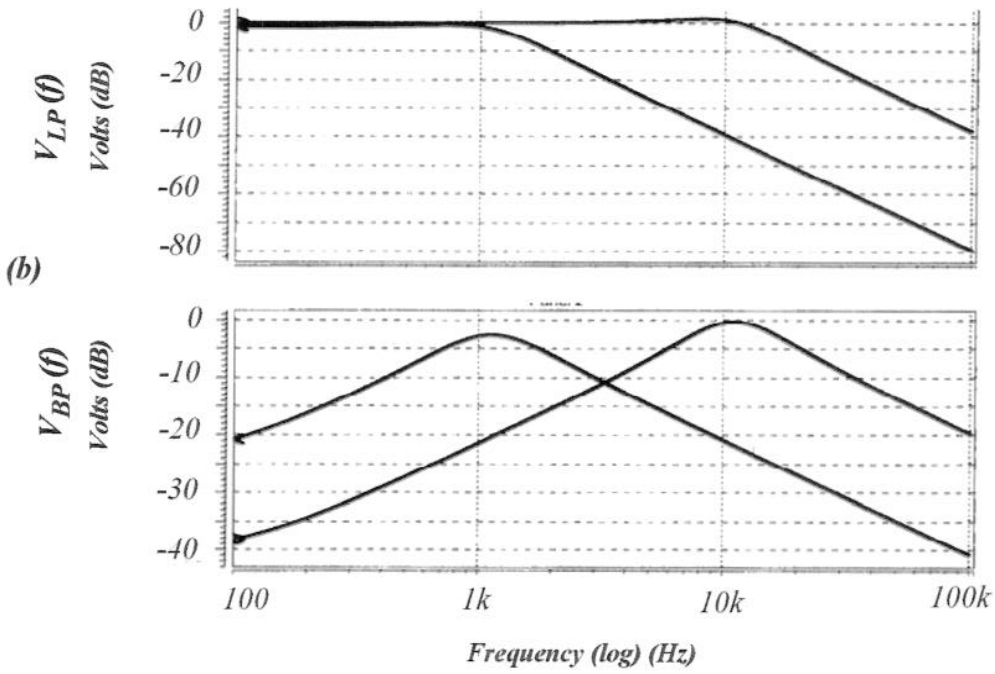
$$\frac{V_{1p}-V_{1n}}{V_{inp}-V_{inn}} = \frac{V_{BP}(s)}{V_{ind}(s)} = \frac{s\frac{G_{m4}}{C}}{s^2+\frac{sG_{m2}}{C}+\frac{G_{m3}G_{m1}}{C^2}}$$

$$\frac{V_{2p}-V_{2n}}{V_{inp}-V_{inn}} = \frac{V_{LP}(s)}{V_{ind}(s)} = \frac{\frac{G_{m3}G_{m4}}{C^2}}{s^2+\frac{sG_{m2}}{C}+\frac{G_{m3}G_{m1}}{C^2}}$$

Bandpass and lowpass filters

(b) (application of theory)

Transfer functions for different parameters values:



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$$\omega_o = \sqrt{\frac{G_{m3}G_{m1}}{C^2}}$$

$$Q = \frac{\sqrt{G_{m3}G_{m1}}}{G_{m2}}$$

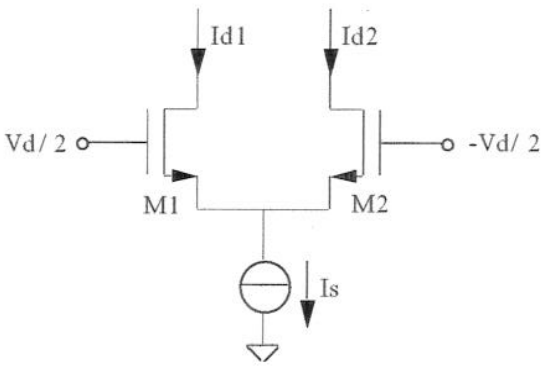
(c) (application of theory)

Speed. Transconductors operate in open loop and hence the speed of the circuit can be equal to the speed of the transconductors. In the case of the OPAMP the bandwidth of the latter has to be around 10 times larger than the maximum speed.

(d) (application of theory)

Many answers are valid. As an example:

As there is no information about constraints, apart from the fact that only five transistors are permitted I would choose the simplest topology: a differential pair. A modification to it could be a differential pair with degeneration resistance. The latter would improve linearity but make noise performance worse.



This circuit with its correponding load would have 5 transistors.

If the number of devices can be double I would probably opt for a linearized topology such as:

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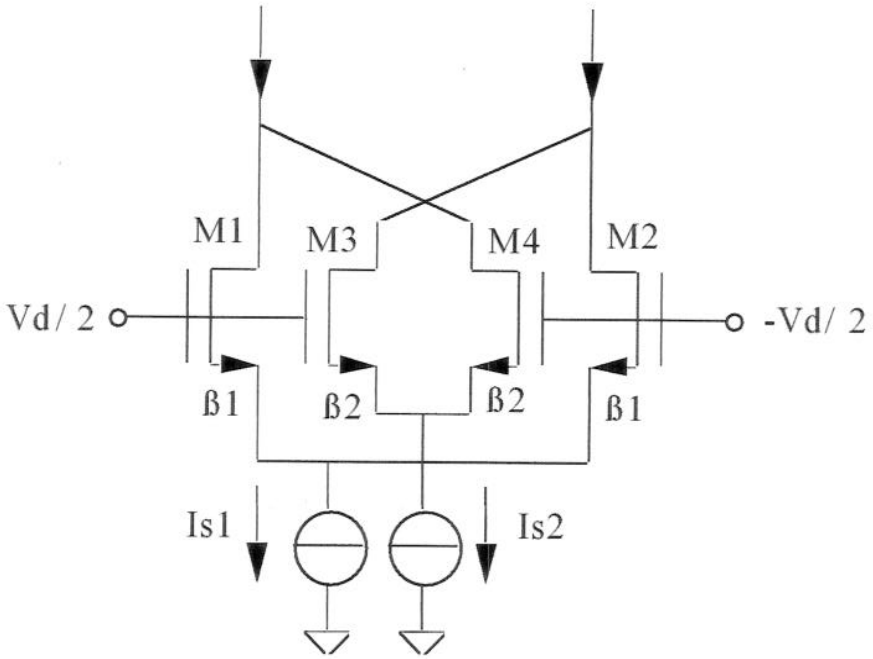

(It's 8 transistors with current sources and load)

(e) (theory)

This is only valid for very small signals. Also second order effects have not been taken into account

$$gm = \frac{\partial Id}{\partial Vgs} = 2\beta(Vgs - Vth) = 2\sqrt{\beta Id}$$

$$\tau = \frac{g_{max}}{C}$$

$$C = \frac{2\sqrt{\beta I_D}}{\tau}$$

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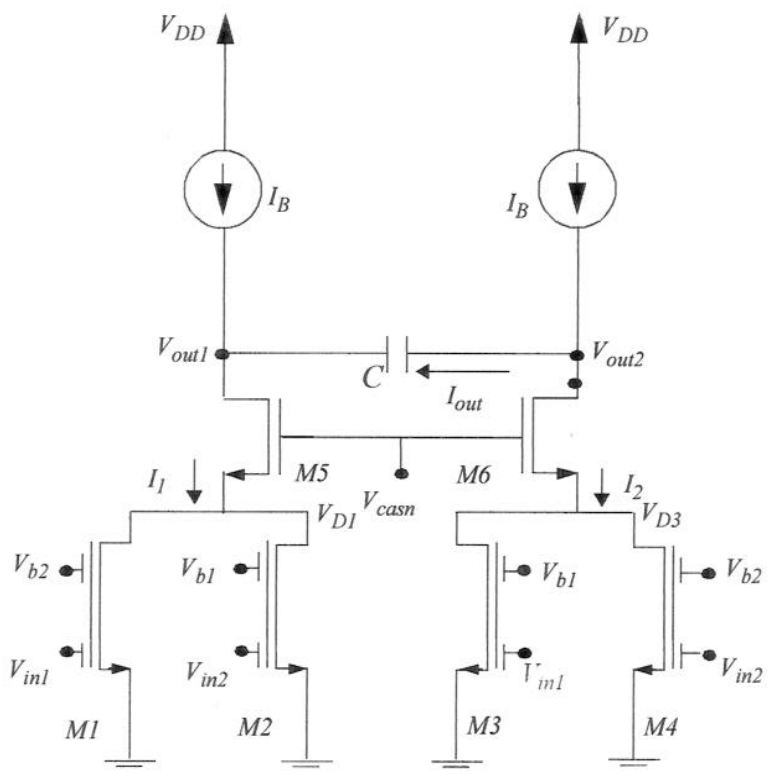
5.

(a) (application of theory)

$$I_{out} = \frac{I_1 - I_2}{2} = \frac{\beta_1 C_{in}^2 (V_{b2} - V_{b1})}{2C_T^2} \cdot (V_{in1} - V_{in2})$$

It is a transconductor

(b) (application of theory)



(c) (application of theory)

$$G_m = \frac{\beta_1 C_{in}^2 (V_{b2} - V_{b1})}{2C_T^2}$$

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The time constant is G_m/C, then:

$$2\pi 100 = (G_m/C)^{-1};\ G_m = C/(2\pi 100);\ \frac{C_{in}}{C_T} = \frac{C}{(2\pi 100)}\sqrt{\frac{2}{\beta_1(V_{b2}-V_{b1})}}$$

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6.

(a)(application of theory)

MOS:

$$I_{out} = 2I_{bias}\tanh\left(\frac{V_{in}}{2\eta U_T}\right)$$

Bipolar:

$$I_{out} = 2I_{bias}\tanh\left(\frac{V_{in}}{2U_T}\right)$$

The (η) parameter

Lower power consumption. Infinite input impedance.

(b) (application of theory)

Increase the size of the transistors to reduce Flicker noise
Design a cross couple topology with scaled sizes to improve linearity and hence keep the DR.

(c) (application of theory)

One of the transistors (M1) is not operating in the weak inversion saturation region.

(d) (theory)

It is a differential configuration. Hence the distortion harmonics are going to be odd order terms and distortion will be dominated by the third order harmonic. The sizes of the transistors (and hence βs) should be chosen so the third order harmonics cancel out without cancelling out the first order harmonic (corresponding to the transconductance)