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IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2005

MSc and EEE PART IV: MEng and ACGI

Corrected Copy

HIGH PERFORMANCE ANALOGUE ELECTRONICS

Thursday, 28 April 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : E. Rodriguez-Villegas
Second Marker(s) : D. Haigh

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1. (a) Figure 1.1 shows the schematic of a superheterodyne receiver. What key decisions need to be addressed in the design of the different blocks within the receiver?

[10]

(b) Explain the superheterodyne principle and the problem of the image in superheterodyne receivers.

[7]

(c) A superheterodyne receiver is tuned to receive an RF signal of 600 MHz. The frequency of the local oscillator ($f_L=\omega_L/2\pi$) is such that the IF signal is 50 MHz. Find the value of f_L and the image frequency.

[3]

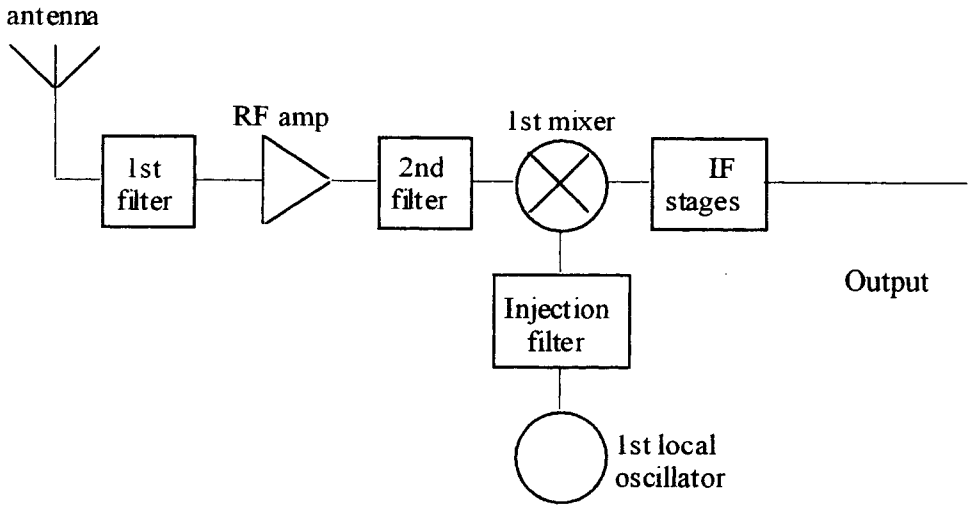

Figure 1.1

2. (a) Derive a formula for the overall noise figure of a cascade of systems, as shown in Figure 2.1. *Fi* is the noise factor of each individual block and *Gi* is the available power gain.

[10]

(b) For the circuit in Figure 2.2; what is the equivalent input noise power spectral density at 1 Hz? What is the equivalent input noise power spectral density at 100 MHz? $vns^2 = vn^2 = 1\ (\text{mV})^2/\text{Hz}$, $in^2 = 1\ (\text{pA})^2/\text{Hz}$, $Rs = 1\ \text{k}\Omega$ and $Cp = 1\ \text{pF}$.

[5]

(c) For the circuit in Figure 2.3; give an expression for the equivalent output noise as a function of the equivalent output noise of transistors M1 and M2 (e_{n1}^2 and e_{n2}^2 respectively). What are the main noise contributors for e_{n1}^2 and e_{n2}^2? How would you design the transistors to reduce the equivalent noise?

[5]

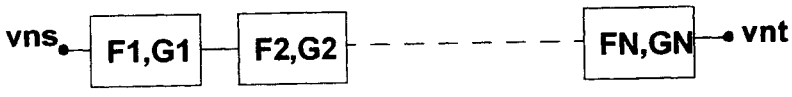

Figure 2.1

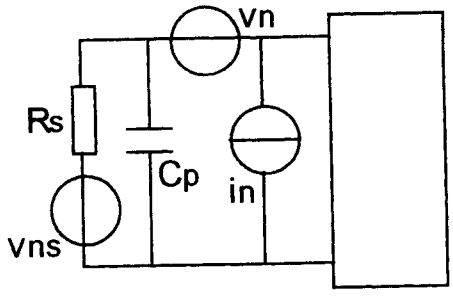

Figure 2.2

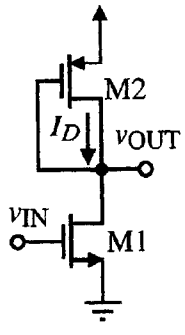

Figure 2.3

3. (a) Derive the transfer function for the circuit in Figure 3.1 $((V_{o1} - V_{o2})/(V_1 - V_2))$. What function does this circuit perform? What are the advantages of this topology versus simpler ones? Can you suggest any reason why the circuit might not behave as expected?

[10]

(b) Using the result obtained in (a), obtain the transfer function for the circuit in Figure 3.2.

[5]

(c) What would be the value of C in Figure 3.2 if the pole due to the 1kΩ resistance is to be at 1 MHz?

[5]

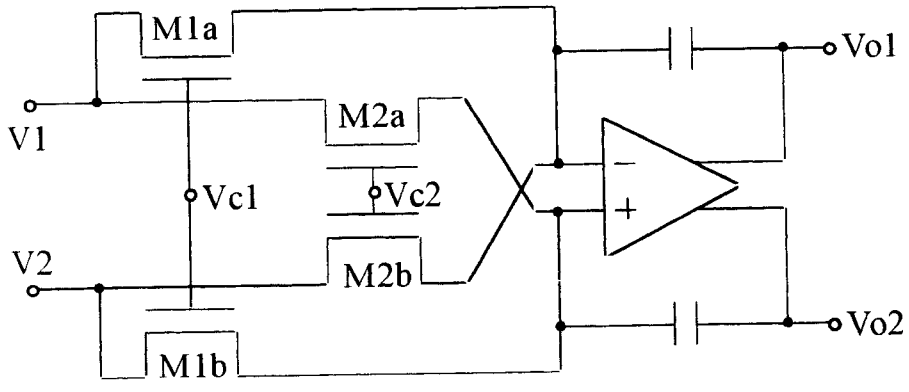

Figure 3.1

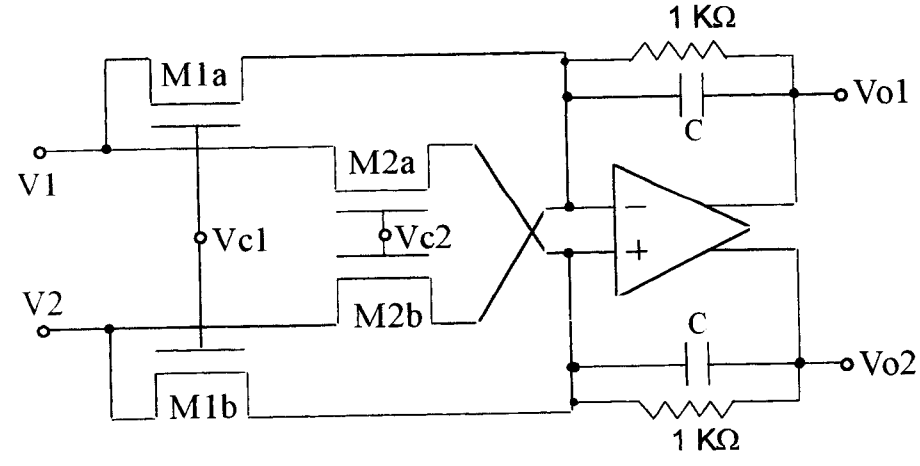

Figure 3.2

4. (a) Figure 4.1 shows a transconductor proposed by Szczepanski et al. in IEEE Transactions on Circuits and Systems II in 1997. Assuming that the transistors are operating in strong inversion and $I_a=I_b=I_{bias}$, what is the expression of the output current, $I_{out}=I_1-I_2$?

[10]

(b) If transconductor is designed in such a way that the value of the transconductance is 1 mS, how would you design a lossless integrator with a time constant of 1 ns?

[5]

(c) Enumerate advantages and disadvantages of the previous topology. How could you change the value of the transconductance after fabrication? How could you implement a mixer using the previous topology?

[5]

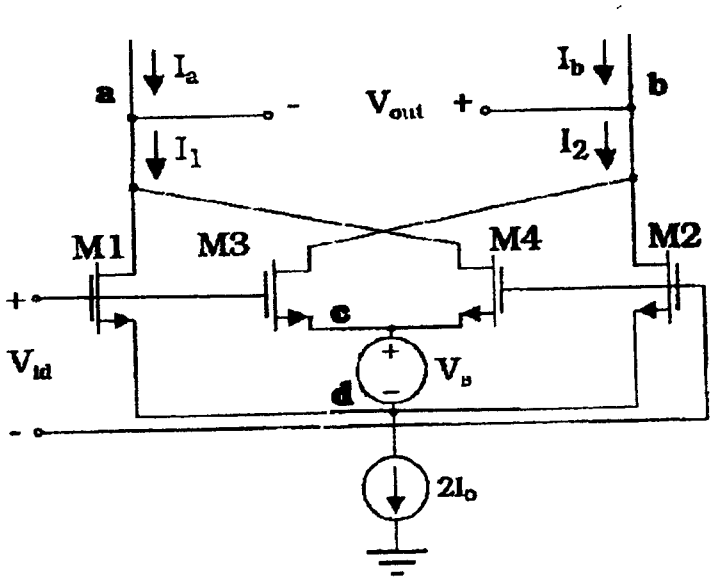

Figure 4.1

5. (a) Figure 5.1 shows an active implementation of an LC-ladder filter. Draw the flow diagram corresponding to that topology.

[10]

(b) Draw the LC ladder corresponding to the flow diagram in (a).

[5]

(c) Describe two possible implementations for the integrators in Figure 5.1. What are the advantages and disadvantages of each implementation?

[5]

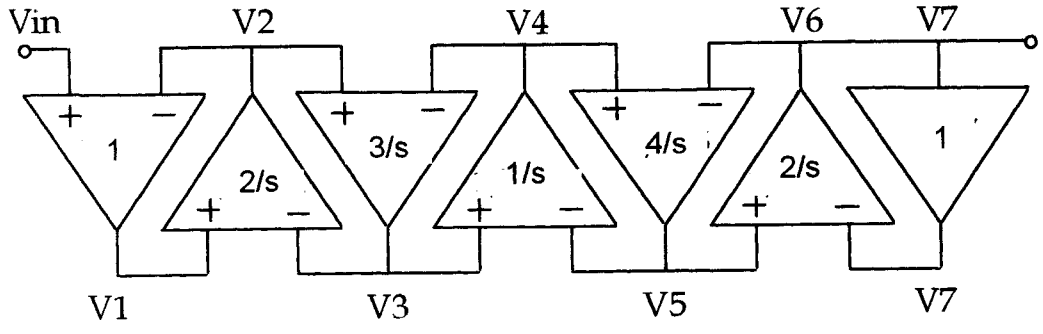

Figure 5.1

6. (a) Explain a way of implementing a transconductor using a single MOS transistor operating in the ohmic/triode region. Give an expression for the transconductance.

[10]

(b) How would you use a differential amplifier to improve the design? Give an expression for the transconductance.

[5]

(c) How would you design the biasing current source for the circuit in part (b) in order to optimize the transconductor's performance? Draw the schematic corresponding to this implementation.

[5]

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1

(a) (theory)

• Antenna: Must be connected to dc ground to prevent static charge accumulation.

• 1st filter (preselector): Limits bandwidth of spectrum reaching the RF amplifier (to reduce IM distortion); attenuates receiver spurious responses (esp. image frequency); attenuates oscillator and first IF re-radiation which may be picked up by the antenna.

• RF amplifier: Noise figure and gain are determined by receiver sensitivity requirements. Amplifier gains greater than 20 dB are usually undesirable, because the required gain may not be achievable from a single device, and high signal levels at the mixer will place severe constraints on mixer linearity.

• 2nd filter: Attenuates noise at the image frequency, and second harmonics which may originate in the RF amplifier.

• First mixer: Mixer performance is possibly the single most important determinant of receiver performance. The mixer encounters the highest RF levels within the receiver, so requires a high intercept point.

• Local oscillator: The oscillator phase noise will determine the adjacent channel performance. LO harmonics will also cause spurious responses. LO implementation will depend on the actual application (i.e. fixed or programmable frequency etc.)

• Injection filter: Attenuates wideband noise around the LO frequency, and attenuates oscillator harmonics.

• IF stages: The IF filter determines adjacent channel selectivity. This is often a crystal filter (narrowband). Crystal filters are available only in certain centre frequencies, which will constrain the choice of IF. Often the second-image requirement is more stringent on the design of this filter. The IF amplifier is usually a high gain stage.

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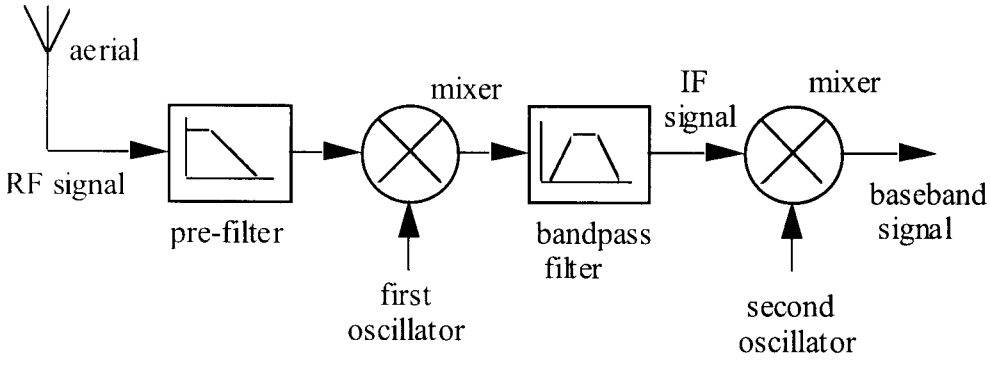
(b) (theory)

If we are trying to select one particular frequency channel from the complete RF spectrum, then we need a bandpass filter to reject any unwanted frequencies. Generally this filter has to be narrowband, and high Q filters are difficult to design at high frequencies. This problem is compounded if the input signal frequency is variable (i.e. the signal is transmitted in one of a number of possible channels, each with the same bandwidth). A tuneable, high Q bandpass filter with constant bandwidth is now required.

The solution is to use a superhet receiver (supersonic heterodyne). This system downconverts the input signal to an intermediate frequency (IF), and a bandpass IF filter is then used to select the wanted signal. The design of the bandpass IF filter is eased since it doesn't have to be tuneable, and the IF centre frequency is much lower than the input RF signal.



The downconversion is performed by 'mixing' (multiplying) the RF input signal (f_{RF}) with a local oscillator signal (f_{LO}), such that the resulting output is at the required IF frequency (f_{IF}).

Received RF signal = $2A\cos[(f_{RF})t + \theta]$ Local oscillator signal LO = $\cos(f_{LO})t$

Mixer output = $2A\cos(f_{LO})t \cos[(f_{RF})t + \theta]$

= $A\cos[(f_{LO} - f_{RF})t - \theta] + A\cos[(f_{LO} + f_{RF}) + \theta]$

i.e. sum and difference components

The sum components are at a very high frequency and are removed by filtering. The difference frequency component is a replica of the RF component in terms of amplitude and phase, but is shifted down to an intermediate frequency (IF):

$$f_{IF} = f_{LO} - f_{RF}$$

The oscillator frequency f_{LO} is often tuneable to ensure that a range of input RF frequencies can be selected.

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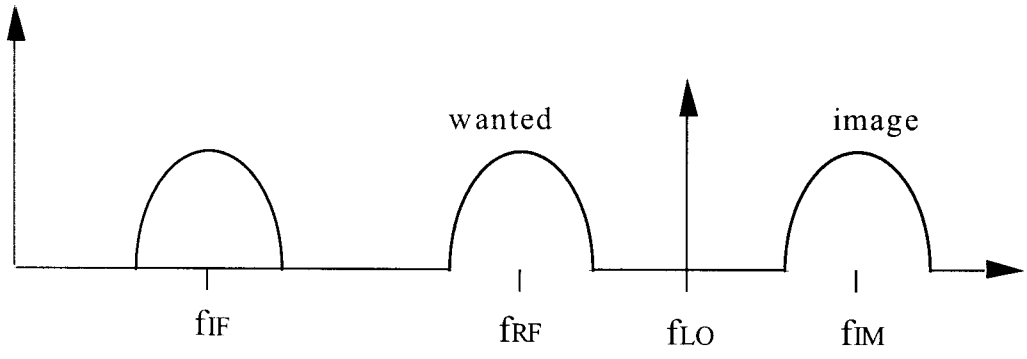
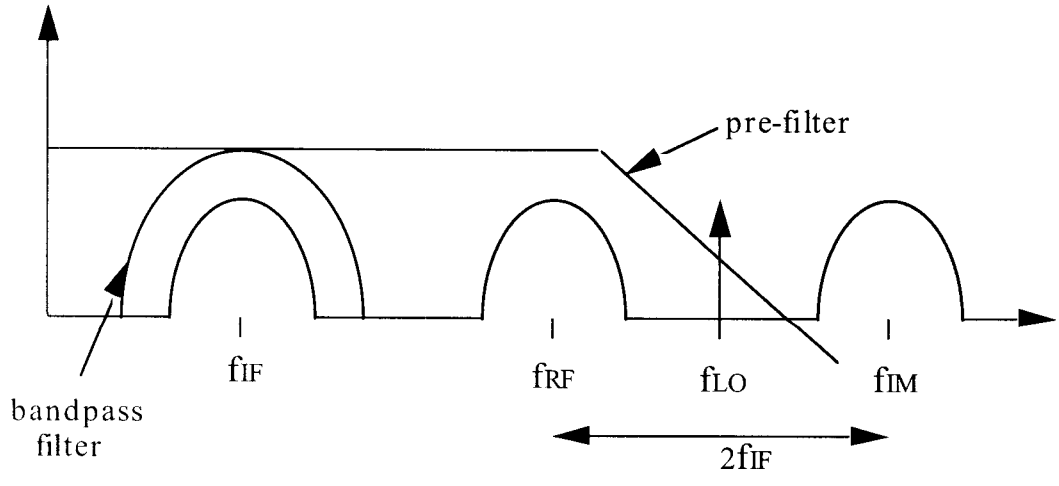
• Image signals: An image channel (f_{IM}) is also converted to the intermediate frequency, where $f_{IF} = f_{IM} - f_{LO}$



This image signal must be suppressed by filtering before downconversion. The pre-filter can be a simple low pass filter. The pre-filter should pass RF signals that are at $f_{LO}-f_{IF}$, but reject image signals at $f_{LO}+f_{IF}$. The design of the pre-filter is thus eased if f_{IF} is fairly high.



The bandpass filter that selects the required channel is centred at f_{IF}. The design of this filter is eased if f_{IF} is fairly low. Thus there is a trade-off between these two requirements.

(c) (new computed example)

f_L is 650 MHz and the image is 700 MHz.

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(a) (new application of theory)

- Considering the first stage alone:

$$F1 = \frac{veq1^2}{vns^2}$$

Thus the equivalent input noise voltage $veq1^2 = F1 vns^2$
This equivalent input noise $veq1^2$ consists of the received (source) input noise, plus internal noise $vn1^2$ contributed by the first stage:

$$veq1^2 = vns^2 + vn1^2$$

$$vn1^2 = veq^2 - vns^2 = (F1-1)\, vns^2$$

- Considering the second stage alone, $vn2^2 = (F2-1)vns^2$

And the same for the N stages: $vnN^2=(FN-1)vns^2$

The total power of noise will then be:

$$vnt^2 = \prod_{i=1}^{N} Gi \cdot vns^2 + \prod_{i=1}^{N} Gi \cdot vn1^2 + \prod_{i=2}^{N} Gi \cdot vn2^2 + \ldots + GN \cdot vnN^2 =$$

$$\prod_{1}^{N} Gi \cdot vns^2 + \prod_{i=1}^{N} Gi \cdot (F1-1) \cdot vns^2 + \prod_{i=2}^{N} Gi \cdot (F2-1) \cdot vns^2 + \ldots + GN \cdot (FN-1) \cdot vnN^2$$

$$F = \frac{vnt^2}{\prod_{i=1}^{N} Gi \cdot vns^2} = F1 + \frac{(F1-1)}{G1} + \ldots + \frac{(FN-1)}{\prod_{i=1}^{N-1} Gi}$$

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(b) (new computed example)

$$vneq(t) = vns(t) + vn(t) + in(t)Rs + vn(t)Rs/Xcp$$

$$= vns(t) + vn(t)(1+Rs/Xcp) + in(t)Rs$$

$$vni^2 = vns^2 + vn^2|1 + Rs/Xcp|^2 + in^2 Rs^2$$

$$= vns^2 + vn^2(1 + (\omega CpRs)^2) + in^2 Rs^2$$

At 1 Hz : 2 $(mV)^2/Hz$
At 100 MHz: 2.394 $(mV)^2/Hz$

(c) (new application of theory)

$$e_{out}^2 = e_{n1}^2\left(\frac{g_{m1}}{g_{m2}}\right)^2 + e_{n2}^2$$

The main sources of noise are flicker at low frequency and thermal noise. If the length of M1 is much smaller than that of M2, the input 1/f noise will be dominated by M1. To minimize the 1/f contribution due to M1, its width must be increased. The thermal noise can be reduced by increasing the transconductance of the transistors. This can be achieved either by increasing the quiescent current or the width of the transistors.

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3

(a) (application of theory)

It's a lossless MOSFET-C integrator

$$Vo1 - Vo2 = \frac{1}{sC}\left(Id1a + Id2b - Id1b - Id2a \right)$$

$$= \frac{1}{sC}\left((G1-G2)(V1-V2)+(\beta 1-\beta 2)\left(V2^2 - V1^2\right)\right)$$

Provided that devices are matched (equal β), then $Vout = \frac{(G1-G2)}{sC}(V1-V2)$

where G1 – G2 = 2β(Vc1 – Vc2)

Advantages: The fully balanced topology cancels out even order harmonics.
The transconductance does not depend on the threshold voltage.
No differential inputs have to be generated.

Disadvantage: The output resistance of the Opamp generates losses in the transfer function.
The new transfer function would be:

$$V_{out} = \frac{(G1-G2)}{sC + R_{out}^{-1}}(V1-V2)$$

(b) (application of theory)

$$V_{out} = \frac{(G1-G2)}{sC + 10^{-3}}(V1-V2)$$

(c) (new computed example)

15.92pF

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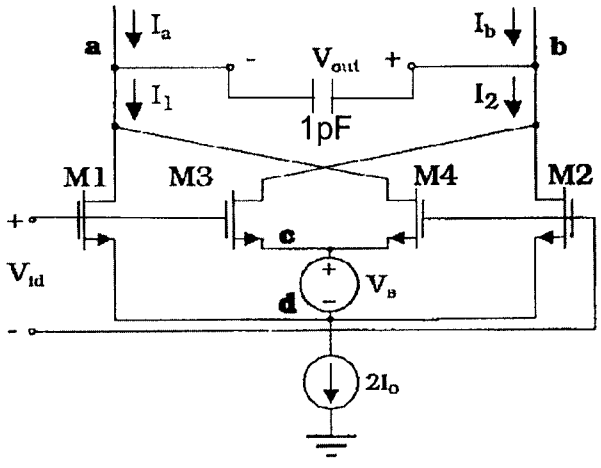
4.

(a) (new theory)

After analysing the circuit, assuming that all the transistors are operating in the strong inversion saturation region:

$$I_{out} = 2\beta_n V_B V_{id}$$

(b) (new theory)



(c) (new theory)

Advantages: The transconductance does not depend on the threshold voltage. It's tunable through V_B. The cross-couple topology cancels out even order harmonics.

Main disadvantage: The output resistance of the transistors originates losses in the transfer function.

It can be tuned through V_B.

A mixer can be implemented by using V_B as a second input.

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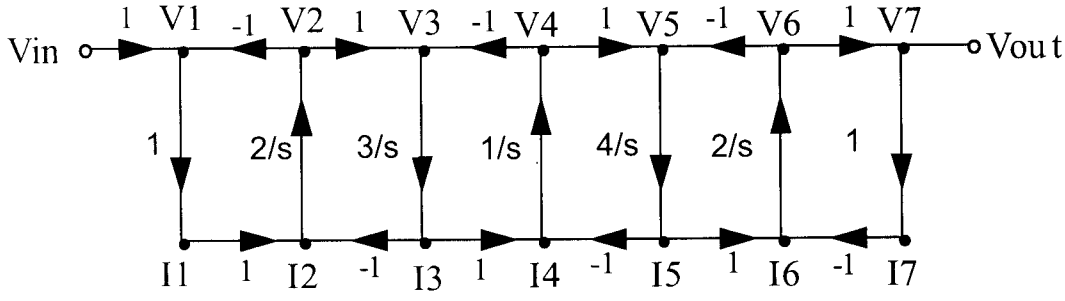
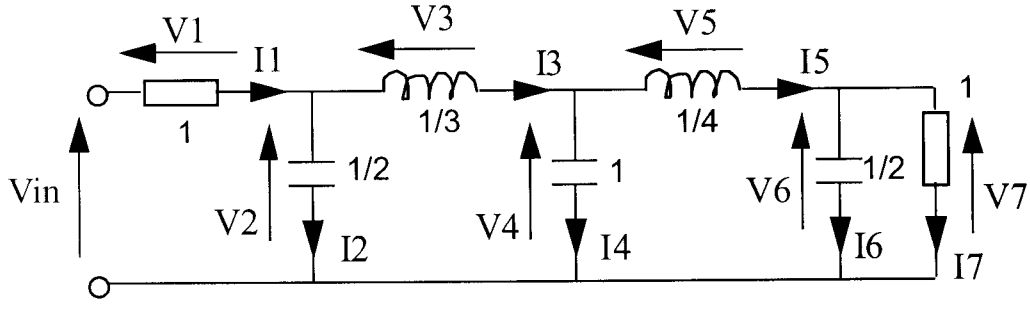
(a) (application of theory and new computed example)

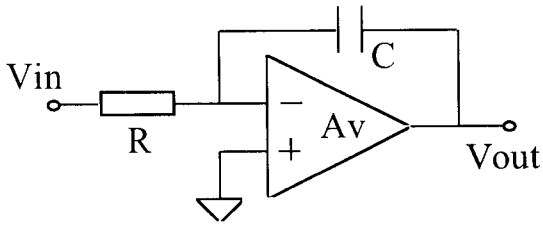


(b) (application of theory and new computed example)



(c) (theory)

Op-amp RC ($\tau = RC$)



Requires a process with linear, stable resistors and capacitors. Not easily tuneable. Capacitor has one end at virtual earth, which eliminates parasitic effects.

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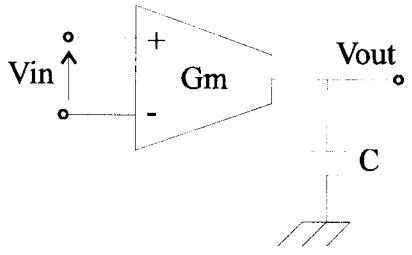
Gm-C

- Single-ended integrator:



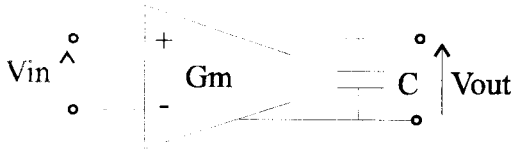
$$\frac{Vout}{Vin} = \frac{Gm}{sC} = \frac{\omega u}{s}$$

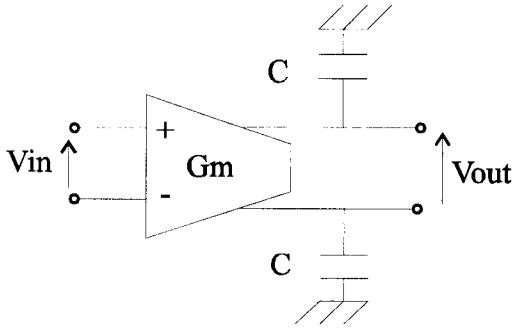
ωu = unity-gain frequency

To implement a summing integrator we simply connect transconductors in parallel since the output currents will sum together.

- Fully-differential integrator:

In most integrated applications it is desirable to keep the signals fully-differential to improve noise immunity and distortion performance.





ωu = Gm/C in both cases

The first circuit will suffer from the effect of bottom plate parasitic capacitance. The second circuit is therefore preferable, although at the expense of an increased area (higher capacitance). Even in the second circuit, some parasitics may remain in parallel with C (due to output devices of the transconductor etc), thus C must be kept fairly high to swamp out the parasitics.

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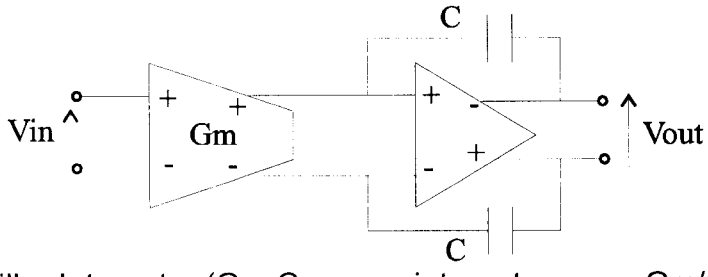
- Miller Integrator



Miller Integrator (Gm-C opamp integrator, ωu = Gm/C)

To further reduce the effect of parasitics, a common approach is to realise a Miller integrator. The transconductor outputs are at virtual earth, which has several benefits:

The transconductor can have a lower output impedance

The transconductor output is not subjected to large voltage swings, so there will be no slew rate problems at these nodes

Transconductor output capacitance does not affect the integrator unity-gain frequency.

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(a) (theory)

The drain current of a MOSFET in the triode region is given by the equation:

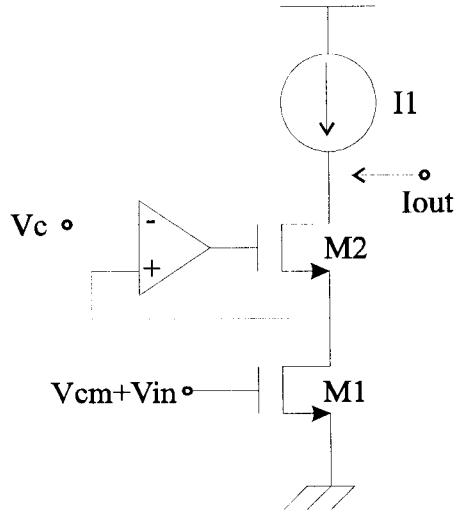
$Id = 2\beta(Vgs-Vth)Vds - Vds^2/2)$ where $\beta=KW/2L$

or

$Id = G\,Vds - \beta Vds^2$ where $G = 2\beta(Vgs - Vth)$.

To operate in the triode region the device must be biased with $Vds < (Vgs - Vth)$. Neglecting the Vds^2 term, the device acts as a resistor with small-signal resistance $dVds/dId = 1/G$. If greater accuracy is required we cannot simply neglect the Vds term, but must cancel it out.

(b) (theory)



Assuming M1 is in the triode region:

$Id1 = 2\beta(Vcm + Vin - Vth)Vc - \beta Vc^2$

If we set $I1 = 2\beta(Vcm - Vth)Vc - \beta Vc^2$, then $Iout = Id1 - I1 = (2\beta Vc)Vin$

$G_m = (2\beta V_c)$

(c) (new theory)

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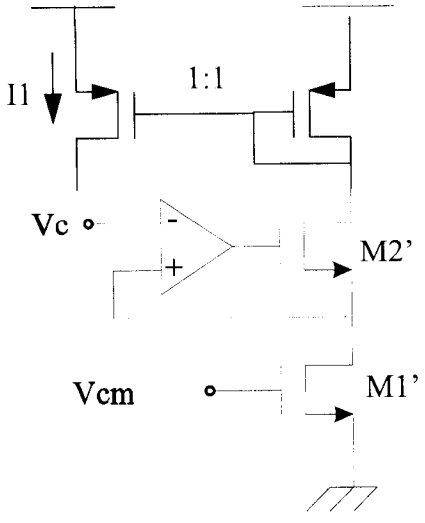

where M1' has to be matched with M1 and M2' with M2.