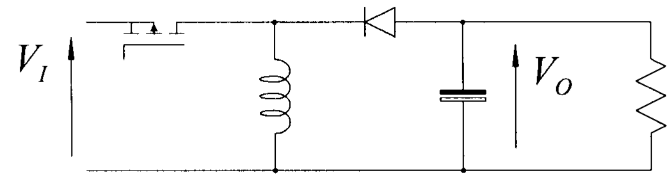
Power Electronics & Machines

Solutions

1. A switch-mode power supply (SMPS) is required to form a -15 V supply (V_O) from an original source of 5 V (V_I). Two possible solutions are examined in this question. The circuit is required to supply output currents between 0.1 A and 2.0 A. The switching frequency chosen is 25 kHz and the output voltage ripple must be less than 100 mV (peak to peak)

(a) For a flyback SMPS

(i) Draw a circuit diagram of the SMPS [2]



(ii) Give the expression for the ratio of output voltage to input voltage for continuous operation [1]

$$\frac{V_O}{V_I} = \frac{-\delta}{1-\delta}$$

(iii) Choose an inductor value to ensure the circuit remains in continuous operation. [4]

$$I_O = I_L(1-\delta)$$

Critical current is:

$$I_L = \tfrac{1}{2}\Delta i_L$$

$$\Delta i_L = 2\frac{I_O^{Min}}{1-\delta}$$

$$\Delta i_L = \frac{V_I}{L}\cdot\frac{\delta}{f}$$

$$L = \frac{V_I(1-\delta)}{2I_O^{Min}}\cdot\frac{\delta}{f}$$

$$\delta = \frac{-V_{Ov}}{V_I - V_O} = \frac{15}{5+15} = 0.75$$

$$L = \frac{5\times 0.25}{2\times 0.1}\times\frac{0.75}{25\times 10^3} = 188\,\mu H$$

(iv) Specify the effective series resistance of the capacitor [3]

$$v_O^{ptp} = R_{ESR}\, i_C^{ptp}$$

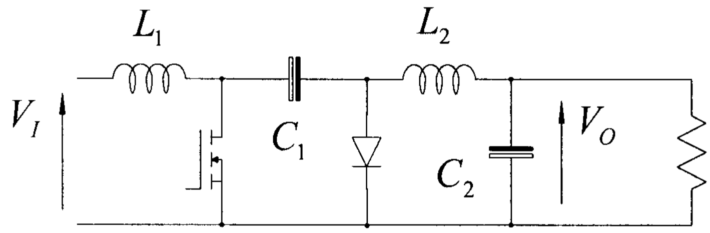
$$i_C^{\,ptp} = I_L + \tfrac{1}{2}\Delta i_L$$

$$i_C^{\,ptp-\max} = \frac{I_O^{\,\max}}{1-\delta} + \tfrac{1}{2}\frac{V_I\delta}{Lf} = \frac{2}{0.25} + \frac{5\times 0.75}{2\times 188\times 10^{-6}\times 25\times 10^{3}} = 8 + 0.4 = 8.4\,A$$

$$R_{ESR} = \frac{v_O^{\,ptp}}{i_C^{\,ptp}} = \frac{0.1}{8.4} = 12\,m\Omega$$

(b) For a Ćuk SMPS

(i) Draw a circuit diagram of the SMPS [2]



(ii) Give the expression for the ratio of output voltage to input voltage for continuous operation [1]

$$\frac{V_O}{V_I} = \frac{-\delta}{1-\delta}$$

(iii) Choose inductor values to ensure the circuit remains in continuous operation. [4]

Critical current in each case is:

$$I_L = \tfrac{1}{2}\Delta i_L$$

$$I_{L1} = I_I \approx \frac{I_O V_O}{V_I} \qquad I_{L2} = I_O$$

$$\Delta i_{L1} = \frac{V_I}{L_1}\cdot\frac{\delta}{f} \qquad \Delta i_{L2} = \frac{V_0}{L_2}\cdot\frac{1-\delta}{f}$$

$$L_1 = \frac{V_I^{\,2}}{2I_O^{\,Min}\,V_O}\cdot\frac{\delta}{f}$$

$$= \frac{5^2}{2\times^{-}0.1\times^{-}15}\times\frac{0.75}{25\times 10^{3}} = 250\,\mu H$$

$$L_2 = \frac{V_O}{2I_O^{\,Min}}\cdot\frac{1-\delta}{f}$$

$$= \frac{-15}{2\times^{-}0.1}\times\frac{0.25}{25\times 10^{3}} = 363\,\mu H$$

(iv) Specify the effective series resistance of the capacitor [3]

$$i_C^{\,ptp} = \Delta i_{L2}$$

$$i_C^{\,ptp} = \frac{V_0(1-\delta)}{L_2\, f} = 2I_O^{\,Min} = 0.2\,A$$

$$R_{ESR} = \frac{v_O^{\,ptp}}{i_C^{\,ptp}} = \frac{0.1}{0.2} = 500\,m\Omega$$

2.

(a) Figure Q2a shows the drain-source voltage and drain current of the transistor in figure Q2b. The parameters marked in the figure have the following values:

$T = 20\ \mu s$

$t_{On} = 16\ \mu s$

$V_{DC} = 550\ V$

$V_{DS(On)} = 2.5\ V$

$I_L = 25\ A$

$t_{ri} = 150\ ns$

$t_{fv} = 30\ ns$

$t_{rv} = 30\ ns$

$t_{fi} = 200\ ns$

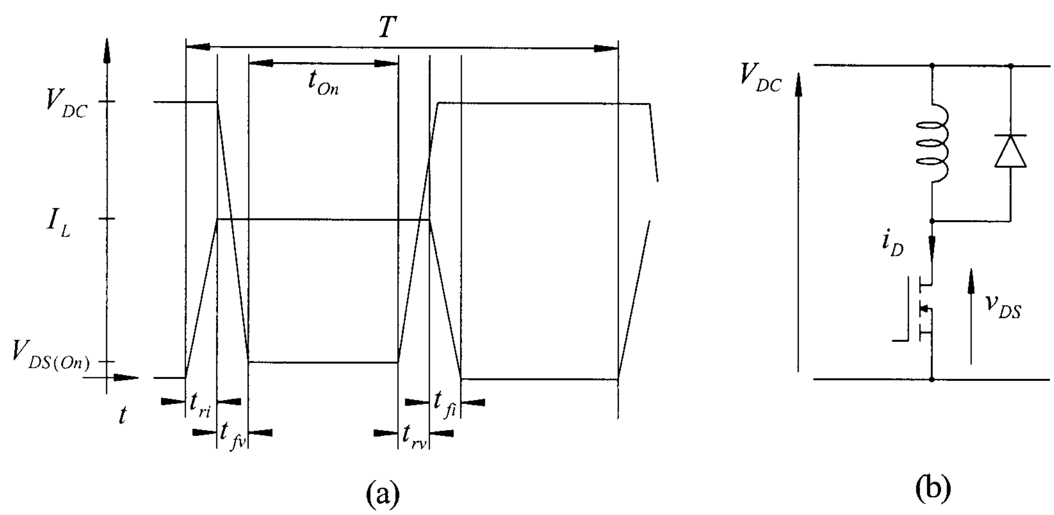


Figure Q2

Calculate the power loss in the transistor. [6]

$$P_{Loss} = V_{DS(On)}\, I_L \frac{t_{On}}{T} + \tfrac{1}{2} V_{DC}\, I_L \frac{\left(t_{ri} + t_{fv} + t_{rv} + t_{fi}\right)}{T}$$

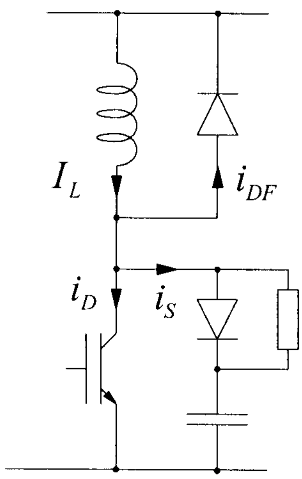
$$= 2.5 \times 25 \times \frac{16}{20} + \tfrac{1}{2} \times 550 \times 25 \times \frac{410 \times 10^{-9}}{20 \times 10^{-6}}$$

$$= 50 + 141$$

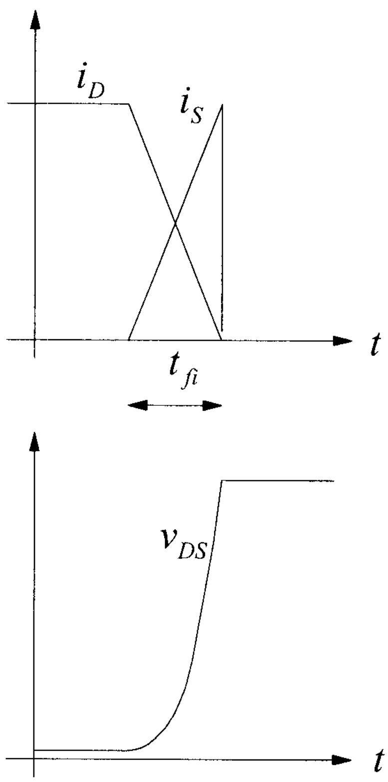
$$= 191\, W$$

(b) A turn-off snubber is be added to the circuit of Figure Q2b to reduce the power loss in the transistor. The capacitor is to be chosen so that the voltage across it rises in exactly the fall time of the current (t_{fi}).

(i) Sketch the circuit to be used [2]



(ii) Sketch the waveforms of the current in the collector and voltage across the snubber capacitor [2]



(iii) Calculate the value of capacitor required [4]

$$i_S(t) = I_L \frac{t}{t_{fi}}$$

$$v_S(t) = \frac{1}{C}\int i_S(t)dt = \frac{I_L t^2}{2Ct_{fi}}$$

$$C = \frac{t_{fi}}{2V_{DC}} = \frac{25\times 200\times 10^{-9}}{2\times 550} = 4.5nF$$

(iv) Choose a suitable discharge resistor [2]

$$5\tau \le t_{Off}$$

$$R \le \frac{t_{Off}}{5C} = \frac{(20-16)\times 10^{-6}}{5\times 4.5\times 10^{-9}} = 160\,\Omega$$

(v) Calculate the turn-off power loss in the transistor and the loss in the reset resistor [4]

$$P_{Loss}^{Turn-Off} = \frac{1}{T}\int^{t_{fi}} i_D(t)v_S(t)dt$$

$$= \frac{1}{T}\int^{t_{fi}}\left(I_L\left(1-\frac{t}{t_{fi}}\right)V_{DC}\frac{t^2}{t_{fi}^{\ 2}}\right)dt$$

$$= \frac{V_{DC}I_L}{T}\left[\frac{\frac{1}{3}t^3}{t_{fi}^{\ 2}} - \frac{\frac{1}{4}t^4}{t_{fi}^{\ 3}}\right]_0^{t_{fi}}$$

$$= \frac{V_{DC}I_L}{T}\cdot\frac{t_{fi}}{12}$$

$$= \frac{550\times 25\times 200\times 10^{-9}}{20\times 10^{-6}\times 12} = 11.46W$$

(Was previously 80 W)

$$P_R = \tfrac{1}{2}CV_{DC}^{\ 2}\frac{1}{T}$$

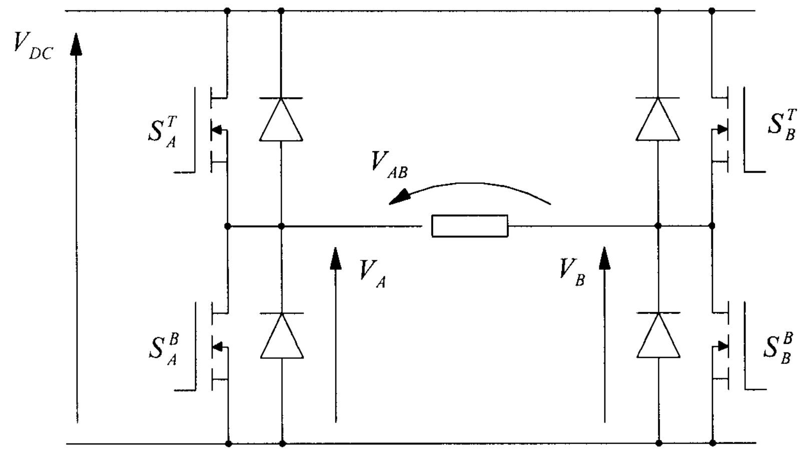
$$= \tfrac{1}{2}\times 180\times 10^{-12}\times 550^2\times\frac{1}{20\times 10^{-6}}$$

$$= 1.36W$$

3.

(a) For a single-phase DC to AC converter (inverter):

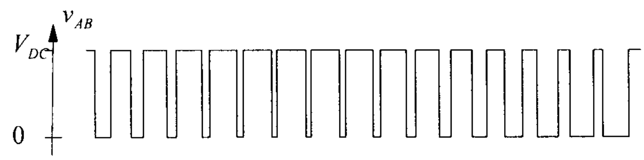
(i) Sketch the circuit diagram of the circuit [2]



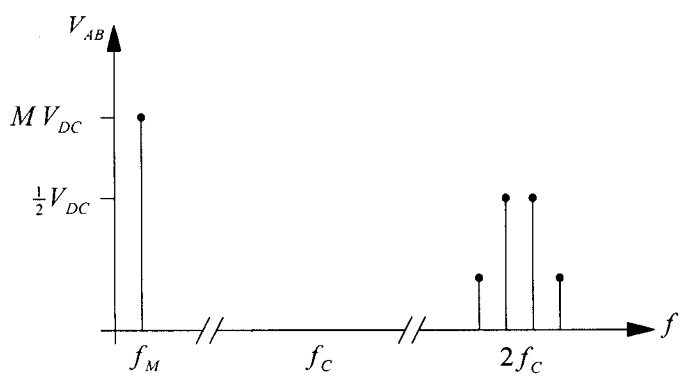
(ii) Describe its operation and in particular describe how the signals to control the switches are obtained [2]

Each half of the H-bridge contains two transistors that are switched in anti-phase so that V_A and V_B can both be varied between 0 and V_{DC}. The switches are switched at high frequency and the pulse-widths modulated to give a sinusoidal distribution of average voltage. The modulation is achieved by comparing the desired wave-shape with a triangle wave carrier. The switches on side-B are switched in the same way as side-A except that (i) the carrier is in anti-phase (to cancel the first carrier frequency itself) and (ii) the modulating signal is inverted (so that when VB is subtracted from VA the base-band signal adds)

(iii) Sketch the AC voltage waveform in the time domain [1]



(iv) Sketch the frequency spectrum of the AC voltage and describe its features [2]



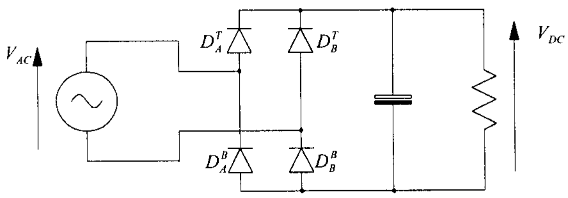
There is

- *no DC term*
- *the base-band signal is proportional to the depth of modulation and the DC voltage*
- *the first carrier term and sidebands are cancelled*

- *the second, and all even, carrier multiples sidebands present*

(b) For a single-phase rectifier (AC to DC converter) using a diode bridge and a large valued smoothing capacitor:

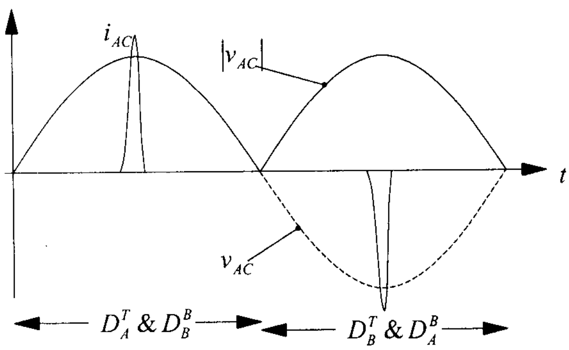
(i) Sketch the circuit diagram of the circuit [1]



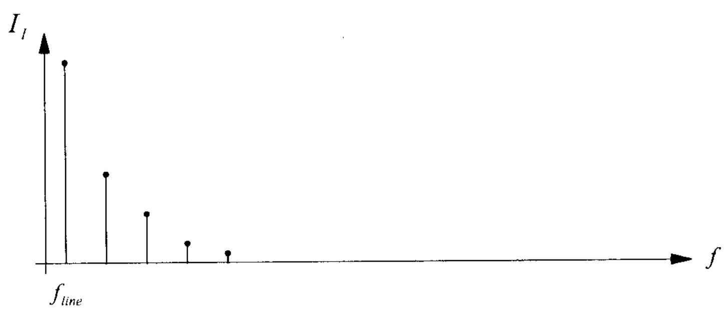
(ii) Describe its operation and in particular what determines the shape of the current waveform [2]

The diodes begin conduction when the AC voltage exceeds the DC voltage. The rise of current is set by the inductance of the current loop which will be composed of source inductance and wiring inductance within the circuit. When the DC voltage plus resistive voltage drop exceeds the AC voltage (shortly before the peak of the AC voltage)the current will start to decrease again and will decay to zero. This current pulse is normally brief but must supply the energy that is transferred to the load during the whole of the cycle.

(iii) Sketch the AC current waveform in the time domain [1]



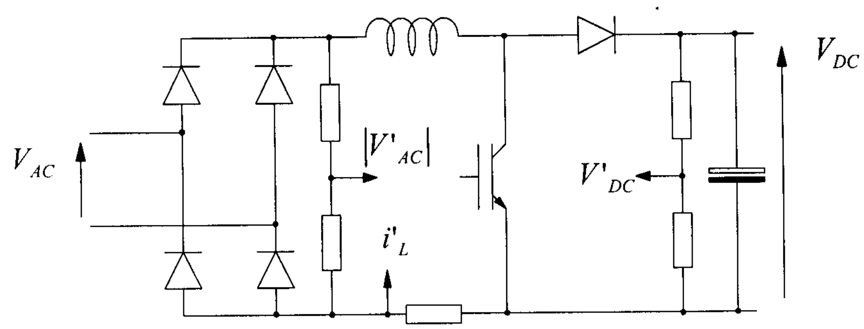
(iv) Sketch the frequency spectrum of the AC current and describe its features [2]



The spectrum consists of a line frequency term and a series of low order harmonics. Only odd harmonic swill exist because of the symmetry of the waveform.

(c) For a single-phase AC to DC converter using a boost switch-mode circuit:

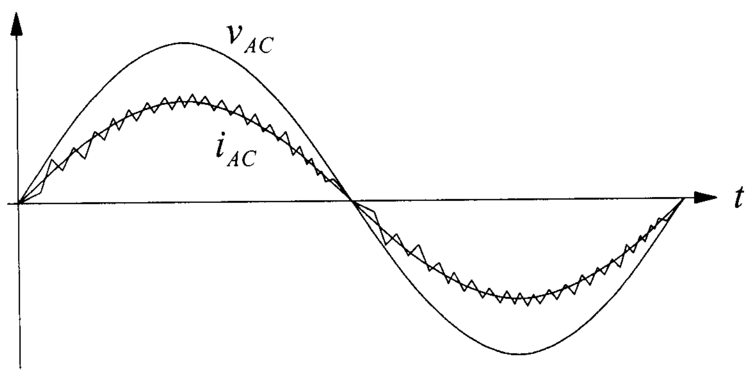
(i) Sketch the circuit diagram of the circuit [2]



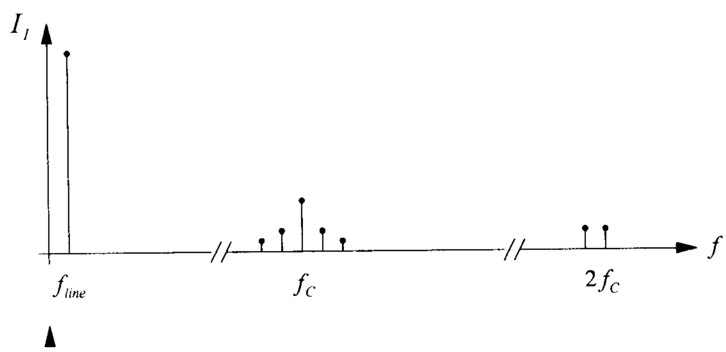
(ii) Describe its operation and in particular describe how the signals to control the switch is obtained [2]

The error between the DC voltage and its reference point is used to set the magnitude of the input current required. This magnitude is multiplied by a sinusoidal shape to form an instantaneous current reference. The current error(multiplied by some gain) is used with a pulse width modulator (triangle wave comparison) to form a switching signal.

(iii) Sketch the AC current waveform in the time domain [1]



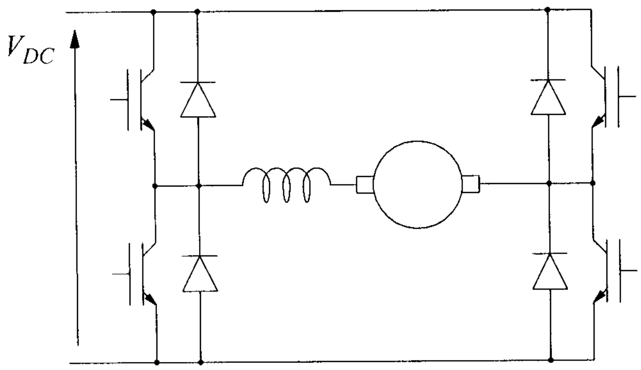
(iv) Sketch the frequency spectrum of the AC current and describe its features [2]



The spectrum will have a dominant line frequency term and a series of carrier and side-band terms at multiples of the switching frequency. Because of the inductive circuit and the large frequency separation, the carrier terms are of low amplitude.

4.

(a) Sketch a circuit diagram of a DC to DC converter suitable for running a DC machine in all 4 quadrants of the torque-speed plane. [2]



(b) Derive an equation relating the torque produced by a DC machine to its speed [3]

$$T = k_A \phi I_A$$

$$= k_A \phi \left(\frac{V_A - E}{R_A} \right)$$

$$= \frac{k_A \phi}{R_A} \left(V_A - k_A \phi \omega \right)$$

(c) Figure Q4 shows the typical limits of operation of a DC machine in terms of torque and speed. Explain why the limits have this shape [4]

- *Torque is proportional to current and flux*
- *Flux is held at its maximum value at low speed (below base speed, forwards or reverse)*
- *Torque is therefore limited by maximum current (independent of speed) and so a flat torque limit is observed.*
- *Speed is varied through voltage. Above some speed (base speed), the back-EMF would be greater than the maximum applied voltage if the flux were maintained constant. In this case, motoring operation could not be achieved.*
- *Above base speed the flux is reduced progressively (field weakening) to achieve higher speed.*
- *Because torque is proportional to flux, the torque limit reduces in inverse proportion to the speed.*

(d) A particular machine has the following properties:

Maximum DC input voltage 100 V

Armature resistance 0.5 Ω

Field flux at maximum field current 18 mWb

Armature constant 12.5 V.s.rad^{-1}.Wb^{-1} (or N.m.A^{-1}.Wb^{-1})

Rated armature current 8 A

(i) Calculate the difference in speed between the no load speed and the speed when the maximum armature current is being drawn at maximum field current. [2]

$$\Delta\omega = \frac{I^{\max} R_A}{k_A \phi} = \frac{8 \times 0.5}{12.5 \times 0.018} = 17.77\, rad/s \quad (= 169.8 \quad r.p.m.)$$

(ii) Calculate the maximum speed the machine can achieve under full load with maximum field current. [3]

$$\omega_{NL} = \frac{V_A}{k_A\phi} = \frac{100}{12.5 \times 0.018} = 444.4 \quad rad/s \quad (= 4{,}244\ r.p.m.)$$

$$\omega = \omega_{NL} - \Delta\omega = 426.67 \quad rad/s \quad (= 4{,}074\ r.p.m.)$$

(iii) Calculate the maximum speed the machine can achieve under full load with field current at half of its maximum value [3]

Both the no-load speed and speed droop will double if the flux halves.

(iv) Compare the torque and power available under the conditions under parts (ii) and (iii) [3]

The torque will halve and the power (half the torque times twice the speed) will remain constant

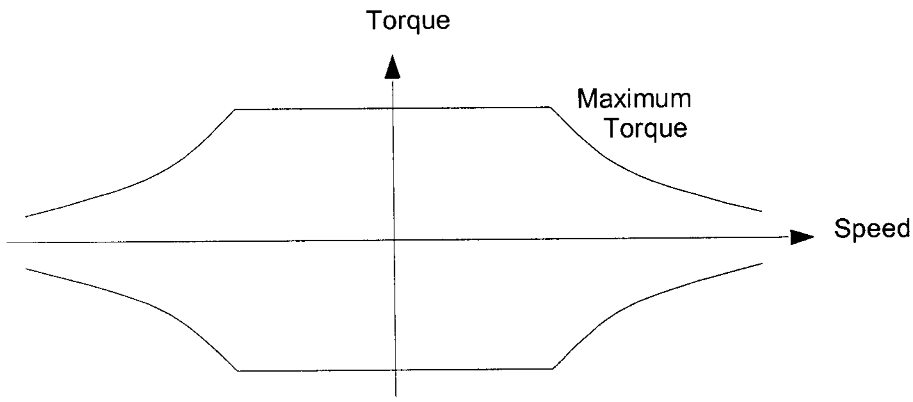
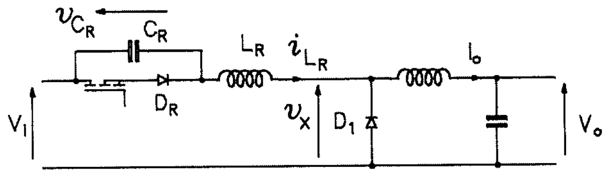


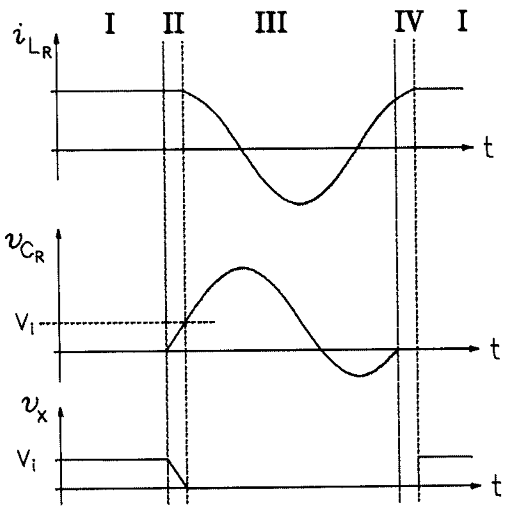
Figure Q4

5. Figure Q5 shows a Zero-voltage switched (ZVS) quasi resonant converter. The operation of the circuit occurs in four stages:

I	MOSFET on
II	MOSFET off; C_R pre-charging
III	C_R and L_R in resonance; MOSFET not conducting
IV	MOSFET on; L_R discharging

(a) Sketch the shape of the waveforms of i_{LR} and v_{CR} [6]





(b) Describe the conditions under which the MOSFET is turned on and turn off in terms of the drain current and drain-source voltage that exists during the switching action and explain why this leads to low power loss during switching. [6]

At turn-off.

The capacitor C_R across the Mosfet (and diode)is initially discharged. It charges (relatively slowly) as current diverts out of the Mosfet. The drain-source voltage is thus held low during turn-off and the turn off loss is low.

At turn-on

The voltage across C_R is negative in the latter phase of the resonant cycle. At this time diode D_R is reverse biased and supports the negative voltage leaving zero voltage across the drain-source. The Mosfet can be turned on with zero power loss.

(c) Resonant action is governed by the equations:

$$i_{L_R} = I_o \cos(\omega_R t)$$

$$v_{C_R} = V_I + \frac{I_O}{\omega_R C_R} \sin(\omega_R t)$$

For a conversion of 12 V to 5 V with an output current of 5 A; choose values of L_R and C_R such that the circuit as a whole operates with a period of 2 μs. [8]

Must ensure period of negative voltage, i.e.,

$$\frac{I_O}{\omega_R C_R} > V_I$$

$$I_O\sqrt{\frac{L_R}{C_R}} > V_I$$

Ratio of resonant period to cycle period is set by voltage ratio. The resonant period is the off-time.

$$\frac{V_O}{V_I} = 1 - \frac{T_R}{T}$$

$$T_R = T\left(1 - \frac{V_O}{V_I}\right) = 2\times10^{-6}\times\left(1-\frac{5}{12}\right) = 1.167\,\mu s$$

$$\frac{T_R I_O}{2\pi V_I} > C_R$$

$$C_R < \frac{1.167\times10^{-6}\times5}{2\pi\times12} < 77\,nF$$

So, choose 47 nF to provide safety margin

$$L_R = \frac{T_R^{\ 2}}{4\pi^2 C_R} = 734\ \text{nH}$$

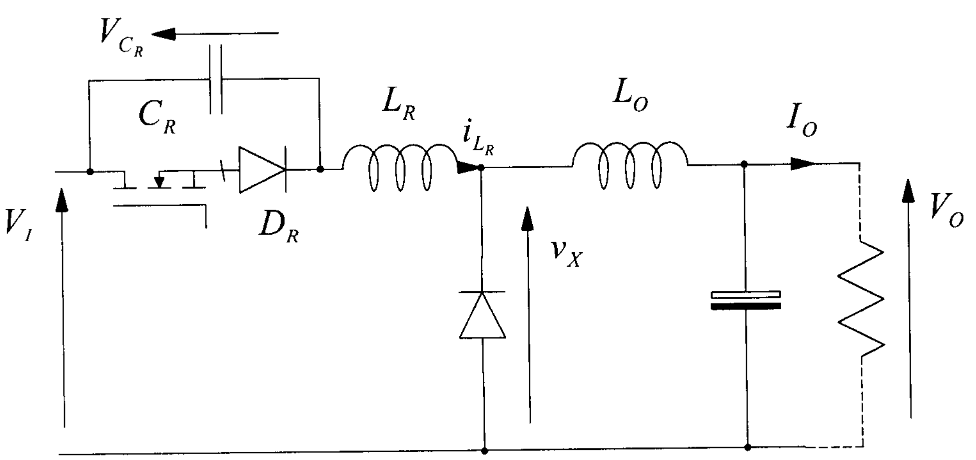


Figure Q5

6.

(a) Uninterruptable power supplies, UPS are installed by electricity consumers to overcome power quality problems. Discuss the range of problems that a UPS can solve and state any limitations that the design of the UPS may place on its effectiveness. [8]

The prime problem that a UPS will overcome is a power outage, i.e., a loss of supply for a matter of minutes. During the supply loss the UPS will supply loads by taking energy from a local store (battery) or a local generator or both. An off-line UPS is only active during a power outage and is bypassed by a switch when the utility company supply is available.

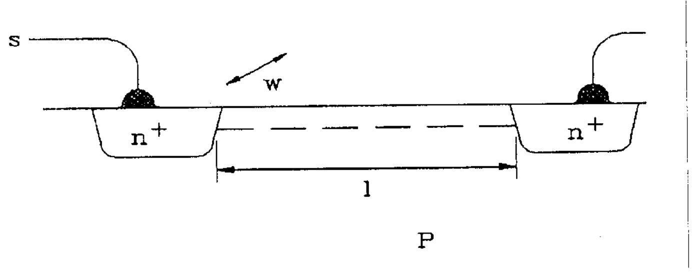
An on-line UPS is active at all times. It rectifies the utility company supply and re-inverts it to AC to supply the load. It is able to provide continuity of supply through even very short interruptions to the supply. It is also able to:

- *Correct voltage sag and swell*
- *Correct frequency drift*
- *Correct distorted voltage wave-shape*
- *Suppress voltage dips and spikes*
- *Filter hf noise*

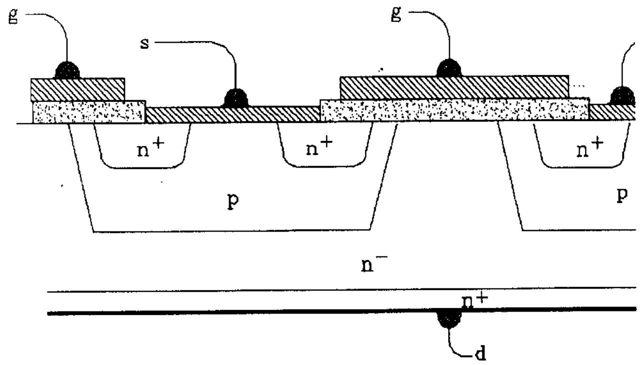
If the on-line UPS internal rectifier is a sine-wave current design the UPS will draw sine-wave current from the utility supply even if the loads are distorting (diode rectifiers).

(b) Explain why a double diffused vertical structure is used for high voltage, high current MOSFETs in place of the lateral structure adopted for general purpose MOSFETs. Sketch the structure of both devices. [8]

A lateral Mosfet has a lightly doped body between to highly doped contact regions. In the off-state, the depletion region (of the blocking drain-body junction) will grow deep into the body. The drain-source separation (l) must be large to avoid punch-through in voltage blocking. However, in the on-state it would be desirable to have a low value of l to obtain a low $R_{DS(On)}$.



To break this trade-off the off-state depletion layer must grow in the drain not the body and therefore a large lightly doped drain is required. This is achieve through a double-diffused vertical structure.



The channel is a short (horizontal) path through the p-well between the source diffusion and the drain epitaxi and so the $R_{DS(on)}$ is low. The drain is deep and punch-through is avoided.

(c) Describe how and why the double diffused MOSFET structure is modified to form an IGBT (Insulated-gate bipolar transistor) [4]

The deep, lightly doped drain region is significantly resistive and this resistance can come to dominate over the channel resistance in high voltage devices. The resistivity of the drain can be reduced by high-level injection (conductivity modulation) by adding a forward biased junction to flood the drain with carriers. This requires that the n+ contact region at the edge of the drain is changed to p+