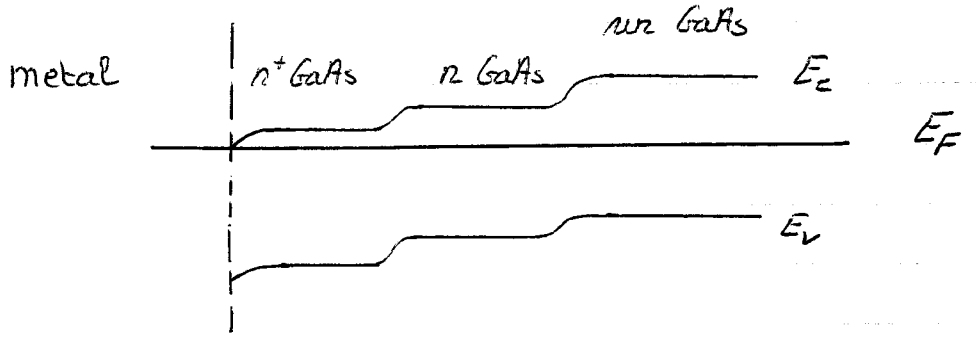
Advanced Electronic Devices - 2003 Answers

1. a) (GaAs) MESFET (Metal Semiconductor Field Effect Transistor)

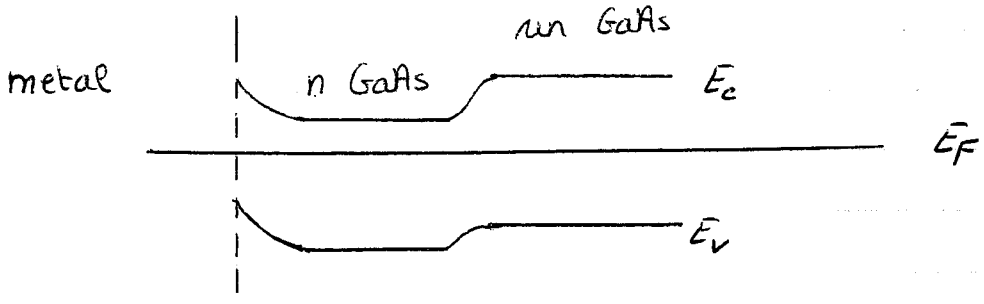
b) n - GaAs layer

c) Gate recess allows to reduce the contact resistance of the source & drain by the thick n^+ GaAs layer, while keeping the required threshold voltage.

d) (i) Ohmic contact



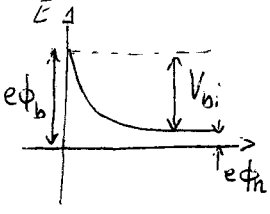
(ii) Schottky contact



e) For depletion mode operation in n-channel device, the value of the threshold voltage $V_{th} \leq 0$. At $V_{th} = 0$ channel just depleted $\Rightarrow$ a_{min} (minimum channel width).

Expression of threshold voltage :

$$V_{th} = V_{bi} - \frac{e N_D a^2}{2 \varepsilon_0 \varepsilon_s}$$



$$V_{th} = (\phi_b - \phi_n) - \frac{e N_D a^2}{2 \varepsilon_0 \varepsilon_s}$$

$$V_{th} = 0 \Rightarrow a_{min}^2 = \frac{2(\phi_b - \phi_n) \varepsilon_0 \varepsilon_s}{e N_D}$$

Page 1 of 10

$$\phi_n = \frac{E_c - E_F}{e}$$

$$n \cong N_c \exp\left[\frac{-E_c + E_F}{kT}\right]$$

$$\Rightarrow \frac{E_c - E_F}{e} = \frac{kT}{e} \ln\left[\frac{N_c}{n}\right] \cong \frac{kT}{e} \ln\left[\frac{N_c}{N_D}\right]$$

$$\begin{cases} \phi_n = kT/e \ln\left[\frac{N_c}{N_D}\right] \\ \phi_b = \phi_m - \chi_s \end{cases}$$

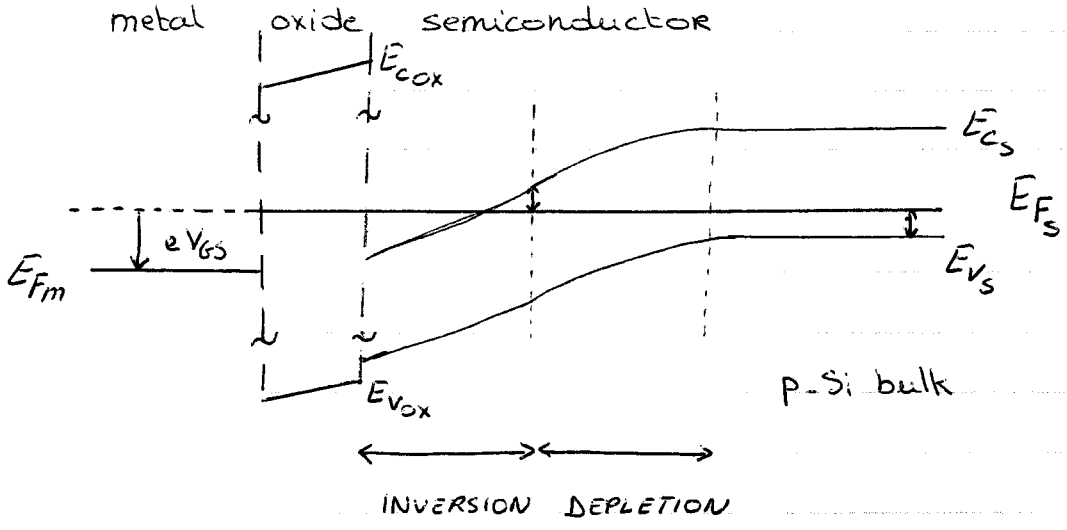
$$\begin{cases} \phi_n = 0.026 \ln\left[\frac{4.7\ 10^{17}\ cm^{-3}}{10^{17}\ cm^{-3}}\right] = 0.04\ V \\ \phi_b = 3.57 - 3.05 = 0.52\ V \end{cases}$$

$$a_{min} = \sqrt{\frac{2 \cdot 0.52\ V\ 8.85\ 10^{-14}\ \frac{F}{cm} \cdot 10}{1.6\ 10^{-19}\ C\ \ 10^{17}\ cm^{-3}}}$$

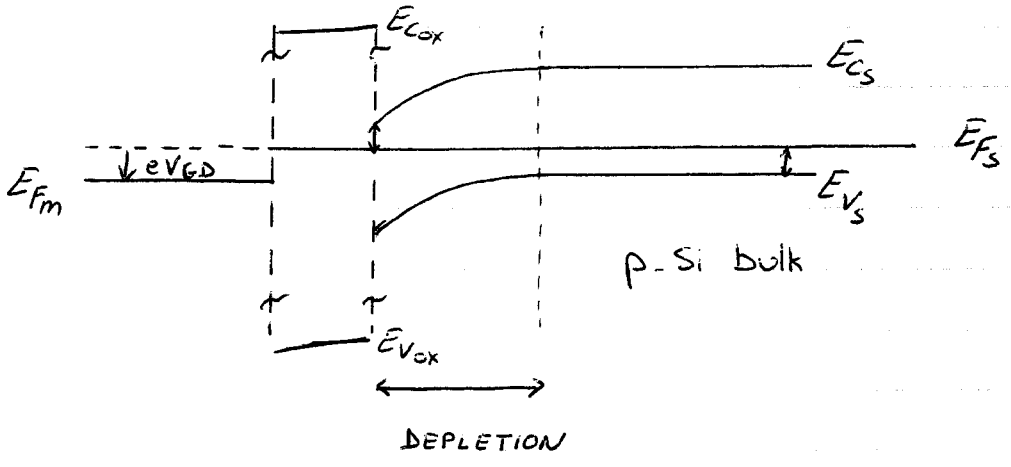
$$a_{min} \cong 7.59\ 10^{-6}\ cm = 75.9\ nm$$

2. a) by dry thermal oxidation in oxygen atmosphere
b) to ensure good ohmic contact (low contact Resistance.

c) (i) at source side



(ii) at drain side (Note: pinch-off @ drain side)



d) Velocity saturation will occur before the voltage V_{DS} is equal to $V_{DS} = V_{GS} - V_{th}$. This results in:

1°) Saturation of the current I_{DS} will happen @ V_{DS} values lower than $V_{DS} = V_{GS} - V_{th}$ for pinch-off

2°) The current I_{DS} will be lower for the same V_{DS} value

e) For $V_{DS} = 2V > V_{GS} - V_T = 2 - 1 = 1V$

$\Rightarrow$ saturation.

$$I_{DS} = \frac{\mu_e W C_{ox}}{L}\left[(V_{GS} - V_{th})\, V_{DS} - \frac{V_{DS}^2}{2}\right]$$

In saturation $V_{DS} = V_{GS} - V_{th}$

$$I_{DS}^{sat} = \frac{\mu_e W C_{ox}}{2L}\left[(V_{GS} - V_{th})^2\right]$$

Intrinsic transconductance

$$g_m^{int} = \frac{d I_{DS}^{sat}}{d V_{GS}} = \frac{\mu_e W C_{ox}}{L}(V_{GS} - V_{th})$$

Extrinsic transconductance is caused by voltage drop across R_S : $I_{DS} R_S$

$$\Rightarrow V_{GS}^{applied} = V_{GS}^{int} + R_S \cdot I_{DS}$$

$$\frac{d V_{GS}^{appl}}{d I_{DS}} = \frac{d V_{GS}^{int}}{d I_{DS}} + R_S$$

$$\frac{1}{g_m^{ext}} = \frac{1}{g_m^{int}} + R_S$$

$$g_m^{ext} = \frac{g_m^{int}}{1 + g_m^{int} \cdot R_S}$$

$$\Rightarrow g_m^{ext} = \frac{\mu_e W C_{ox}(V_{GS} - V_{th})}{L\left(1 + \frac{\mu_e W C_{ox}}{L}(V_{GS} - V_{th})\right)}$$

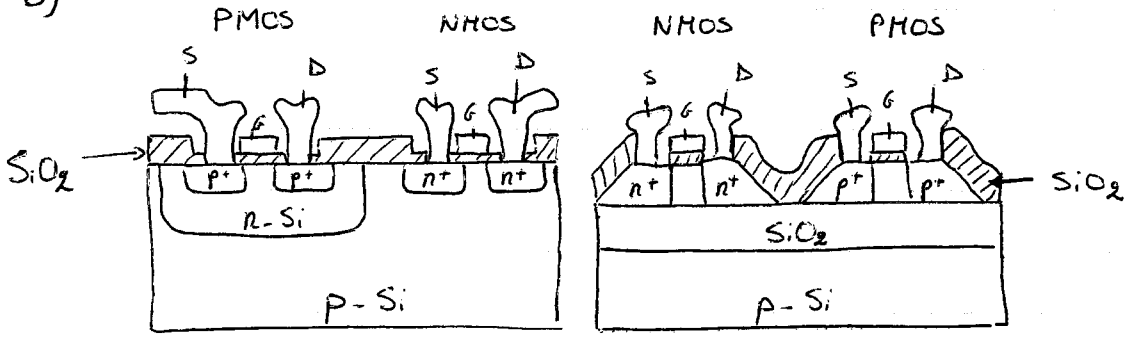
$$g_m^{int} = \frac{500 \cdot 50\,10^{-4}\; 8.85\,10^{-14} \cdot 4 \cdot 1}{2\,10^{-4}\quad 10\,10^{-7}}$$

$C_{ox} = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}}$ $\quad g_m^{int} = 0.0044\ S$

$$g_m^{ext} = \frac{0.0044}{1 + 0.0044\ 100} = 0.0031\ S$$

3. a) SIMOX allow a good control of the thickness of the Si film on top of the buried oxide.

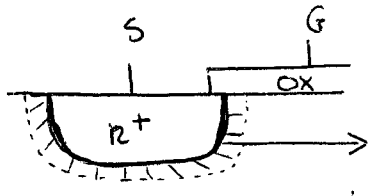
b)



Si - bulk SOI

c) * Parasitic capacitances due to the ohmic contacts (S & D)

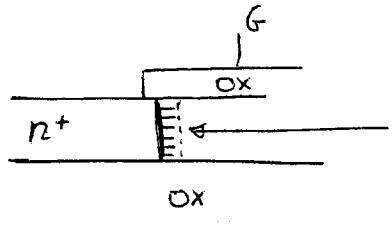
in bulk-Si



— indicates the capacitor area.

p-bulk A_{bulk}

in SOI



— indicates the capacitor area A_{SOI}

SOI

$A_{SOI} < A_{bulk}$

Since $C \propto A$.

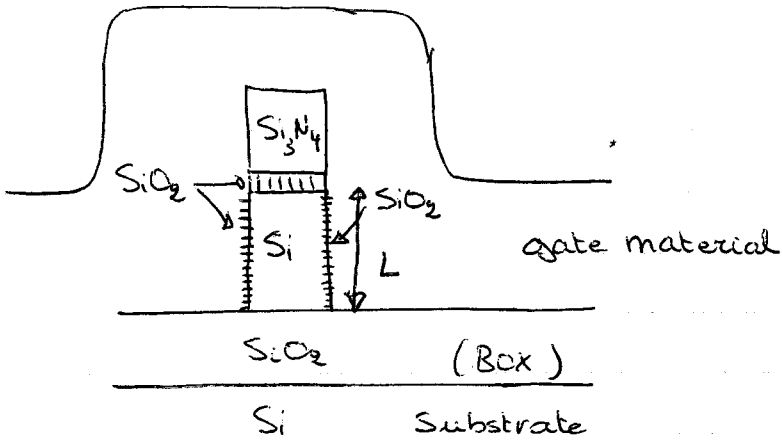
$C_{SOI} < C_{bulk}$

* The capacitance C_{ds} in the bulk is non-existant in SOI.

d) Because leakage current paths via the substrate are non-existent in SOI.

e) (i) 8

(ii)



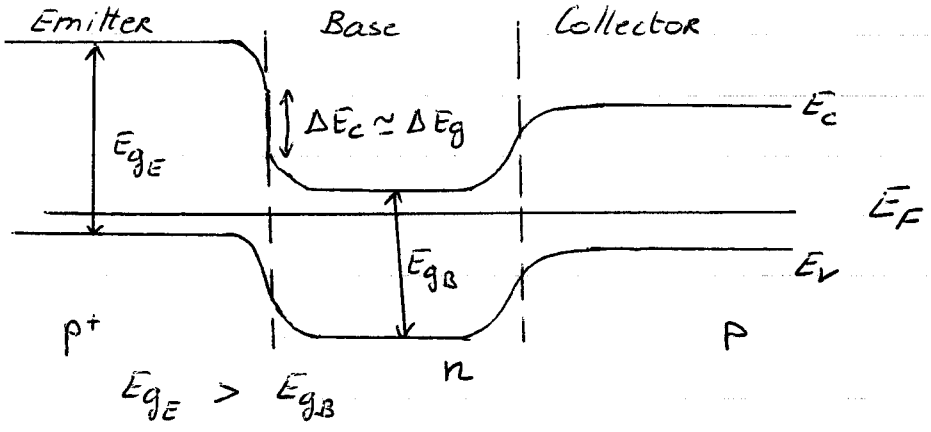
L = gatelength (= height of fin)

(iii) If the width of the fin is sufficiently small, a fully depleted structure results, then no charge redistributions can occur in the undepleted parts of the fin which might influence the threshold voltage. If the width of the fin is narrow, a better gate control results.

4. a) A composition gradient in the base adds drift to the usual diffusion current only => the transit time through the base reduces, therefore cut-off frequency increases.

b) The gain of a bipolar transistor is limited by the amount of carriers (holes in an npn transistor) flowing out of the base into the emitter. In an HBT the potential barrier in the valence band is larger than in a BJT. Therefore the emitter injection efficiency in an HBT is larger than in a BJT and thus also the gain.

c)



d) Emitter current crowding. Due to the voltage drop in the base region, the voltage at the centre of the emitter contact is smaller than at the edge. This means that the current will mainly flow the edge of the emitter.

e) $$\beta_{BJT} = \frac{\mu_e L_E N_{D_E}}{\mu_B W_B N_{A_B}}$$

$$\beta_{HBT} = \beta_{BJT} \exp\left(\frac{\Delta E_g}{kT}\right)$$

1°) $\exp\left(\frac{\Delta E_g}{kT}\right) = 10 \Rightarrow \beta_{BJT} = 50$

$$\frac{2\ 10^{-4}\ 10^{18}}{W_B N_{AB}} = 50 \Rightarrow W_B N_{AB} = 4\ 10^{12}\ cm^{-2}$$

Diffusion capacitance :

$$C_{diff} \propto W_b^2$$
$$C_{diff} \propto I_e$$

$\Rightarrow$ general expression : $C_{diff} = C_0 W_b^2 . I_e$

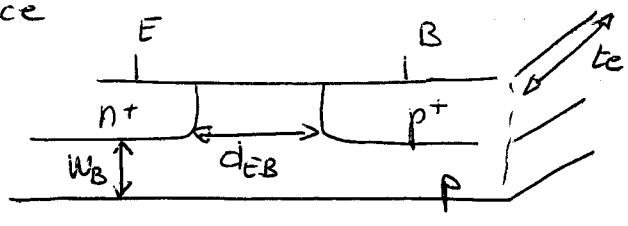
$$\Rightarrow \begin{cases} 8\ 10^{-12}\ F = C_0\ W_b^2\ 10^{-2}\ A \\ 4\ 10^{-12}\ F = C_0\ W_b^2\ 5\ 10^{-3}\ A \end{cases}$$

$$\Rightarrow \begin{cases} \boxed{W_b \simeq 1\ \mu m} \\ C_0 \simeq 0.08 \end{cases}$$ Base width

$$W_b \cdot N_{AB} = 4\ 10^{12}\ cm^{-2}$$
$$N_{AB} = \frac{4\ 10^{12}\ cm^{-2}}{10^{-4}\ cm} = 4\ 10^{16}\ cm^{-3}$$

$$\boxed{N_{AB} = 4\ 10^{16}\ cm^{-3}}$$ Base doping

Base spreading resistance



$$r_{bb} \simeq \frac{\rho_{base}\ d_{EB}}{W_B .\ te}$$

$$\rho_{base} = \frac{1}{\sigma_{base}} \simeq \frac{1}{\sigma_e} = \frac{1}{e\ N_{AB}\ \mu_e}$$

$$r_{b'b} = \frac{d_{EB}}{e\ N_{AB}\ W_B\ \mu_e\ te} = \frac{2\ 10^{-4}}{1.6\ 10^{-19}\ 4\ 10^{12}\ 500\ 10^{-2}} = 62.5\ \Omega$$

$$\boxed{r_{b'b} = 62.5\ \Omega}$$

5. (a) portable applications (e.g. computers, mobile phones) work on batteries and need low power consuming circuits. In sub-threshold : currents & voltages are small

(b) Because below threshold, diffusion currents become important. These diffusion currents are due to charge gradients along the channel.

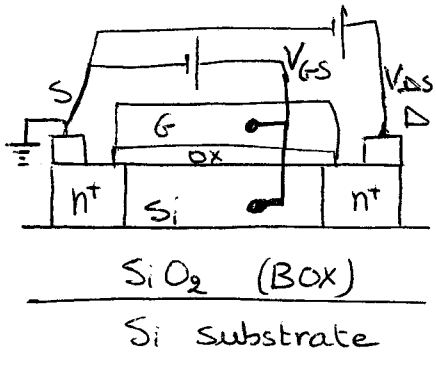
(c) The sub-threshold voltage swing is the maximum gate voltage swing for which the log I_{DS} in sub-threshold is linear.

(d) Because off-current are lower in SOI

(e) In sub-threshold operation the mobility of the carriers is decreasing, degrading the FET performance. The carrier mobility in buried channel Si:SiGe FETs is
1°] higher for all V_{GS} compared to Si FETs
2°] the degradation of the carrier mobility in subthreshold is less fast than for the Si FETs

(f) DTMOS

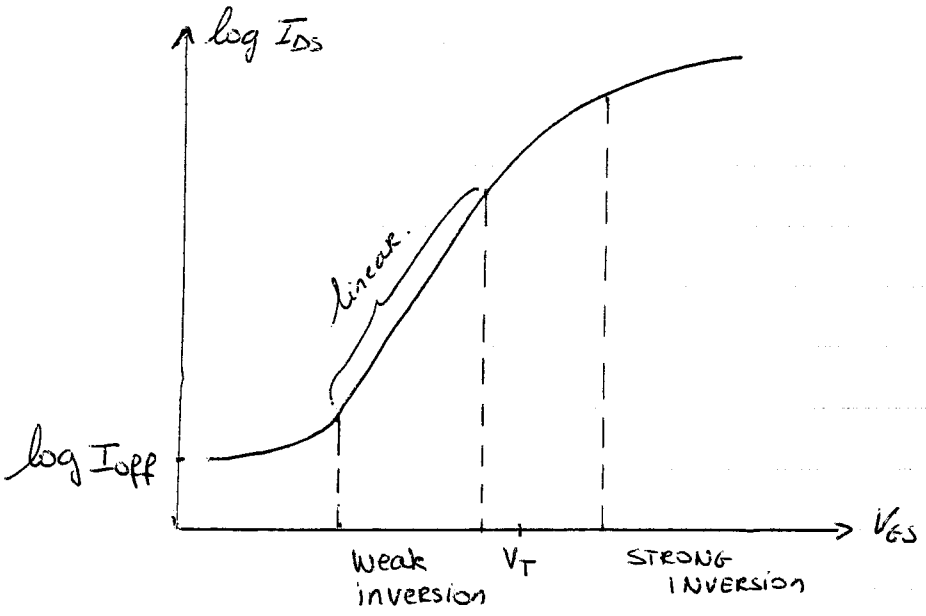
(i)



→ the gate is tied to the bulk

(ii) In this device the threshold voltage is a function of the gate voltage. As the gate voltage increases the threshold voltage drops resulting in a higher current drive for low supply voltages. On the other hand, V_T is high at $V_{GS} = 0$, therefore leakage current is low.
The sub-threshold swing reaches its ideal value.

(g)


log I_{DS}
linear
log I_{off}
V_{GS}
Weak inversion
V_T
STRONG INVERSION