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Isc 3.19

IMPERIAL COLLEGE OF SCIENCE TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
M.Eng., B.Eng., B.Sc(Eng.) and A.C.G.I. EXAMINATIONS 2003

PART III and PART IV

**DIGITAL SYSTEM DESIGN**

# SOLUTIONS

**First Marker:** *PYKC*

**Second Marker:** *DMB*

**Answer to Question 1**

a)

$$\sum_{i=0}^{N-1} 2^i(-x_i + x_{i-1})$$

$$= \sum_{i=0}^{N-1} -2^i x_i + \sum_{i=0}^{N-1} 2^i x_{i-1}$$

$$= -\sum_{i=0}^{N-1} 2^i x_i + \sum_{i=-1}^{N-2} 2^{i+1} x_i$$

$$= -2^{N-1} x_{N-1} - \sum_{i=0}^{N-2} 2^i x_i + \sum_{i=0}^{N-2} 2 * 2^i x_i$$

$$= -2^{N-1} x_{N-1} + \sum_{i=0}^{N-2} 2^i x_i$$

which is the two's complement representation of a binary number.

Consider bit $i$ & $(i+1)$ together:-

$$2^i(-x_i + x_{i-1}) + 2^{i+1}(-x_{i+1} + x_i)$$

$$= 2^i(-2x_{i+1} + x_i + x_{i-1})$$

Therefore, the two's complement number becomes (assuming that N is even):

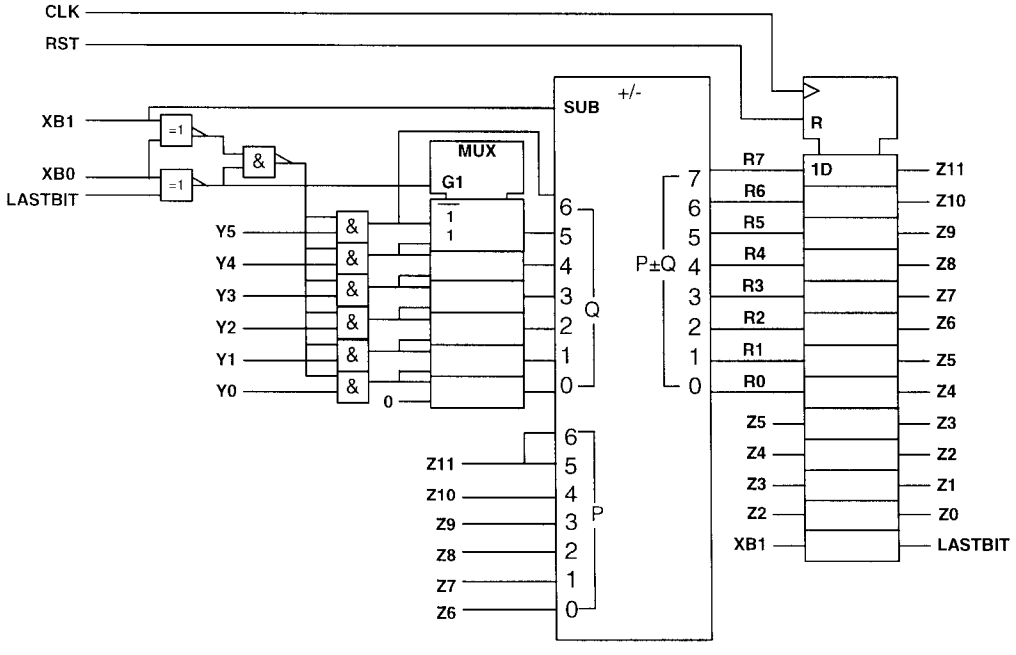
$$\sum_{i=0,2,4,\ldots}^{N-2} 2^i(-2x_{i+1} + x_i + x_{i-1})$$

where $i=2j$.

$$= \sum_{j=0}^{N/2-1} 2^{2j}(-2x_{2j+1} + x_{2j} + x_{2j-1})$$

[5]

b) This is a standard modified booth multiplier that takes three cycles to multiply two 6-bit numbers..




[12]

c) Assuming the +/- block consists of 8-bit adder with a MUX and inverter on the Q-input path, the worst case delay is 7+2 = 9ns.

Worst case path: LASTBIT: XOR+2 gates + MUX + add/sub + setup time + register output delay

Worst case delay : 2+2+1+9+1+2 = 17 ns. Therefore max frequency = 58.8 MHz.

(This will vary depending on student's circuit.)

[3]

**Answer to Question 2** (Mostly bookwork)

a) .

Modern electronic systems have high density PCB with surface mount components. Impossible to get at any pins of devices. Therefore testing becomes very difficult if not impossible. JTAG boundary scan provides a means of accessing both the internal circuits on components as well as external circuit outside the components.

Students should explain how JTAG actually work. .....

JTAG test configuration includes EXTEST for testing external devices. Test patterns can be strobed serially into the JTAG compliant device to drive external interconnect to 1 or 0. Another JTAG compliant device would act as 'receiver' and parallel load the pattern. This is then strobed out and compare to expected pattern.

[7]

b)

Metastability can occur in any synchronous system interfacing to one or more asynchronous input. Since the input signal is not synchronised to the system clock, it may violate the setup or hold time of the synchronous system. Metastability may be reduced by a synchronizer circuit using one or more D-FF connected in series.

[3]

c) Cause of ground bounce:

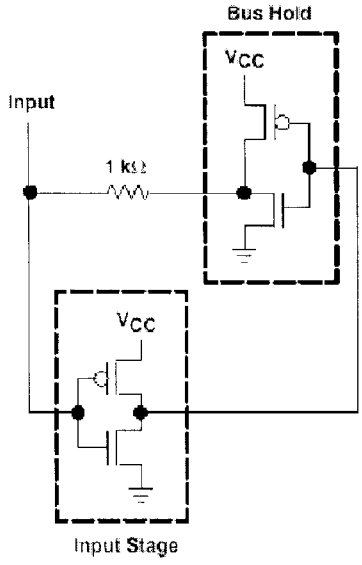
- Ground Bounce is a voltage oscillation between the ground pin on a component package and the ground reference level on the component die.
- Ground Bounce is one of the primary causes of false switching in high speed components and is a major cause of poor signal quality.
- It is caused by a current surge passing through the lead inductance of the package.
- The effect is most pronounced when all outputs switch simultaneously, (hence the alternate name, Simultaneous Switching Noise).
- While the inductance is the combined effect of the package lead, the package lead frame, the bond wire and the inductance in the die pad, most of the inductance is caused by the bond wire.

Ground Bounce effect can be reduced by:

1. Using all Vcc/Gnd pins available
2. Avoid pullup/pulldown resistors (i.e. use bus hold circuit)
3. Possibly use series damping resistors
4. Control output slew rate
5. Extra care in holding clock signals to solid voltage level (Vh) and fast clock transistions

[5]

d) The schematic for a bus-hold circuit is:

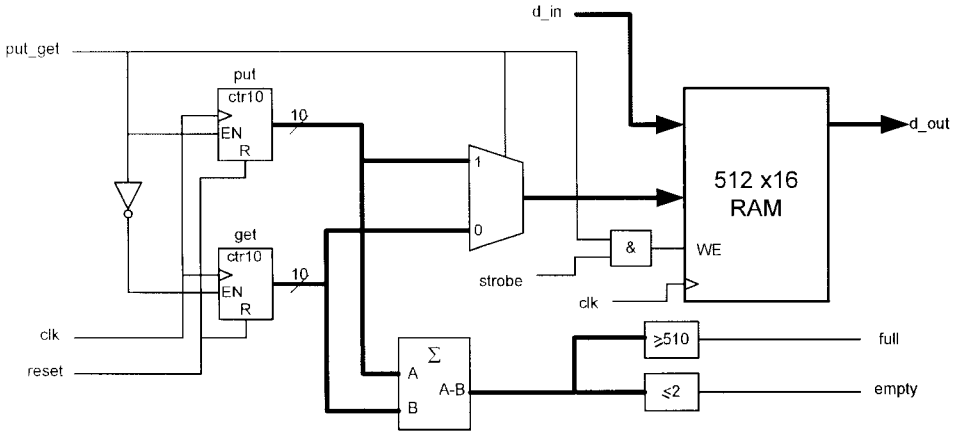



- Bus-hold circuits are used to help solve the floating-input problem and eliminate the need for pullup and pulldown resistors.
- Bus-hold circuits consist of two back-to-back inverters with the output fed back to the input through a resistor.
- To understand how the bus-hold circuit operates, assume that an active driver has switched the line to a high level. This results in no current flowing through the feedback circuit.
- Now, the driver goes to the high-impedance state and the bus-hold circuit holds the high level through the feedback resistor.
- The current requirement of the bus-hold circuit is determined only by the leakage current of the circuit.
- The same condition applies when the bus is in the low state and then goes inactive.

[5]

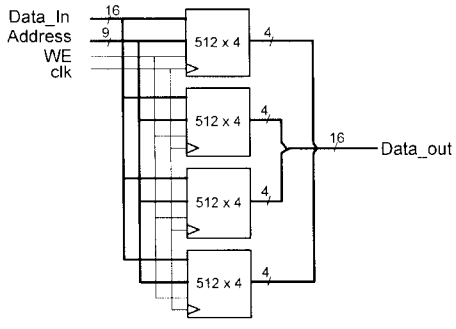
**Answer to Question 3**

a)




[10]

b) (i)




[4]

(ii)

| Component | Resources |
|---|---|
| Memory | 4 EABs |
| Put Counter | 10 LEs |
| Get Counter | 10 LEs |
| Subtractor | 10 LEs |
| MUX | 9 LEs |
| <= 2 circuit | 3 LEs |
| >=510 circuit | 3 LEs |
| AND gate | 1 LEs |
| **Total** | **4 EABs, 46 LEs** |

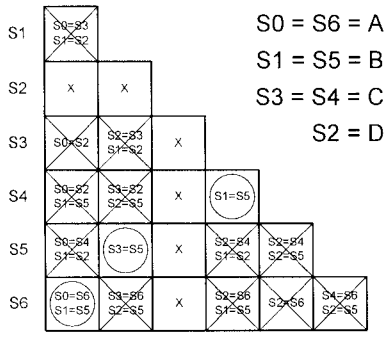
[4]

(iii) With a register at the output, data will be available for reading from the FIFO until the next FIFO read operation. This provides far better flexibility in the read time available for external circuits and more predictable timing (since it is relative to a clock edge).

[2]

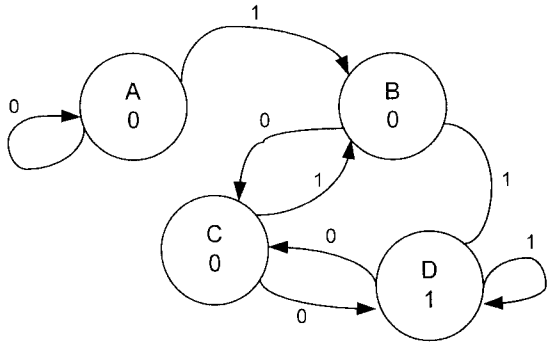
**Answer to Question 4**

a)




[10]

b)




[3]

c)

| Q3 | Q2 | Q1 | Q0 | X | D3 | D2 | D1 | D0 | Y |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

D0 = Q0 & !X

D1 = Q0 & X + Q2 & X

D2 = Q1 & !X + Q3 & !X

D3 = Q1 & X + Q2 & !X + Q3 & X

Y = Q3

[4]

d) This recognises

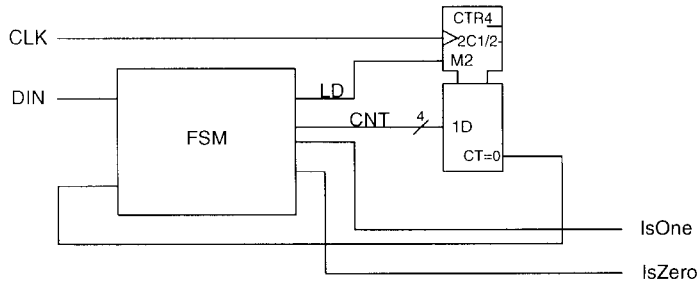
(i) two or more ones,

(ii) a 1 followed by an even number of 0s,

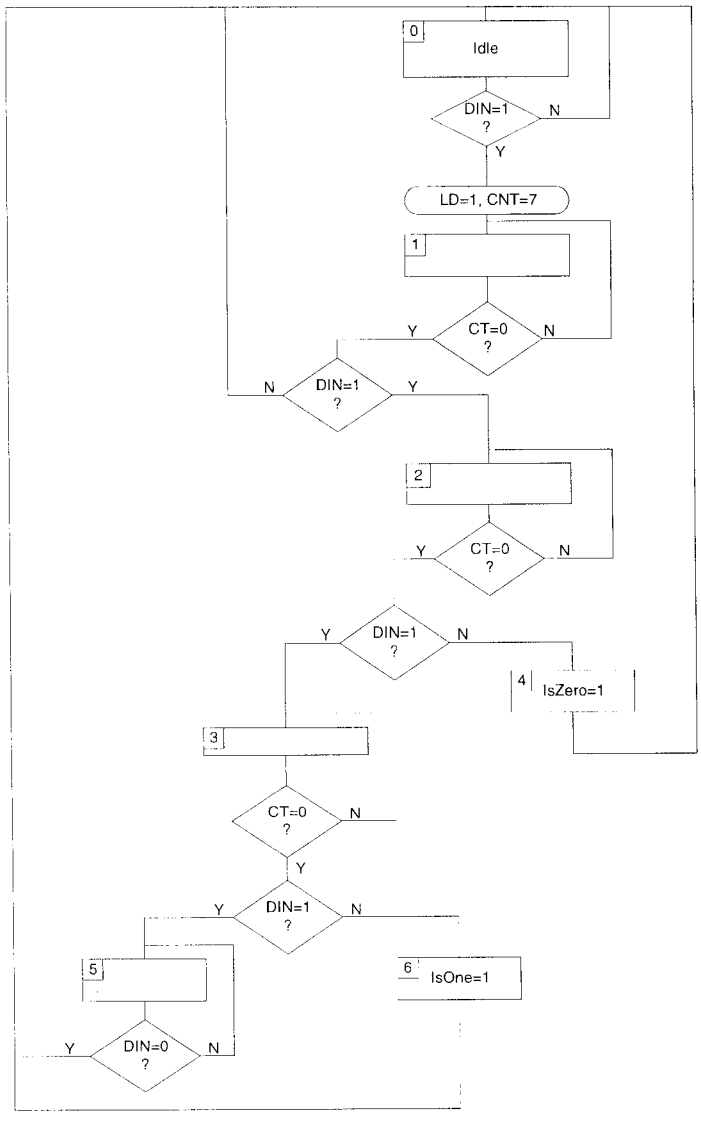
(iii) a 1 followed by an even number of 0s followed by a 1.

[4]

**Answer to Question 5**




[5]




[15]

**Answer to Question 6**

(a)

$$\overline{ROMEN} = \overline{\overline{A15} \bullet RD}$$

$$\overline{RAMEN} = \overline{\overline{A12} \bullet A15 \bullet (RD + WR)}$$

$$\overline{FRAMEN} = \overline{A12 \bullet A13 \bullet A14 \bullet A15 \bullet (RD + WR)}$$

[4]

(b)

Available access time from address to data = 2*A + n_wait*A - B - F

= 2*15.2 + n_wait*15.2 - 5 - 3

= 22.4 + n_wait * 15.2

Access from EN to data = 1.5 * A - C - $t_{decode}$ - F + A * n_wait

= 1.5 * 15.2 - 5 - 5 - 3 + 15.2 * n_wait

= 9.8 + 15.2 * n_wait

Therefore:

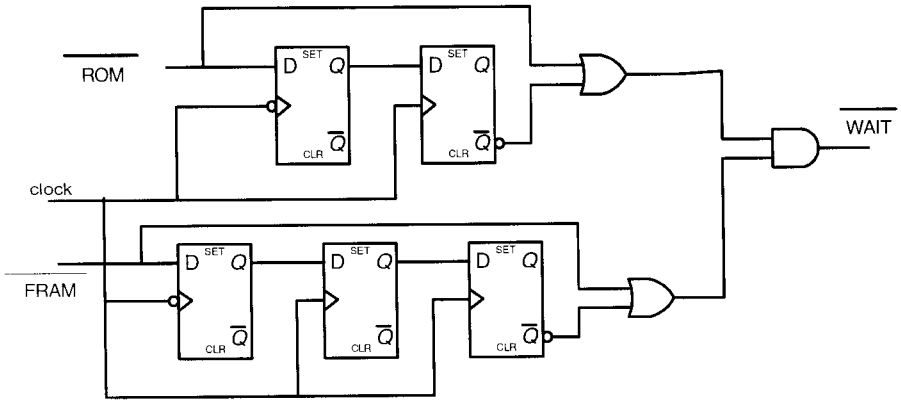
ROM : 1 wait state

RAM: 0 wait state

FRAM: 2 wait states

[6]

(c) One possible solution based on D-FF as delay elements:



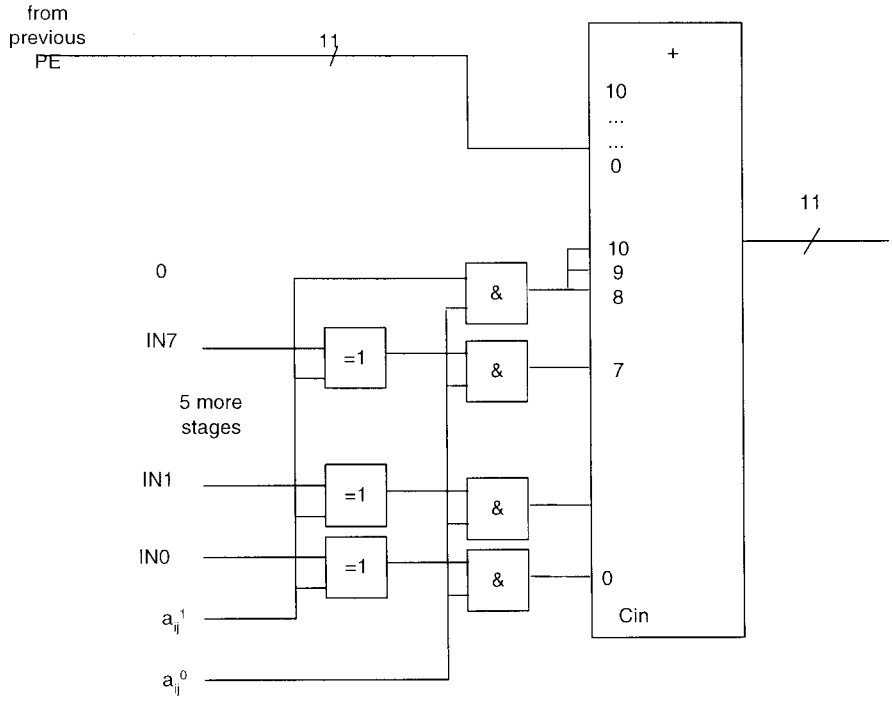

[10]

**Answer to Question 7**

a) The range of $X_j$, $Y_j$ and $Z_j$ is -765 to +765, hence need 11-bits.

[4]

b)




$F$, $G$, $H$ are all zero.

[12]

c) minimum period = tcq + 2*tgate + 3*tadder + tsu

= (1+2+15+1) ns

= 18 ns

Max frequency = 55.6 MHz.

[4]