IMPERIAL COLLEGE OF SCIENCE TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
M.Eng., B.Eng., B.Sc(Eng.) and A.C.G.I. EXAMINATIONS 2000

PART III and PART IV

DIGITAL SYSTEM DESIGN

There are **SEVEN** Questions.

Answer **FOUR** questions.

First Marker: **P.Y.K. Cheung**

Second Marker: **D.M. Brookes**

Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least significant bit of a bus signal is labelled as bit 0, and the most significant bit with the highest integer number. Therefore the signal X7:0 is an eight bit bus with X7 being the MSB and X0 the LSB.

In questions involving circuit design, you may use any standard digital circuits that are not explicitly forbidden by the question provided that you fully specify their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

1. Design a circuit to produce an output pulse on OUT lasting 256 clock cycles when a positive edge is detected on the asynchronous input IN as shown in *Figure 1*. IN is guaranteed not to produce another positive edge when OUT is high. You may assume that the signal IN does not change near to a CLOCK rising edge.

[12 marks]

Modify the design to allow the length of the output pulse to be changed between 2 and 256 clock inclusive using an 8-bit control input. The output pulse length is required to be N clock periods where 2 N 256, and the 8-bit control input is set to the binary representation of (N-1). Assume that this 8-bit control input is stable just before the positive edge on IN and that is remains unchanged during the entire time that OUT is high.

[8 marks]

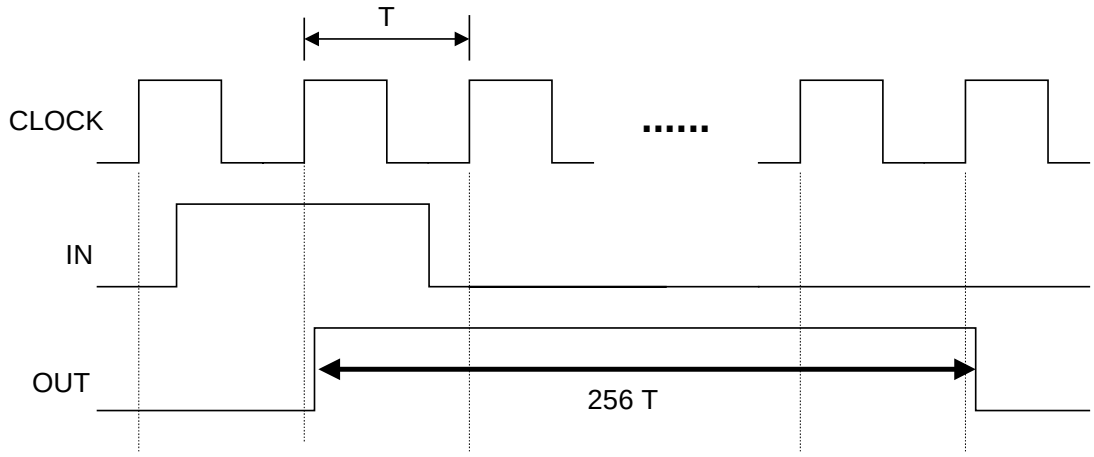


Figure 1

2. *Figure 2* shows the state transition diagram of a Moore Finite State Machine (FSM) with one input X and one output Z.

a) Draw a state table for the FSM.

[4 marks]

b) Using an Implication Chart, or otherwise, reduce this to an equivalent FSM with the minimum number of states.

[12 marks]

c) For what sequence of input values will a '1' be produced at the output Z?

[4 marks]

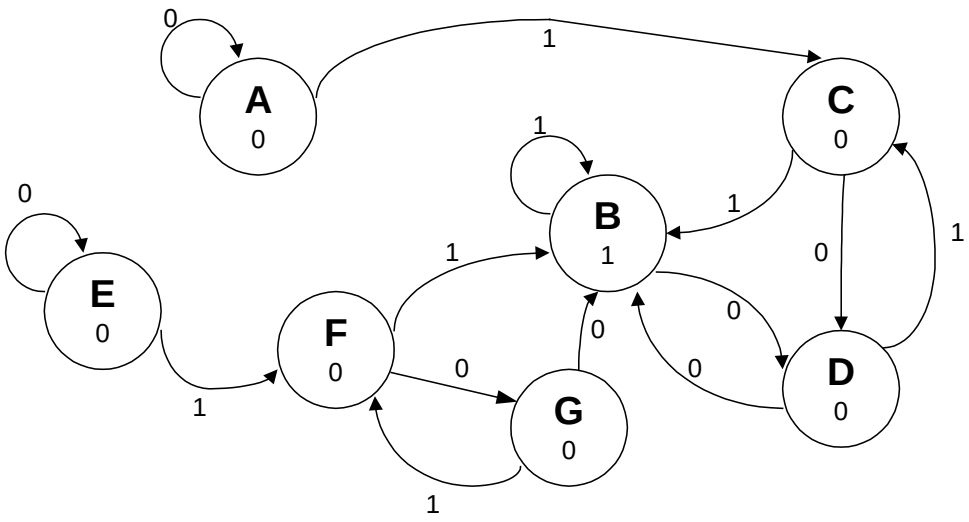


Figure 2

3. *Figure 3* shows an averaging circuit that computes the average of every four consecutive samples of an eight bit data stream `data_in` according to the equation:

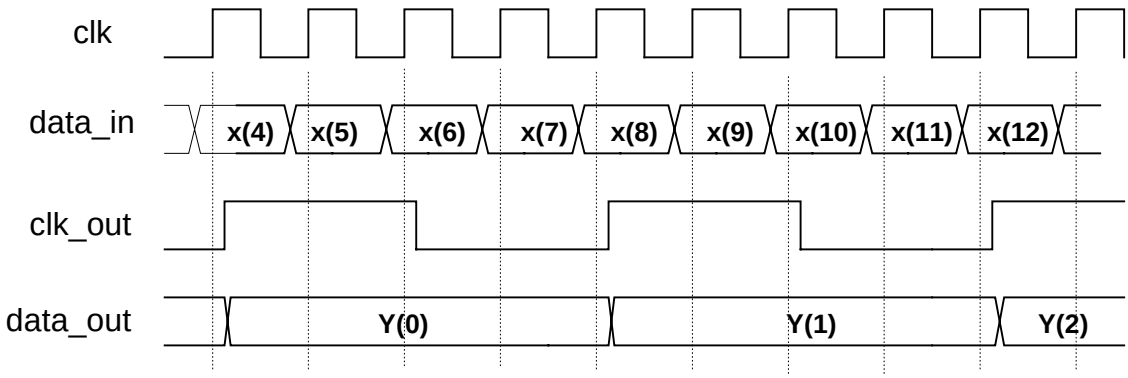
$$y(n) = \frac{x(4n) + x(4n+1) + x(4n+2) + x(4n+3)}{4}$$

where fractional values are rounded down to the nearest integer.

The input samples are clocked into the circuit at an input sample rate of 20 MHz. The averaged output is produced on `data_out` at 5 MHz as shown in *Figure 3* shortly after the rising edge of the output clock signal `clk_out` which is derived from the system clock `clk`.

Using adders, counters, registers and any other logic gates, design the averaging circuit. You may assume that the input-to-output delay of the adder is 20 ns. The propagation delays of all other gates and the set-up times of flip-flops are all 5 ns. The hold-times of flip-flops are 0 ns.

[20 marks]



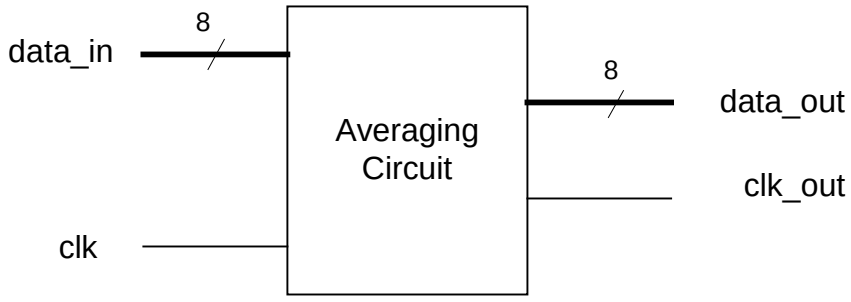


Figure 3

4. Given that x is an N-bit signed 2's complement number, the following equation applies:

$$x = \sum_{j=0}^{N/2-1} 2^{2j}(-2x_{2j+1} + x_{2j} + x_{2j-1}) \qquad \text{where } x_{-1} = 0, \text{ and for } i \quad 0,\ x_i \text{ is bit } i \text{ of } x.$$

Using an 8-bit binary adder, a 13-bit register, a 6-input multiplexer, and any additional gates required, design a circuit that multiplies two 6-bit 2's complement signed numbers in three clock cycles to give a 12-bit 2's complement answer. Draw a timing diagram showing the control signals required for your circuit.

[15 marks]

Given that the propagation delays of the various components are as follows: MUX – 5ns; adder – 15ns; register – 5ns; XOR gate – 5ns; any other gates – 2ns; and that the data set-up time for the register is 2ns, derive the maximum possible clock frequency for your circuit. State any further assumptions you make.

[5 marks]

5. *Figure 4* shows the memory interface circuit for an 8-bit microprocessor system with a 16-bit address bus and is controlled by a symmetrical clock running at 33.33 MHz. The system has three memory components with the following address ranges and chip-enable/address to data access times:

	Address Range (hex)	Access Time (EN/Addr to Data)
RAM	0000 - 7FFF	15 ns
ROM1	A000 - BFFF	50 ns
ROM2	C000 - FFFF	75 ns

The processor memory read cycle with a single wait cycle inserted is given in *Figure 5* with the various timing constraints as shown. The $\overline{WAIT}$ signal is sampled on the falling edge of *CLOCK* during T2 and subsequent wait cycles, and one extra cycle is inserted if $\overline{WAIT}$ is low, otherwise it proceeds to T3.

a) Derive in the form of Boolean equations the address decoder circuit needed to generate the chip-select signals for RAM, ROM1 and ROM2. (Memory should only be enabled during memory accesses.)

[4 marks]

b) Assuming that the address decoder circuit has a worst-case delay of 10 ns, derive the number of wait states, if any, needed for each type of memory read access.

[6 marks]

c) Design a circuit to produce the signal $\overline{WAIT}$ required to ensure proper memory read access for the memory components.

[10 marks]

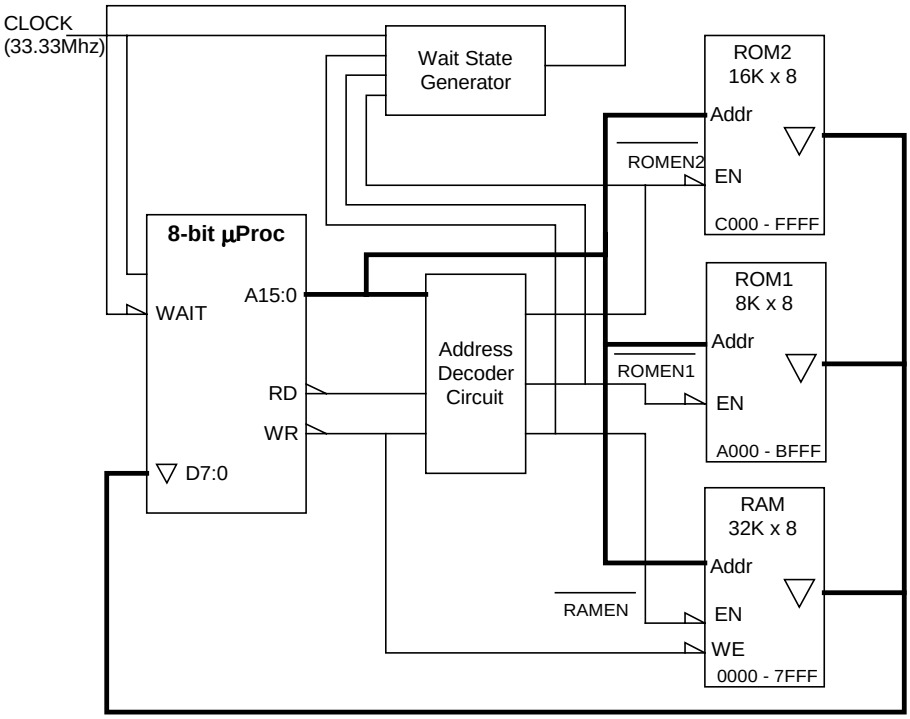


Figure 4

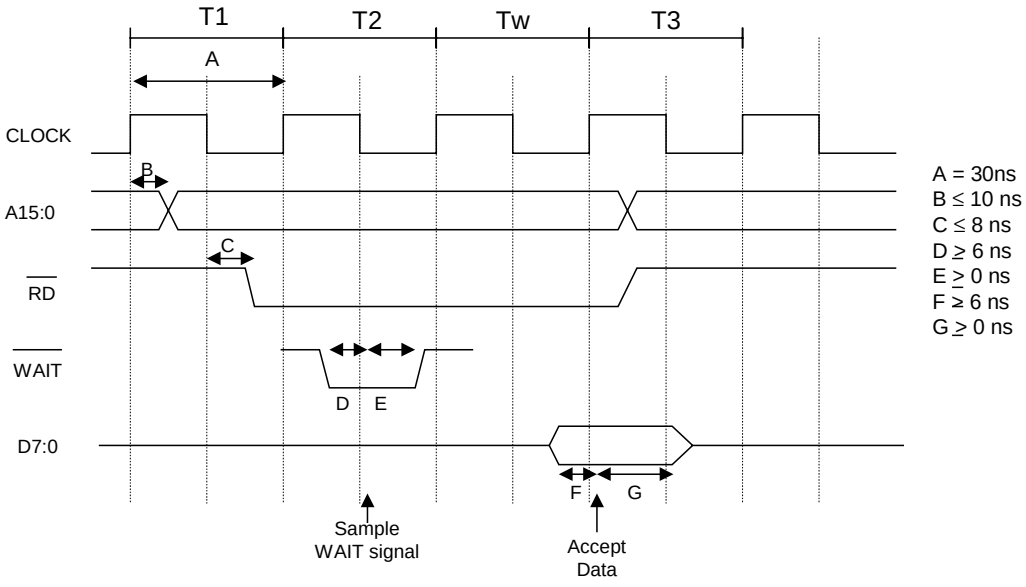


Figure 5

6. a) Design a 8 x 8 combinatorial, unsigned, parallel multiplier using only ripple carry adders and four 4 x 4 unsigned parallel multipliers.

[16 marks]

b) The Altera Flex 10K family of FPGAs contain Embedded Array Blocks (EABs) that can be configured as 2048 x 1-bit, 1024 x 2-bit, 512 x 4-bit or 256 x 8-bit RAM blocks. They also contain Logic Elements (LEs), each having a 4-input Look-Up Table and a register.

Estimate with justifications the hardware resources required to implement the multiplier in (a) as a pipelined multiplier using a Flex 10K device. You may assume that 1 LE is required for each output bit of an adder.

[4 marks]

7. *Figure 6* shows a sequential circuit with one input P and one output Q. P changes shortly after the rising edge of CLK. On power-up, the Finite State Machine is always reset to an idle state.

   Design a state machine in the form of a Mealy state diagram or an Algorithmic State Machine chart for each of the following cases:-

   a) Q = 1 if and only if the total number of 1's in P sampled on the rising edges of CLK is divisible by 3 as depicted in *Figure 7*.

   [6 marks]

   b) Q = 1 if (a) is true AND the total number of 0's in P sampled on the rising edges of CLK is an even number greater than or equal to 2.

   [14 marks]

Figure 6

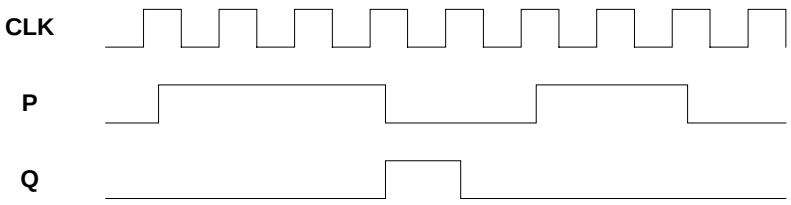
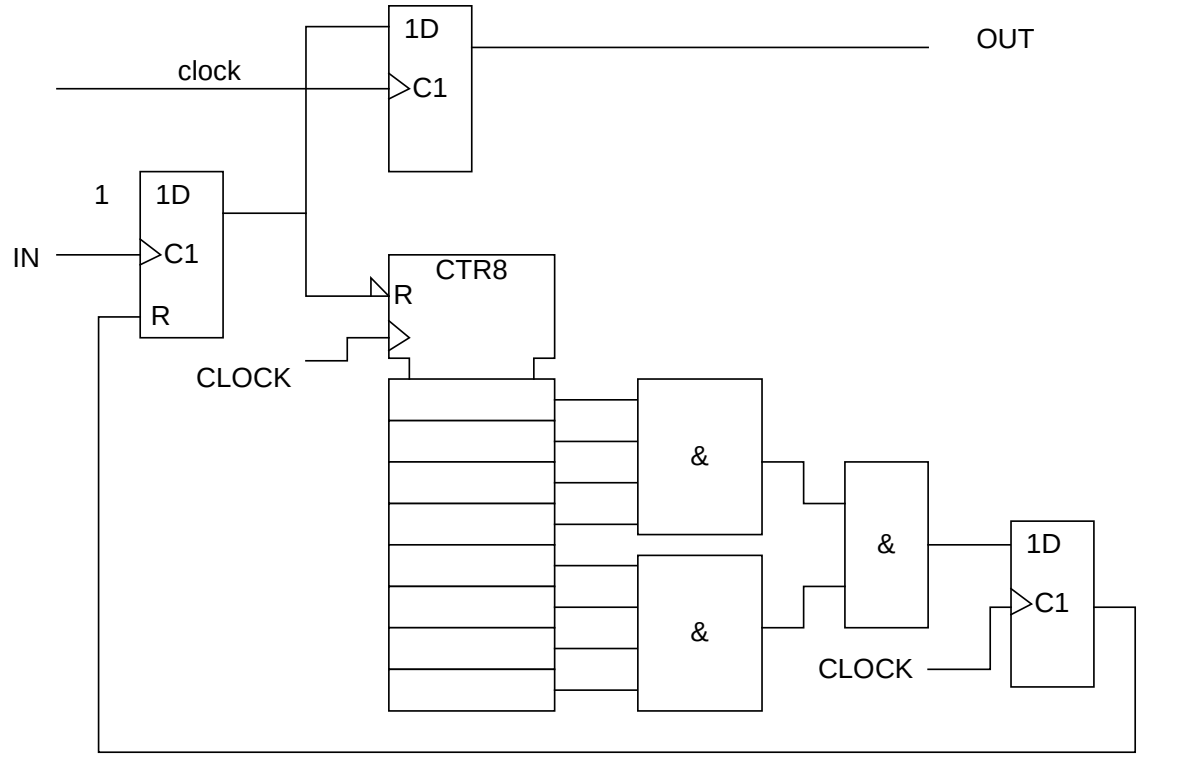


Figure 7

[END]

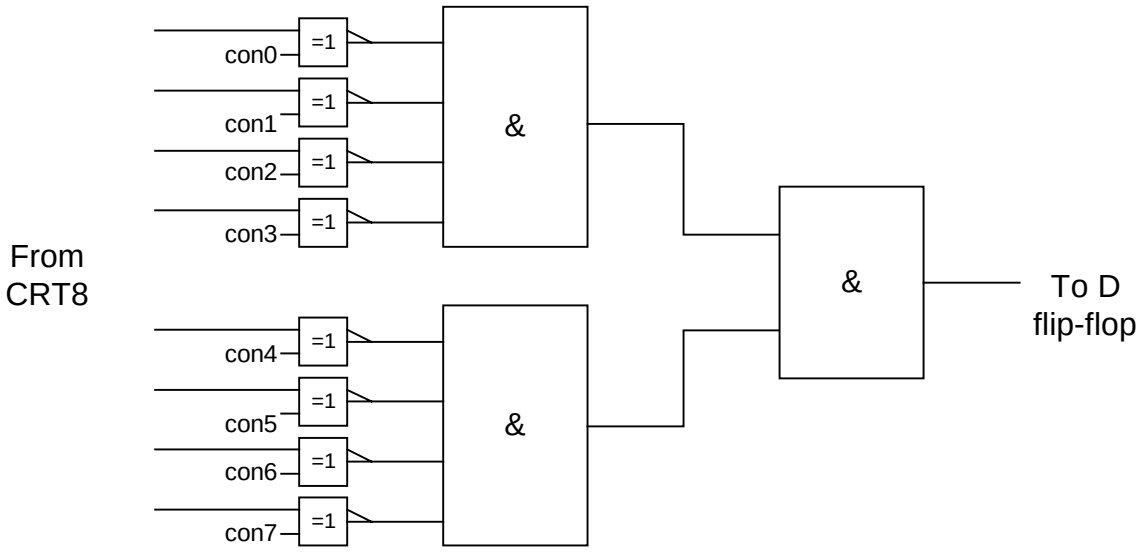
Answer to Question 1

(a)



[12 marks]

(b) Same as (a) with the following modifications to the input of the AND gate:-



[8 marks]

Answer to Question 2

(a)

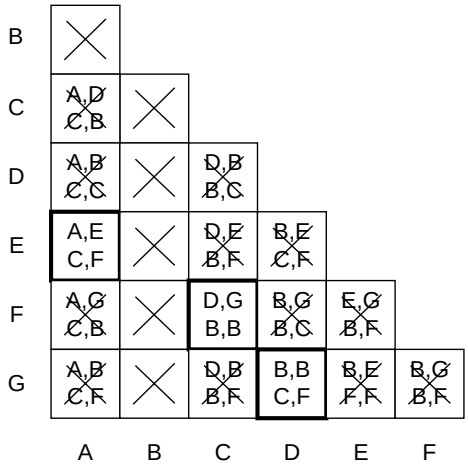
Current State	Next State X=0	Next State X=1	Output Z
A	A	C	0
B	D	B	1
C	D	B	0
D	B	C	0
E	E	F	0
F	G	B	0
G	B	F	0

or (need to latch output)

Current State	Next State, Next O/P x = 0	Next State, Next O/P x = 1
A	A, 0	C, 0
B	D, 0	B, 1
C	D, 0	B, 1
D	B, 1	C, 0
E	E, 0	F, 0
F	G, 0	B, 1
G	B, 1	F, 0

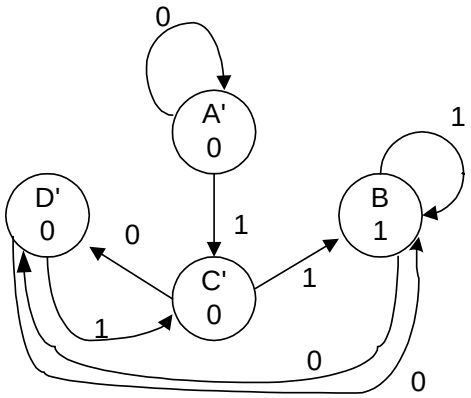
[4 marks]

(b) For 1st table (Moore representation)



[12 marks]

Therefore A E, C F, D G



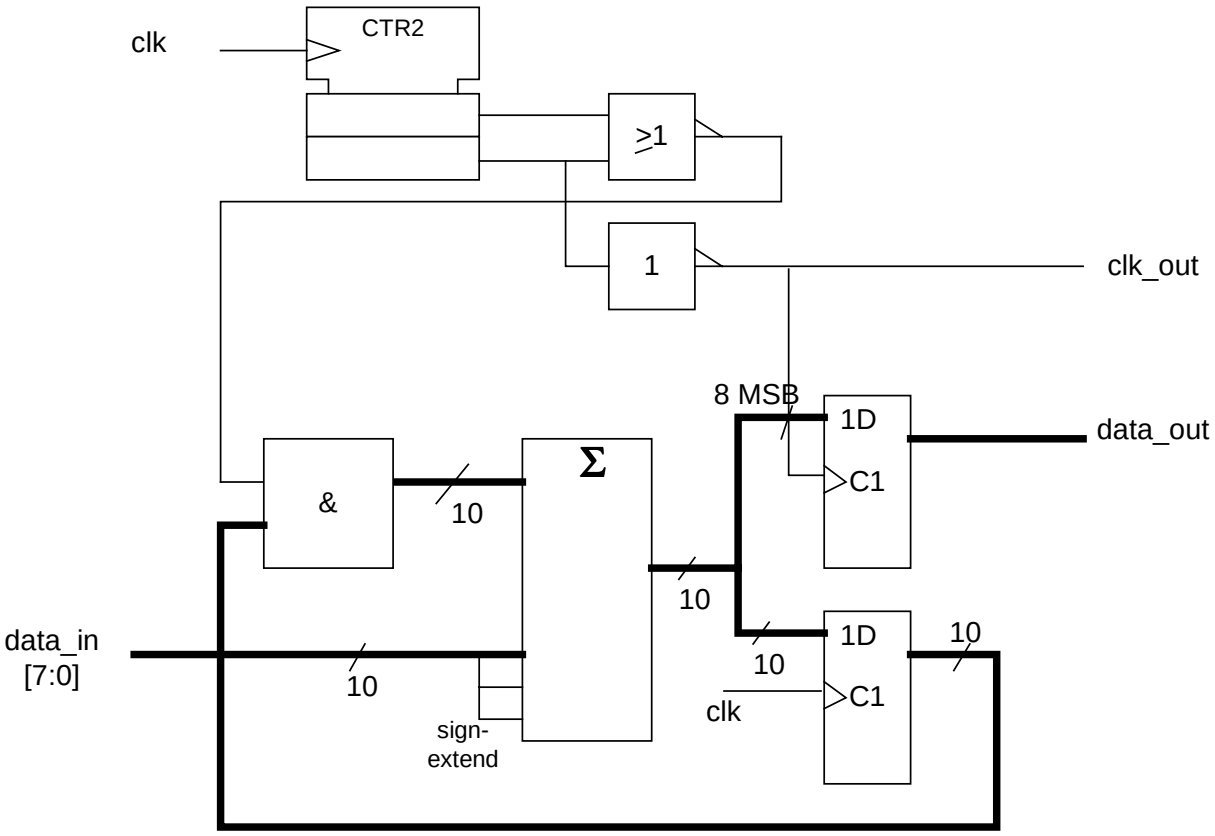
Reduced machine:

Current state	X=0	X=1	Z
A’	A’	C	0
B	D’	B	1
C’	D’	B	0
D’	B	C	0

(c) Whenever there are two or more consecutive ‘1’s, or double ‘0’ after a ‘1’.

[4 marks]

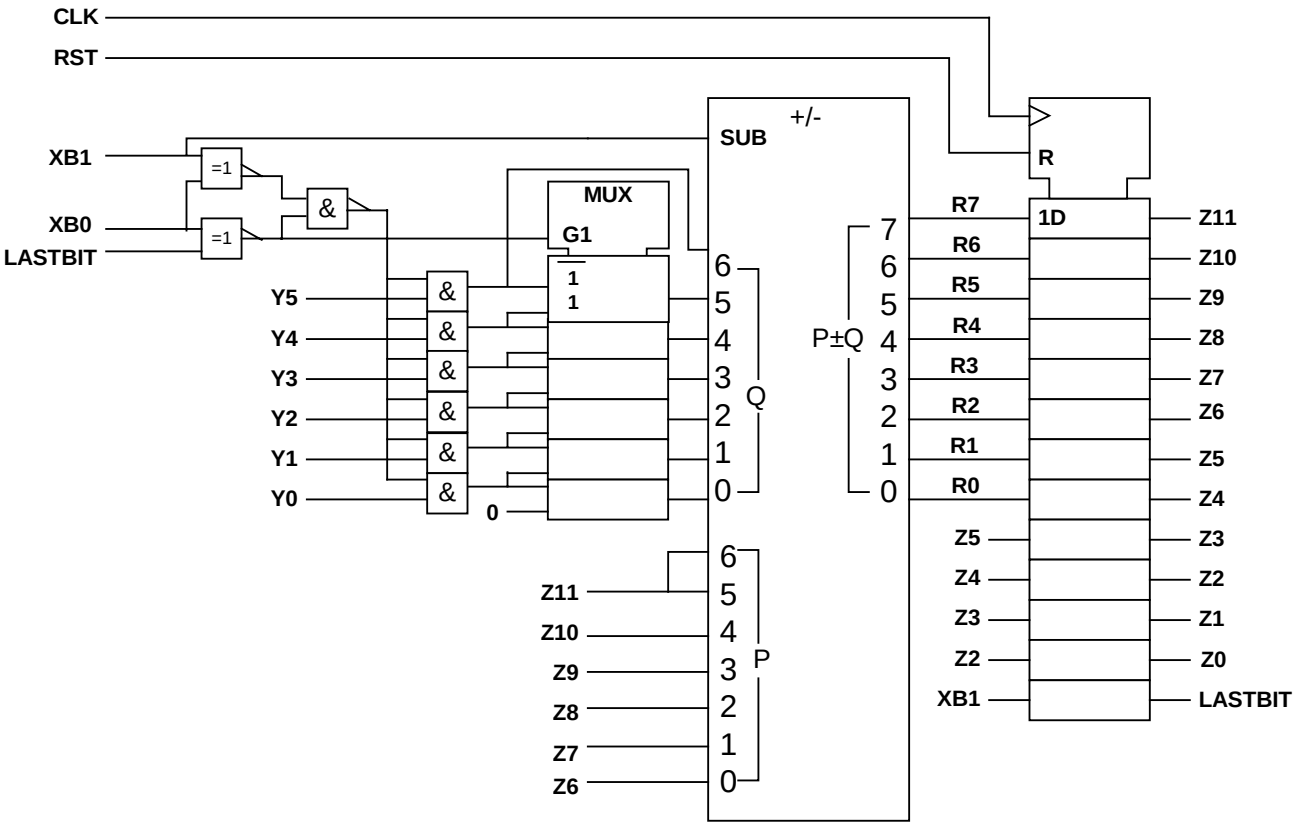
Answer to Question 3



[20 marks]

Answer to Question 4

This is a standard modified booth multiplier that takes three cycles to do 6 bits.



[15 marks]

The +/- block consists of 8-bit adder with XOR gates on Q-input controlled by SUB. Therefore worst case delay is 15+5 = 20ns.

Worst case path: LASTBIT – gates – MUX – add/sub – setup time – register output delay

Worst case delay : 10+2+2+5+15+2+5 = 36 ns. (asumme add/sub = 15ns)

(This will vary depending on student's circuit.)

Therefore max frequency = <u>27.8 MHz</u>.

[5 marks]

Answer to Question 5

(a)

$$\overline{RAMEN} = \overline{\overline{A15} \bullet [RD + WR]}$$

$$\overline{ROMEN1} = \overline{A13 \bullet \overline{A14} \bullet A15 \bullet RD}$$

$$\overline{ROMEN2} = \overline{A14 \bullet A15 \bullet RD}$$

[4 marks]

(b)

Available access time from address to data = 2*A + n_wait*A - B - F

= 2*30 + n_wait*30 - 10 - 6

= 44 + n_wait * 30

Access from EN to data = 1.5 * A - C - t_{decode} - F + 30 * n_wait

= 1.5 * 30 - 8 - 10 - 6 + 30 * n_wait

= 21 + 30 * n_wait

Therefore:

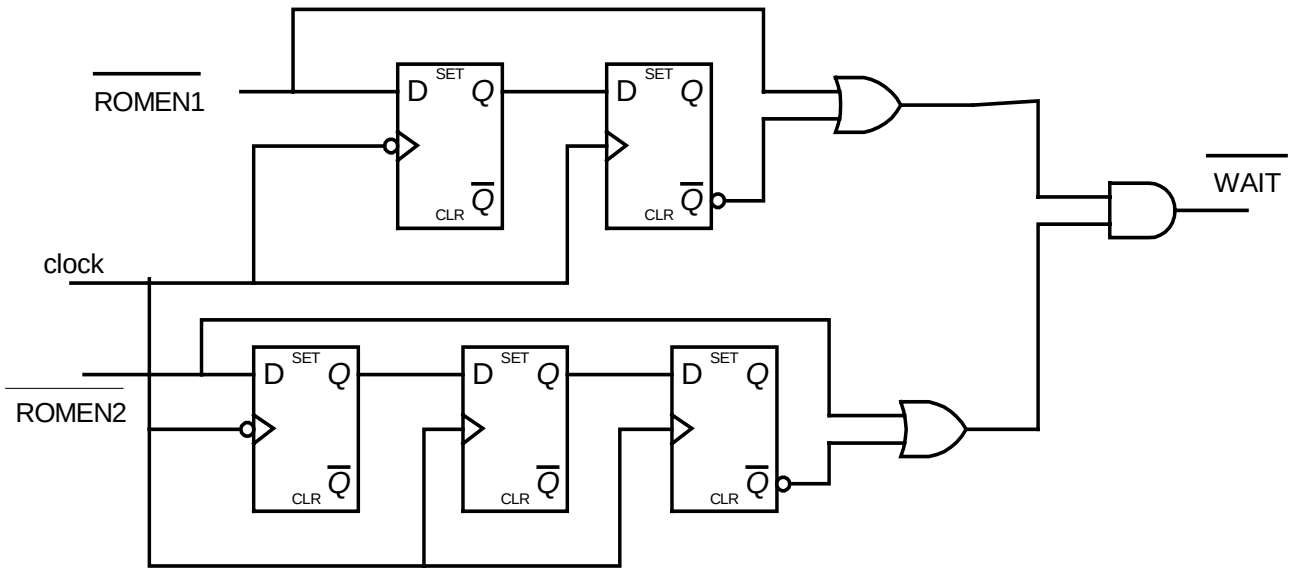
RAM : 0 wait state

ROM1: 1 wait state

ROM2: 2 wait states

[6 marks]

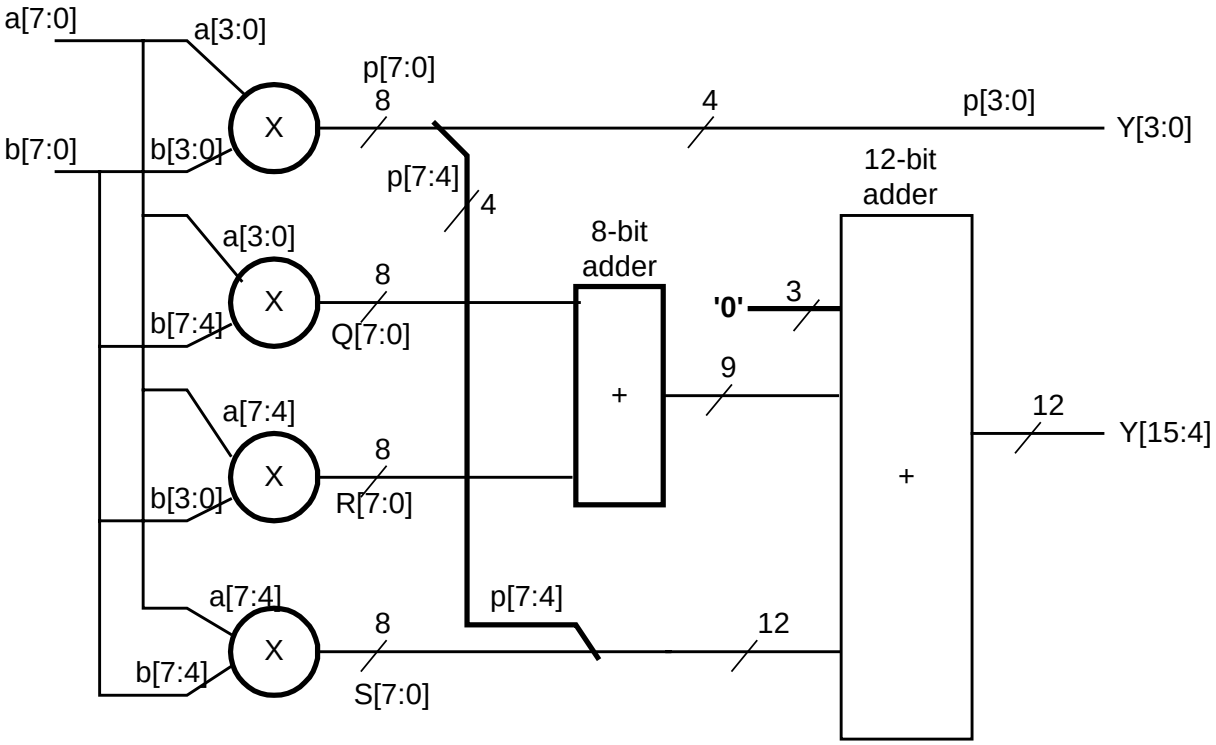
(c)



[10 marks]

Answer to Question 6

a.



[16 marks]

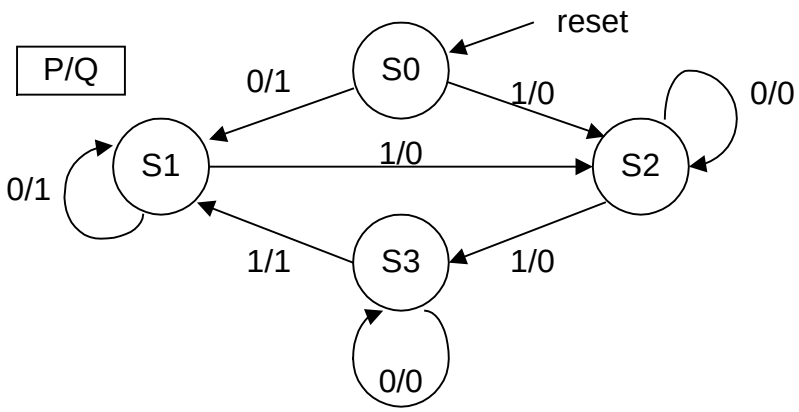
b.

Needs 4 EABs which already contains pipeline registers. Each LE give a single bit adder. Therefore need 20 LE in total.

[4 marks]

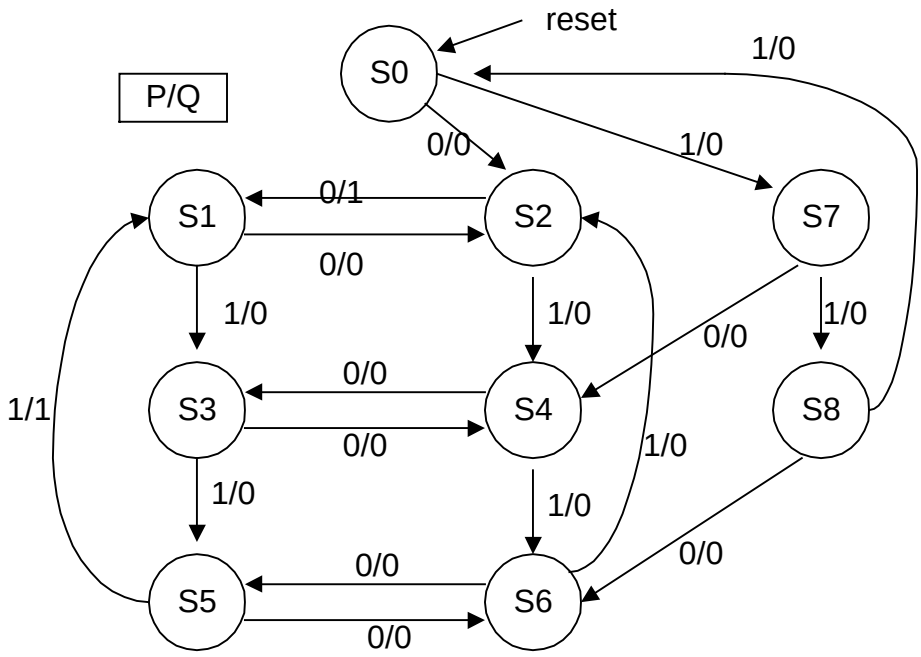
Answer to Question 7

a) Output is delayed through a register – Mealey machine.



[6 marks]

b.



[14 marks]