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IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2005

MSc and EEE PART III/IV: MEng, BEng.and ACGI

Corrected Copy

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Wednesday, 11 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : C. Toumazou

Second Marker(s) : D. Haigh

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1. (a) Figure 1 shows a partially-designed two-stage CMOS op-amp required to give a voltage gain of approximately *83 dB*. Given that the technology is a fixed *5μm* length double metal CMOS process, design the channel width of output driver transistor Q8 to achieve the required voltage gain specification. Aspect ratios of all other devices are shown on the circuit. Assume all bulk effects are negligible and that the voltage gain of level shifting buffer Q11 is approximately unity. Device model parameters are given below.

[12]

(b) Estimate the gain bandwidth product and slew rate for your op-amp design. Where would you connect two additional NMOS devices in Figure 1 to significantly increase the voltage gain of the op-amp?

[4]

(c) Briefly explain the function of transistor Q13.

[4]

CMOS TRANSISTOR MODEL PARAMETERS

MODEL PARAMETERS	$Kp\ (\mu A/V^2)$	$\lambda\ (V^{-1})$	$V_{T0}\ (V)$
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

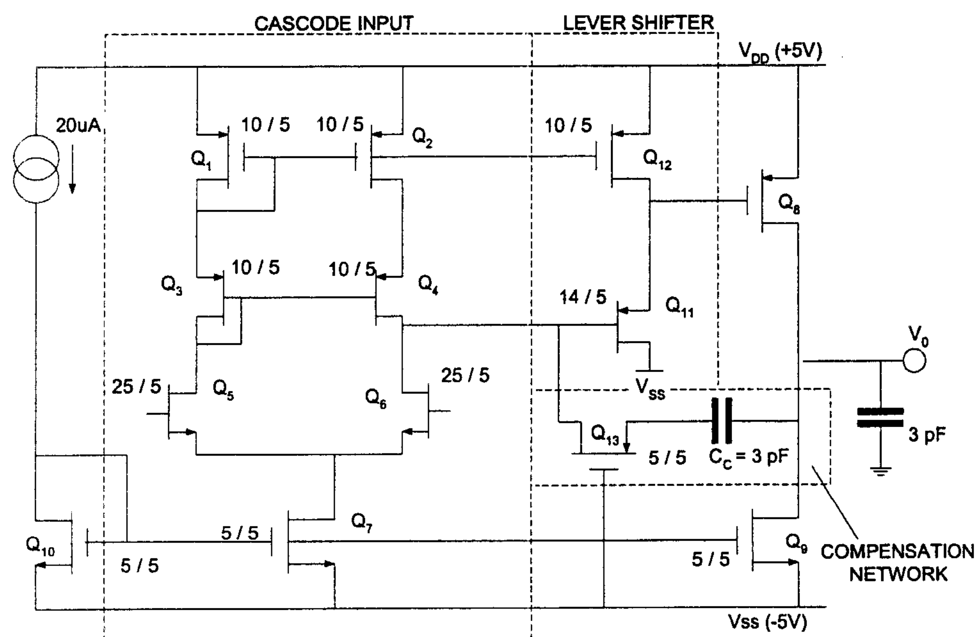

Figure 1

2. Advances in bipolar process technology have led to the development of a new generation of high speed, constant bandwidth operational amplifiers (op-amps) known as current-feedback op-amps.

   (a) Briefly discuss these technological advances and, with the aid of a macromodel, explain the theoretical concept of current-feedback and how it results in constant bandwidth amplification.
   [10]

   (b) The circuit shown in Figure 2 is a typical architecture for a current-feedback op-amp. Very briefly explain the operation of the circuit and comment upon why the slew rate of such an op-amp architecture can potentially be greater than *1000 V/μs*.
   [5]

   (c) Using the op-amp as a closed-loop non-inverting voltage amplifier and design the amplifier to have a voltage gain of 100 at a fixed bandwidth of approximately 10 MHz.
   [5]

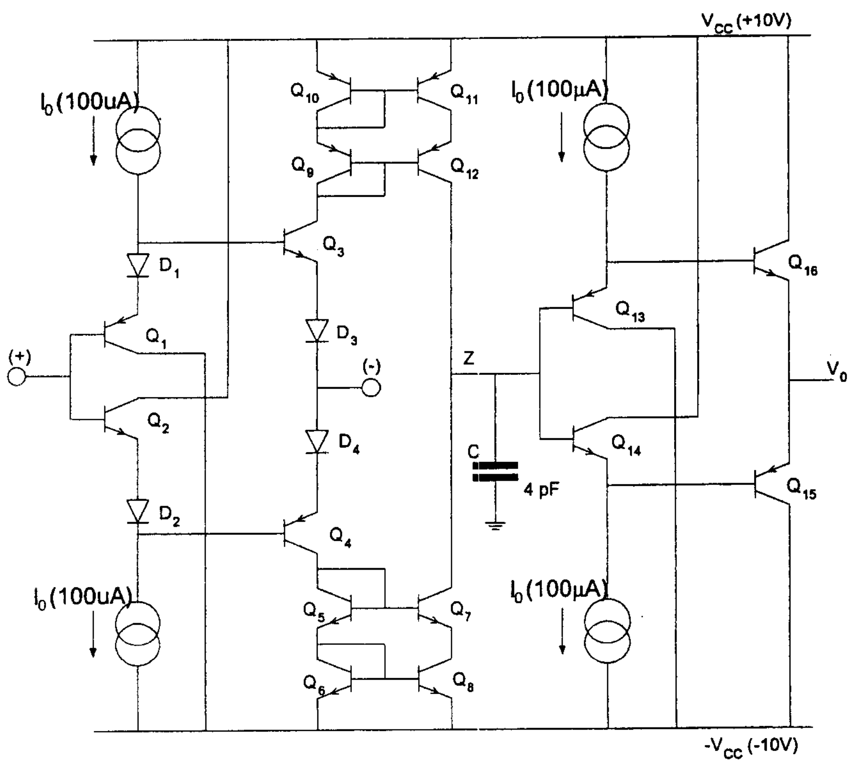

Figure 2

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3. Figures 3(a), 3(b) and 3(c) show the basic design of three integrated circuit precision integrators.

   (a) Derive an expression for the time constant of each integrator. Assume that the sampled-data integrators of Figure 3(b) and (c) are driven by non-overlapping clocks and that the switches are ideal.

   [15]

   (b) Figure 3(d) shows an active RC biquadratic filter. Replace the filter with a switched capacitor equivalent and design the filter to give a 10 kHz cut-off frequency. The filter design is based on a Butterworth low pass filter with a clocking frequency of *fc* = 250 kHz.

   [5]

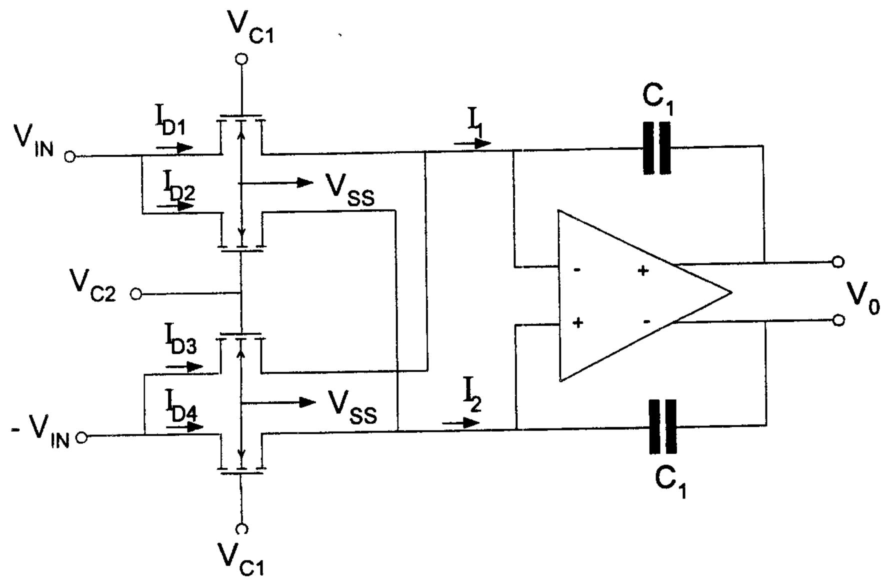

Figure 3(a)

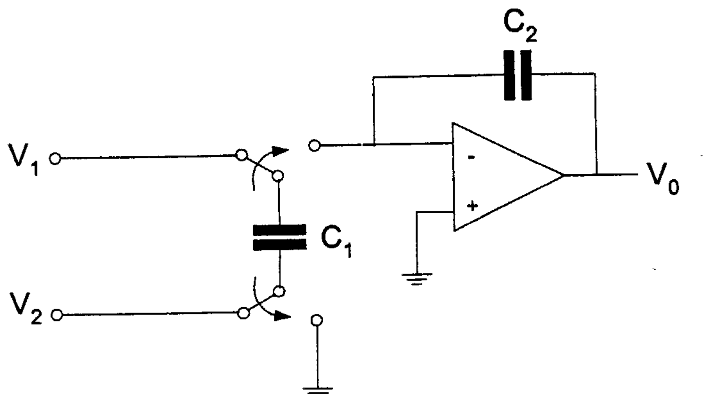

Figure 3(b)

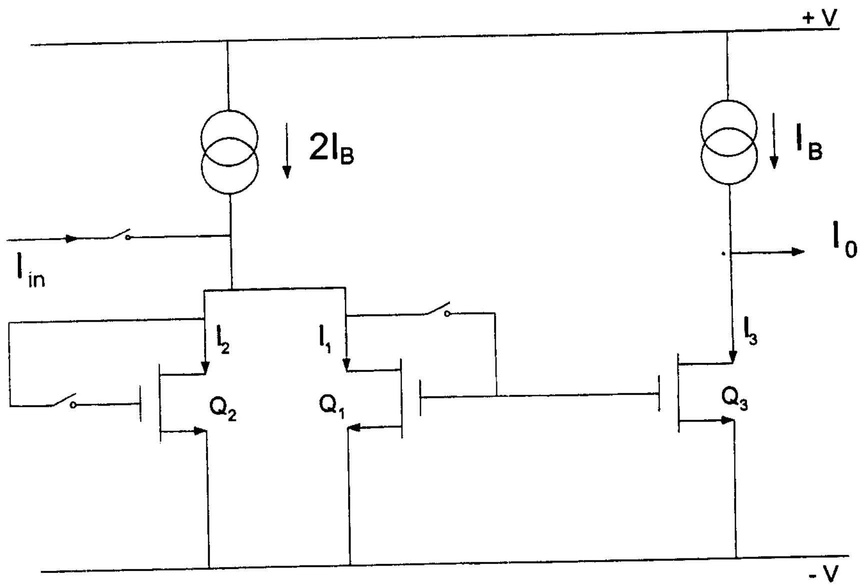

Figure 3(c)

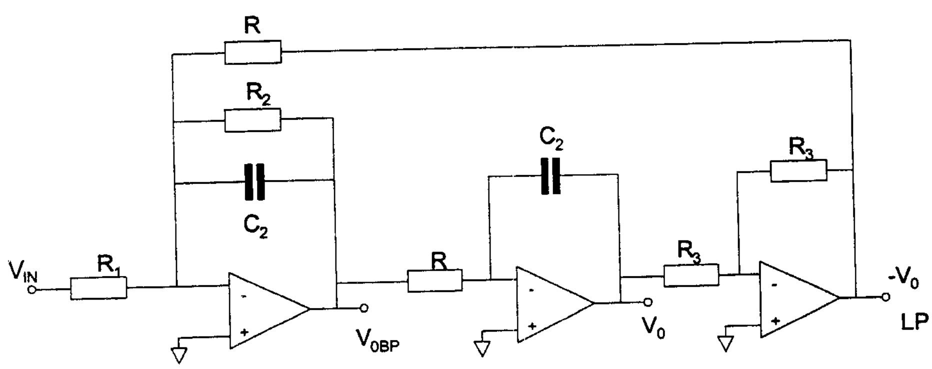

Figure 3(d)

4. Figure 4 (a, b c, and d) show four popular biasing schemes typically used in analogue integrated circuits.

(a) Briefly explain the function of each of the circuits in Figure 4 (a, b, c and d) and derive expressions for the constant output parameter in each case, clearly indicating component design requirements and any approximations you have made. You may ignore bulk effects in the CMOS circuits.

[16]

(b) Design the constant current generator of Figure 4(c) to give an output current of 5 μA. Assuming R is a polysilicon resistor with a temperature coefficient of 1500 ppm/°C, calculate the fractional temperature coefficient of the circuit at room temperature.

[4]

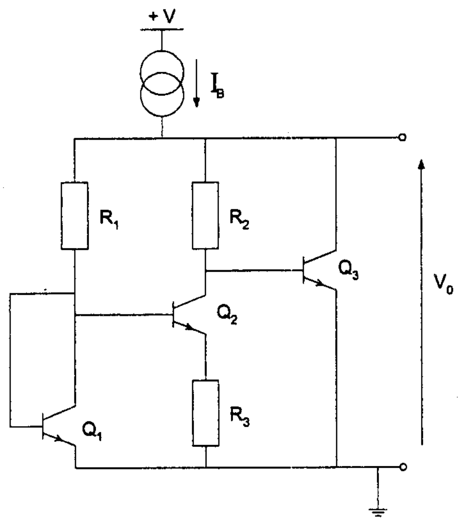

Figure 4(a)

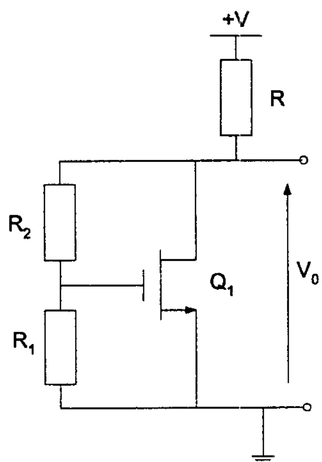

Figure 4(b)

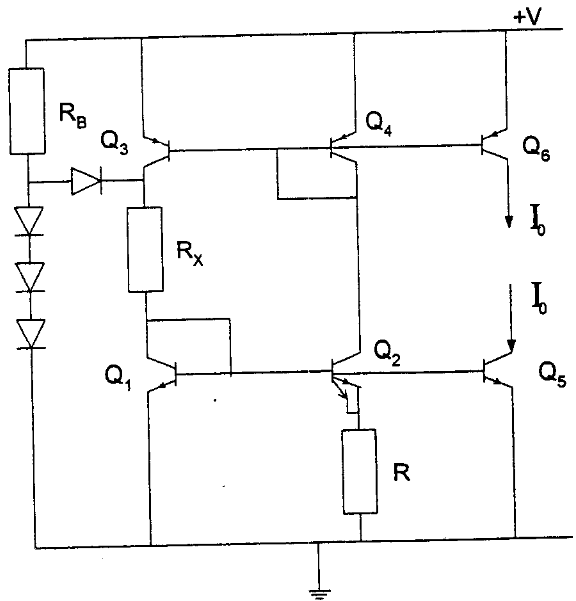

Figure 4(c)

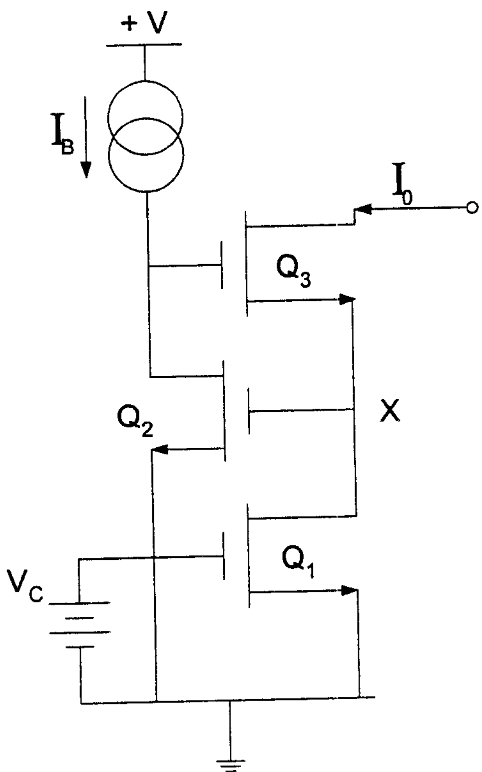

Figure 4(d)

5. (a) Two high-performance analogue-to-digital converters are the current-mode algorithmic converter and the sigma-delta converter. Sketch a typical architecture for ONE of these converter types and explain its principles of operation.

[10]

(b) Assume that the maximum resolution of any sampled-data converter is limited by switch noise (KT/C), calculate the maximum resolution of a stereo-audio system running at a sample rate of 40 kHz. Assume a MOSFET switch aspect ratio $(W/L) = 1/8$, transconductance parameter $Kp = 20\ \mu A/V^2$ and a device threshold voltage $V_T = 1\ V$. The on voltage of the switch is a $5\ V$ reference (i.e. $V_{GS}on = V_{ref} = 5\ V$). You may also assume that the switch settles in $10\ \tau$ (where τ = time constant) over one period of the clock frequency.

Boltzmanns constant $k = 1.38 \times 10^{-23}\ J/K$ and the ambient temperature is $300\ K$.

[10]

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6 (a) Figure 6(a) shows a folded cascode connection. What is the main advantage of this design over the more classical cascode connection? Show via a brief sketch how the architecture of Figure 6(a) can be used to form the basis of a single stage folded cascode operational amplifier (op-amp).

[6]

(b) Give one advantage and disadvantage of a single stage over a two-stage op-amp. Figure 6(b) shows a two-stage CMOS op-amp. Estimate the low-frequency differential voltage gain and gain-bandwidth product of the amplifier. Aspect ratios of all devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below.

[11]

Answer one of the following:

(c) The gain-bandwidth product, voltage gain and slewrate of the op-amp of Figure 6(b) are below the desired specification. Explain qualitatively a minimum sequence of parameter change so that the op-amp design satisfies all of its specifications.

[3]

or

(d) Explain why a resistor in series with the compensation capacitor *C* in Figure 6(b) can significantly improve the amplifier's phase margin.

[3]

CMOS TRANSISTOR PARAMETERS

MODEL PARAMETERS	K_p ($\mu A/V^2$)	λ (V^{-1})	V_{TO} (V)
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

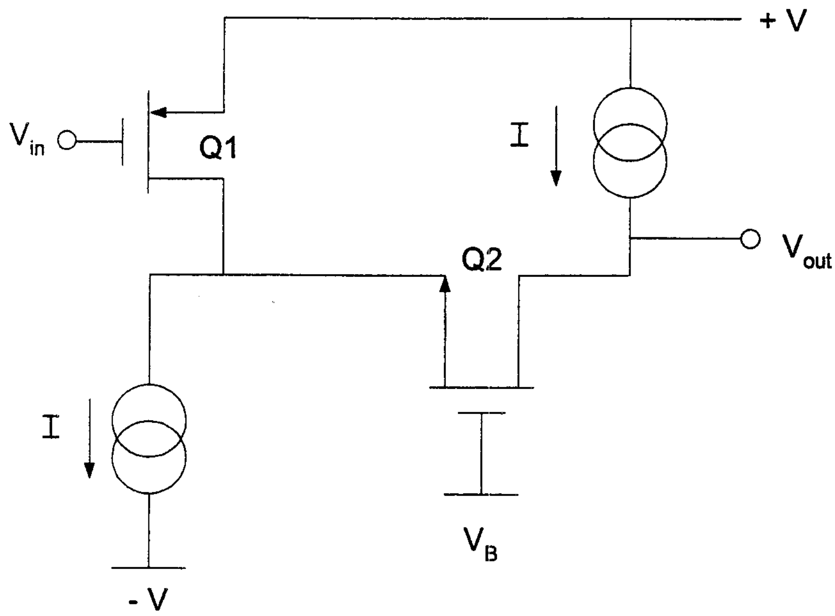

Figure 6(a)

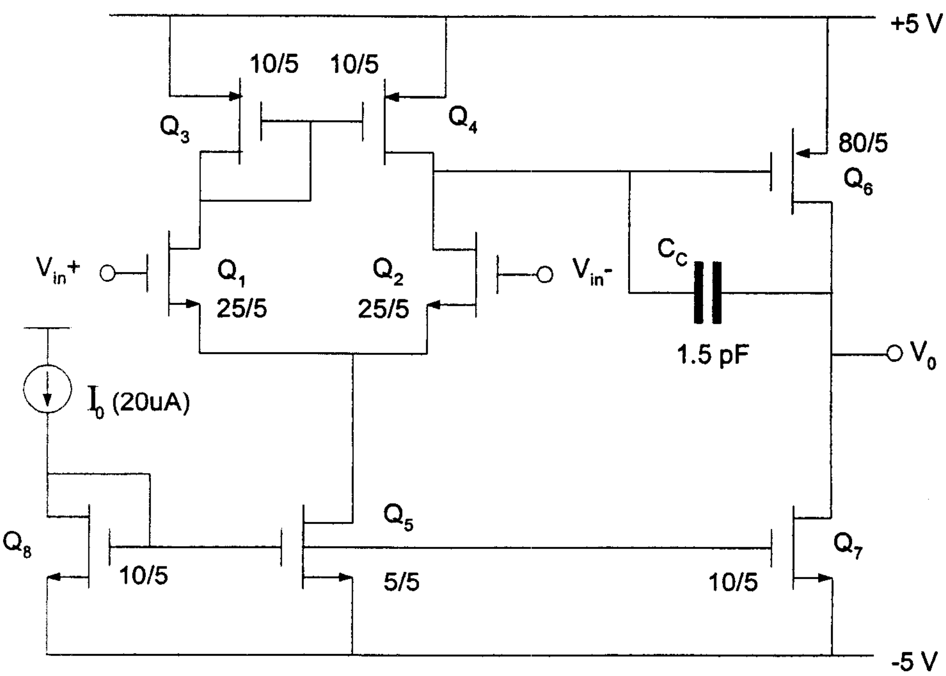

Figure 6(b)

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ANALOGUE I C AND SYSTEMS

EXAM SOLUTIONS

2005

Solutions all fine!

C. TOUMAZOU

MARCH 2005

Question (1)

Q.

Required gain ≃ 83dB.

A_1 (1st stage), $A_1 = g_{m6} / [g_{o6} + \frac{g_{o2} g_{o4}}{g_{m4}}]$

From $I_D = \frac{\beta}{2}(V_{GS} - V_T)^2$

$g_m = 2\sqrt{\beta I_D}$ where $\beta = kW/2L$

$\therefore g_{m6} = \sqrt{2 \times 30 \times 10^{-6} \times 10^{-6} \times 5} = 5.477 \times 10^{-5} S$

$g_{m4} = \sqrt{2 \times 20 \times 10^{-6} \times 10^{-6} \times 2} = 2.83 \times 10^{-5} S$

$g_{o6} = \lambda_N I_d = 0.02 \times 10 \times 10^{-6} = 2 \times 10^{-7} S$

$g_{o4} = g_{o2} = \lambda_p I_d = 0.03 \times 10 \times 10^{-6}$

$= 3 \times 10^{-7} S$

$\therefore A_1 = 269.57 = 48.6 dB.$ — (6)

Gain of 2nd stage $A_2 \approx 83 - 48.6 \approx 34dB$

≈ 50

$\therefore A_2 \approx g_{m8}/(g_{o8} + g_{o9}) \approx 50$

$\therefore g_{m8} = 2\sqrt{\beta_8 I_d} = 50 I_d (\lambda_N + \lambda_p)$

$\beta_8 = 25(\lambda_N + \lambda_p)^2 I_d = 25(0.05)^2 \times 20 \times 10^{-6}$

$= 3.125 \times 10^{-5}$

Since $\beta_8 = \frac{k_p W}{2L} \Rightarrow (W/L)_8 = 3.125 \times 10^{-5} A/V^2$

$\therefore W_8 = 16 \mu m$ — (6)

b) G·B product $\approx g_{m6}/C_c$

$$\approx 5{\cdot}477\times10^{-5}/3\text{ pF} = 18{\cdot}25\times10^{6}\text{ rads/s}$$

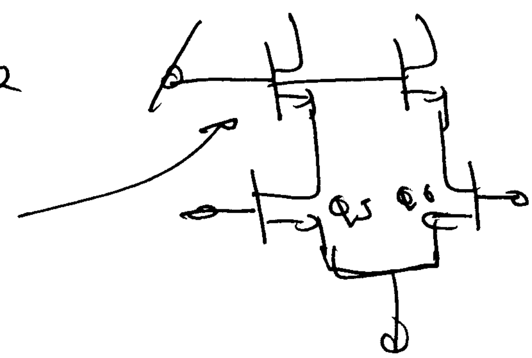
$$f = (18{\cdot}25/2\pi)\times10^{6} \approx$$

$$\underline{\underline{2{\cdot}9\text{ MHz}}}$$

$$\text{S·Rate} = I_o/C_c = (20\times10^{-6}/3\text{ pF}) = \underline{\underline{6{\cdot}66}}\text{ V/μs}$$

−4

c Two additional devices could be used to cascode Q5 and Q6, now fully cascoded resulting in a voltage gain of $(g_m/g_o)^2\,\tfrac{1}{2}$



c) The function of Q13 is to simulate an active resistor.

$$R \approx \frac{1}{2\beta(V_{GS}-V_T)}$$

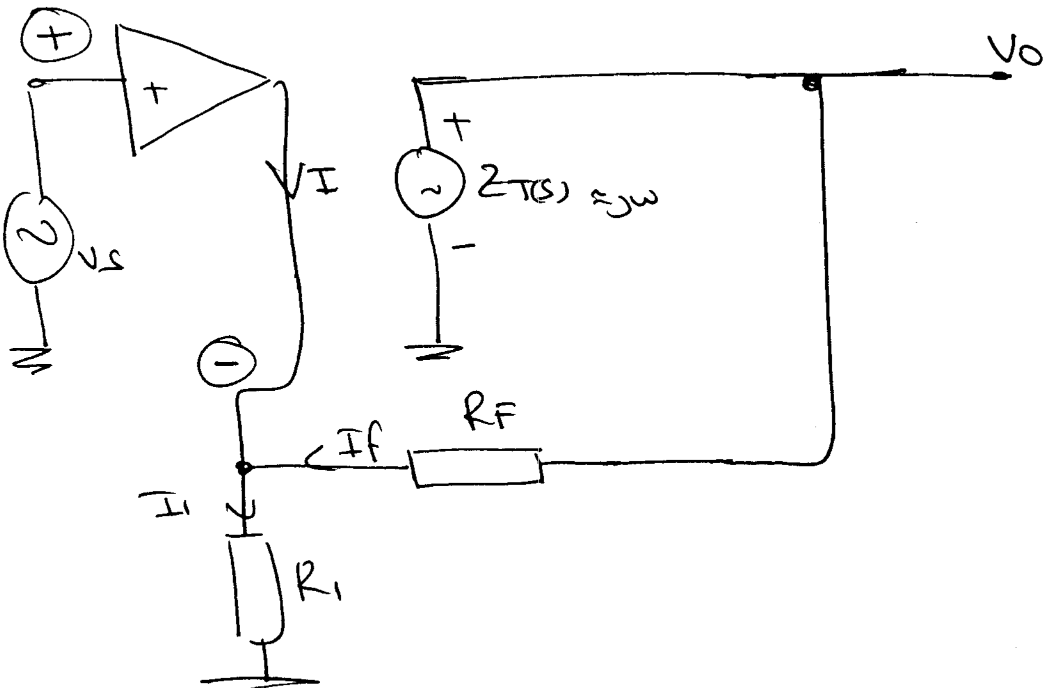
. Its function is to provide feedforward compensation and eliminate the undesirable Right hand Plane zero. with R, $Z = [g_{m8}/C_c]$, with R_{out}

$$Z = 1/(1/g_{m8} - R)C_c.$$

−4

Qu2

The most significant technological breakthrough was introduction of vertical PNP transistor and 'true complementary' bipolar technology.



$Z_T(s) = Z_{T0}/(1+jf/f_p) \Rightarrow f_p$ dominant pole

From model

$$I_f = (V_o - V_s)/R_F$$

$$I_1 = (V_s/R_1)$$

$$V_o = Z_T(s) I = Z_T(s)(I_1 - I_f)$$

From above

$$(V_o/V_s) = (1 + R_F/R_1)\left(\frac{Z_T(s)}{R_F + Z_T(s)}\right)$$ (5)

substitute for $Z_T(s)$, and assume $Z_{T0} \gg R_F$

$$(V_o/V_s)_{j\omega} = (1 + R_F/R_1)\left[\frac{Z_{T0}}{Z_{T0}+R_F}\right]\left[\frac{1}{1 + jf/f_p\frac{(Z_{T0}+R_F)}{R_F}}\right]$$

Again assuming $Z_{T0} \gg R_F$

$$(V_o/V_s)_{j\omega} = (1 + R_F/R_1)\, 1 \Big/ \left(1 + jf\Big/\frac{GB}{R_F}\right)$$

Qu(2) - cont.

where $G.B = f_p Z_{TO}$

$$f_{p\,closed} \approx (G.B/R_F)$$

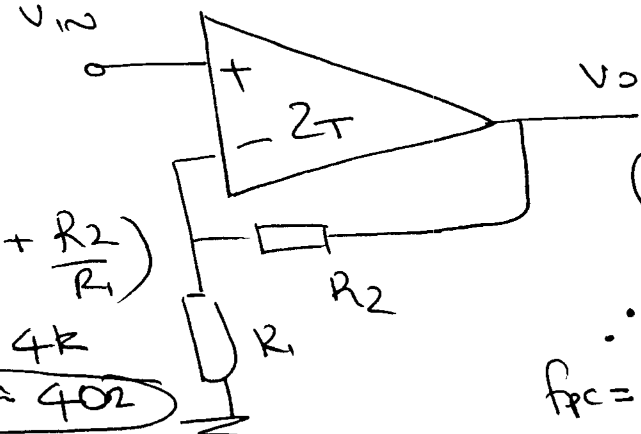
$R_1 \rightarrow$ Gain, $R_F \rightarrow$ Bandwidth.

Gain / bandwidth independence. (5)

b). Q1, Q2, Q3 and Q4 with bias chain form Class AB input voltage buffer between + and − input. Diodes ensure good matching. Cascode mirrors (Q9−Q12), (Q5−Q8) sense output current buffer (input current into (−ve) terminal) via collectors of Q3 and Q4 respectively. Z (high impedance gain node). Q13 − Q15 form class AB output buffer → low impedance output terminal. C − compensation capacitor (5)

Slew-rate high because of Class AB input stage, bias Io does not limit slew rate

c/.



$A_{cl} = \left(1 + \frac{R_2}{R_1}\right)$

$R_2 = 4k$

$R_1 \approx 40\Omega$

$f_p = \frac{1}{2\pi Z_T C}$

$\therefore$

$f_{pc} = 10MHz = \frac{1}{2\pi C R_2}$ (5)

knowing $C = 4pF \Rightarrow R_2 = 3.98k \approx \underline{\underline{4k}}$

Question 3

(a) Floating integrated RC integrator.

Double mos differential

$$R = \frac{V_{IN} - (-V_{IN})}{(I_1 - I_2)} = \frac{1}{2\beta(V_{C1} - V_{C2})}$$

$$\tau \approx RC = \frac{C}{2\beta(V_{C1} - V_{C2})} \text{ — } (*) \qquad (5)$$

(b) Differential, parasitic insensitive SC integrator. During one switch phase C_1 charges to $(V_1 - V_2)$ such that $I_{C1} = 1/T\,(V_1 - V_2)C$ or $f_c C_1 (V_1 - V_2)$ where f_c = clock frequency.

During the 2nd clock phase

$$I_{C1} = I_{C2} = j\omega C_2 V_o$$

$$\therefore \quad V_o = \frac{C_1}{C_2}\left[\frac{f_c}{j\omega}\right](V_1 - V_2)$$

Assumes $f_c \gg 2\pi/\omega$

$$\tau = \left[\frac{C_2}{C_1 f_c}\right] \longrightarrow (*) \qquad (5)$$

Question 3 cont

c/. Switched current integrator.

$\phi_2(n-1) \Rightarrow$

$$I_2(n-1) = I_B + I_{in}(n-1) + I_o(n-1)$$

During ϕ_1 of period(n)

$$I_1(n) = 2I_B - I_2(n-1) = I_B - I_{IN}(n-1) - I_o(n-1)$$

$$\Rightarrow I_o(n) = I_{IN}(n-1) + I_o(n-1)$$

In Z domain

$$I_o(z)\left[1 - z^{-1}\right] = I_{in}(z)z^{-1}$$

$$H(z) = \frac{I_o}{I_{in}}(z) = \frac{z^{-1}}{(1-z^{-1})} = \left(\frac{1}{z^{1} - 1}\right)$$

Since $z = e^{j\omega T} \approx (1 + j\omega T)$ for $\omega T \ll 1$

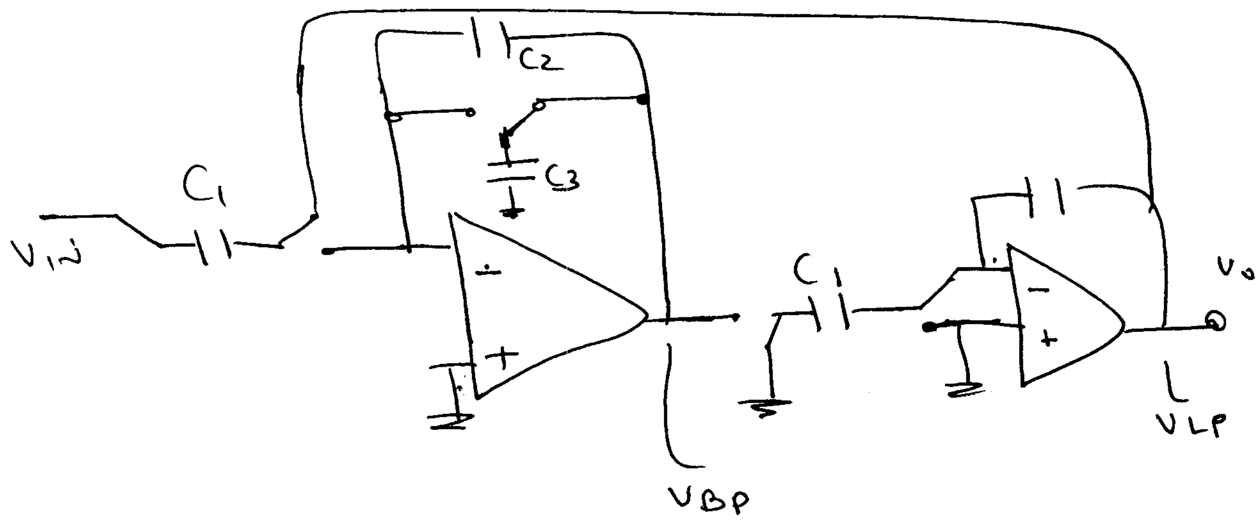
$\therefore H(z) = 1/j\omega T$ and so

5

$$\underline{\underline{\tau = T}}$$

Question 3d

Possible SC equivalent:-



For RC

$f_0 = 1/2\pi C_2 R$, $Q = R_2/R$

$H_{BP} = -R_2/R_1$, $H_{LP} = R/R_1$

SC $f_0 = \dfrac{C_1}{2\pi C_2}$, $Q = C_1/C_3$

For butterworth $Q = 1/\sqrt{2}$, $\sqrt{2} = C_3/C_1$

and $C_2/C_1 = (f_c/f_0)(1/2\pi) = 39.8$

if $C_1 = 1pF$, $C_2 = 39.8pF$, $C_3 = 1.41pF$

5

Q4.

a) Bandgap reference. Output voltage reference independent of temperature.
Assumes VBE ≈ −2.5mV/°C
Analysis β>>1

$V_{BE3} - V_{BE2} = V_T \ln(I_1/I_2) = I_2 R_1$

thus $V_o = V_{BE3} + (R_2/R_3)(V_T)\ln I_1/I_2$

for $dV_o/dt = 0$, then $(R_2/R_3)\ln I_1/I_2 \approx 24.5$, $V_o = 1.283V$ (4)

b) V_{gs} multiplier. Can replace stacked diodes with a single resistor for biasing purposes.

$V_o \approx V_{GS}[1 + R_2/R_1]$

$\approx (1 + R_2/R_1)[V_T + \sqrt{I_D/\beta}]$ (4)

c) PTAT (proportional to absolute temperature) constant current source/sink. The output current is virtually independent of the power supply voltages. Diode chain RB and RA form automatic start-up circuitry ensures circuit behaves in correct output state. (4)

Analysis – Assume matched devices β>>1
then $I_O = \Delta V_{be}/R = [V_T \ln(I_{IN}/I_O)(I_{S3}/I_{S1})/R$
$(I_{S3} = 2I_{S1})$ then $I_O = (V_T \ln 2)R$.

Question 4 – continued.

Fig 4d →

Regulated cascode current sink, since drain-source voltage of Q1 is regulated by the feedback amplifier Q2 the circuit has a very high output impedance equivalent to that of a double cascode.

Analysis, $I_O = \beta (V_G - V_T)^2$

assume FET Q1 is saturated (4)

b) $I_O = (V_T \ln 2) / R$

assuming $V_T = 25\,mV$ at $300°k$

then $R = 3.465\,k\Omega$.

$$T_{CF} = \frac{1}{V_T}\frac{\partial V_T}{\partial T} - \frac{1}{R}\,\partial R/\partial T$$

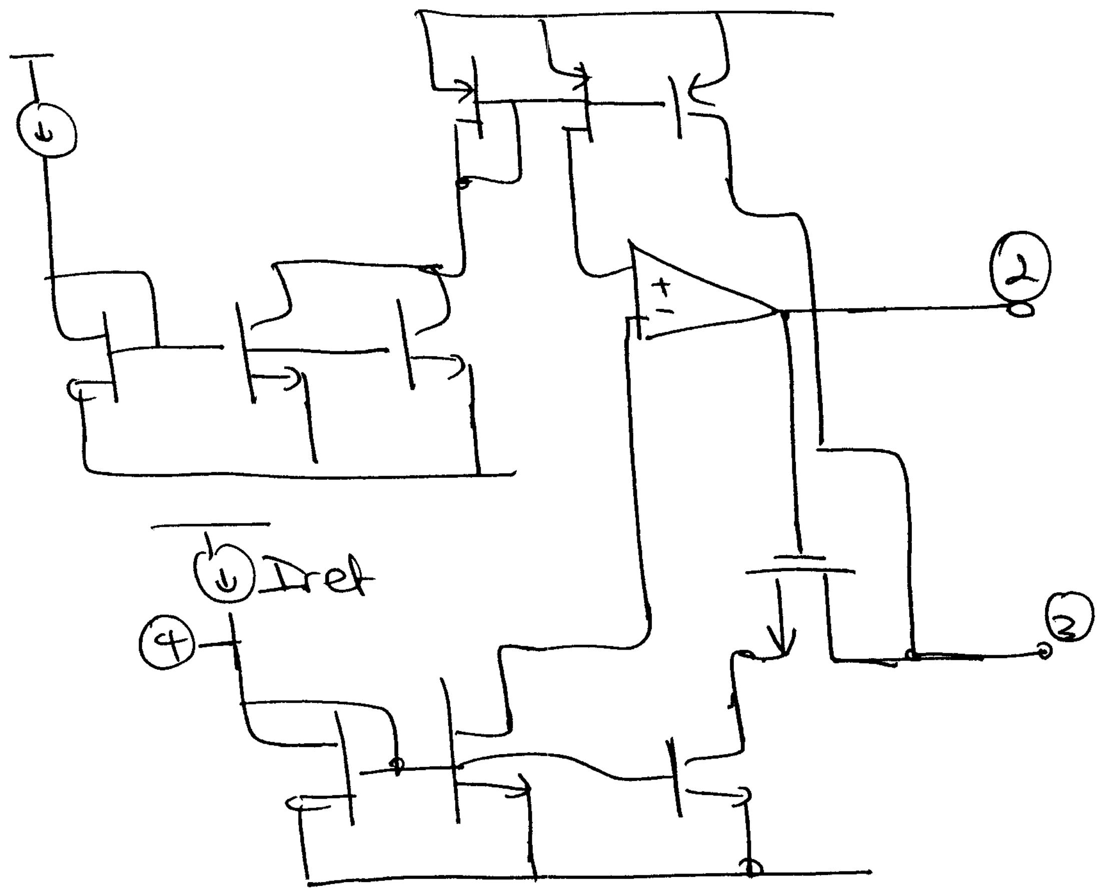
$$= \frac{1}{T} - \left(\frac{1}{R}\frac{\partial R}{\partial T}\right)$$

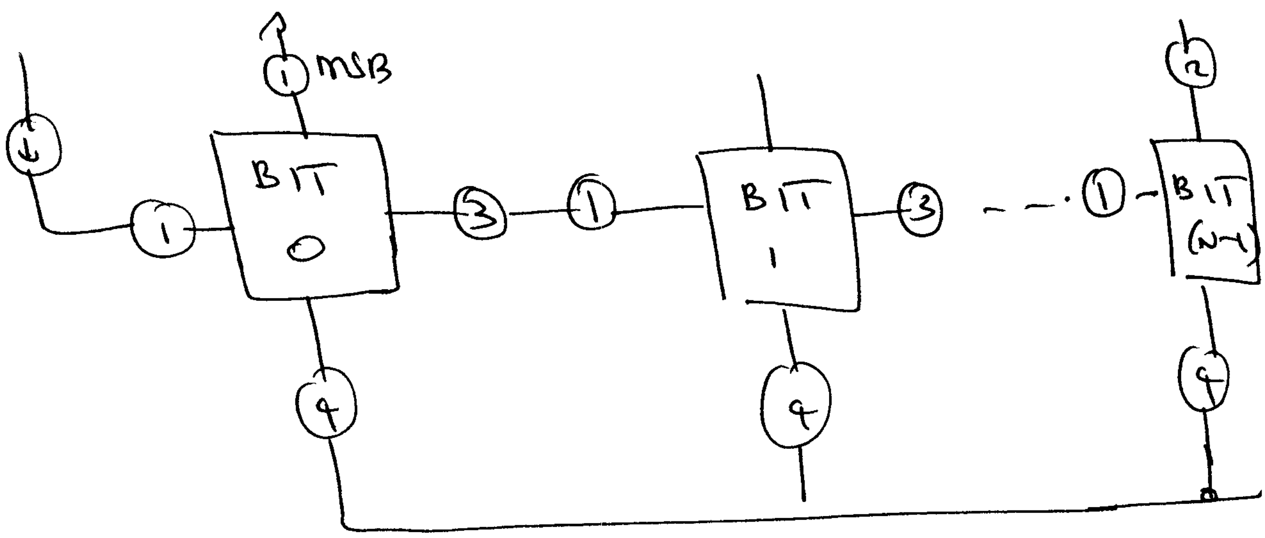
$$= (1/300) - 1500 \times 10^{-6}$$ (4)

$$= \underline{\underline{1833\ ppm/°C}}$$

Question 5

Algorithmic Converter 1 Bit





BASIC ARCHITECTURE

Question 5 - Cont

If $2I_{IN} < I_{ref}$

Comp goes low , digital output = 0

and analogue output $2I_{in}$

If $2I_{IN} > I_{ref}$, comp output goes high , digital = 1

analogue output $(2I_{IN} - I_{ref})$

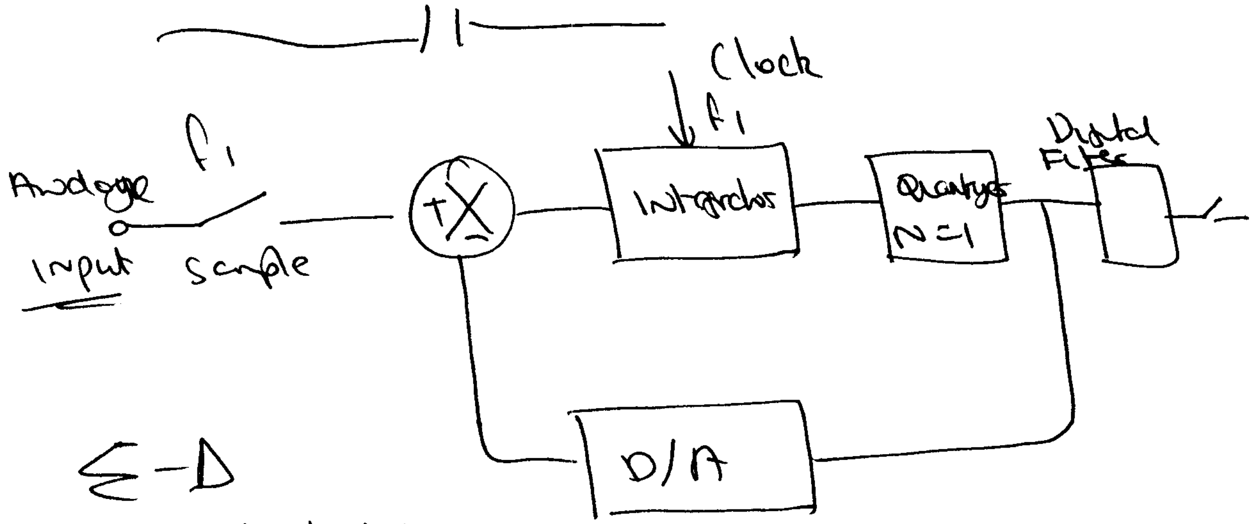
Analogue output consequently feeds into following 'bit', which

performs exactly the same function.

The process is repeated as many times as necessary to achieve desired

resolution.

(10)



Σ-Δ

modulator

Question 5 - cont

Coarse quantization at high sampling rate combined with negative feedback and digital filters to achieve increased resolution at lower sampling rates.
A means of trading resolution in time for resolution in amplitude avoiding the need for precision analogue components.

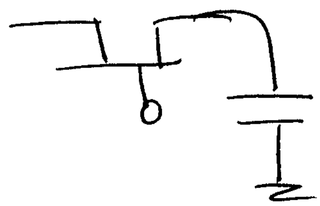
Negative fdbk produces coarse estimate that oscillates about the true value of the input, the digital filter averages the coarse estimate to give a finer approximation.
Feedback A/D + integrator →
quantization error to have a high frequency spectrum, filtered out by digital filter.
Noise shaped and all high frequency noise filtered away very high (S/N) at low frequency.

10

Question 5 cont

$DR \triangleq V_{ref} / Noise = 2^N$

Switch



Rms noise of switch capacitor

$$\sqrt{\frac{kT}{C}}$$

Assume $f_c = \frac{1}{10 R \cdot C}$, then

Solving for C gives

$$DR = 2^N = V_{ref} / \sqrt{kT\, 10 \cdot R \cdot f_c}$$

$$R_{on} = \frac{1}{2\beta (V_{SS} - V_T)} \approx \frac{1}{(2\beta \times 4)}$$

$$\beta = \left[\frac{kW}{2L}\right]$$

Can now find DR at 40kHz

10

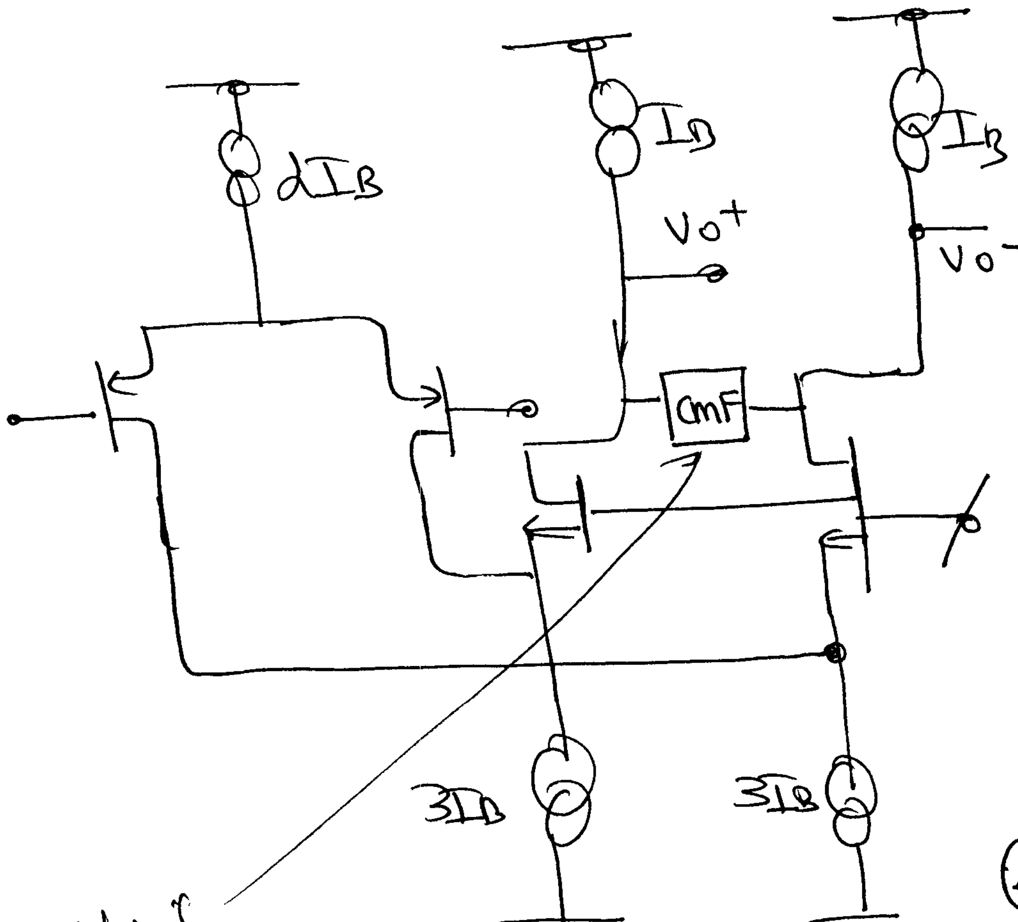
Solution should be completed.

Question 6

a)

Main advantage is that signal path is folded giving a balance between input and output allowing supply voltage to be reduced.

(2)



Extra marks if CMF circuit connected.

(4)

Question 6 - Cont

b) Single stage

Advantage :- High speed
Good phase margin

Disadvantage :- lower gain
lower CMVR/output swing.

(2)

Op-Amp 3(b)

Voltage gain $= -g_{m2} / (g_{o2} + g_{o4})$

$(g_{o2} + g_{o4}) = I_{D2} (\lambda_N + \lambda_P) =$

$5 \times 10^{-6} \times 0.05 = 2.5 \times 10^{-7} s$

$g_{m2} = 2\sqrt{\beta_2 I_{D2}} \Rightarrow \beta_2 = \frac{k_N}{2}\left(\frac{W}{L}\right)_2 = 7.5 \times 10^{-5}$

$g_{m2} = 3.87 \times 10^{-5} s$

$A_1 = \underline{\underline{-154.9}}$

$(g_{o7} + g_{o6}) = I_{D6} (\lambda_N + \lambda_P)$

$= 20 \times 10^{-6} \times 0.05$

$= 10 \times 10^{-7} \Omega^{-1}$

$g_{m6} = 2\sqrt{\beta_6 I_{D6}} \Rightarrow \beta_6 = \frac{k_P}{2}\left(\frac{W}{L}\right)_6$

$= 1.6 \times 10^{-4} A/V$

Question 6(b) continued.

$\Rightarrow g_{m6} = 1.13 \times 10^{-4}$

(7)

$A_2 = -113$

$A_{TOTAL} = A_1 A_2 = 17503$

$G\cdot B\,product = \dfrac{g_{m2}}{2\pi C_c} = \underline{4.1\,MHz}$ (2)

<u>Last Part</u>

a) To increase gain and GBproduct then W_1 and W_2 should be increased.

To increase slewrate $\Rightarrow$ I_S increased or C_c reduced (either)

(3)

b) Sequence

1/ increase I_S $\rightarrow$ slew rate increases

2/ increase W_S (1,2) $\rightarrow$ increase gain and G.B.

OR introduce R —R—||C— (improves φ margin)

feedforward compensation, eliminates RHP zero

Zero given by $Z = -g_{m6}/C_c$

with R $\Rightarrow$ $Z = -1/\left(\left(1/g_{m6} - R\right)C_c\right)$