IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2004

MSc and EEE PART III/IV: MEng, BEng.and ACGI

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Tuesday, 4 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Corrected Copy

Answer Question 1 and three others

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : C. Toumazou
Second Marker(s) : D. Haigh

This question is compulsory

1. (a) The circuit shown in Figure 1.1 is a single-stage inverting voltage amplifier using two CMOS FETs. Write a simple SPICE programme which will compute a small signal gain and phase frequency response analysis of the circuit over the frequency range 10 kHz to 10 MHz. The .OPTIONS card and the transistor model process parameters *QP* and *QN* are already built into the SPICE Library.

[10]

(b) Sketch and label typical phase and gain characteristics and indicate key values you would expect from the simulation, and outline how the phase margin of the amplifier is determined from the curves.

[6]

(c) What is the function of the passive components C_1, R_1 and R_2 shown on the circuit?

[4]

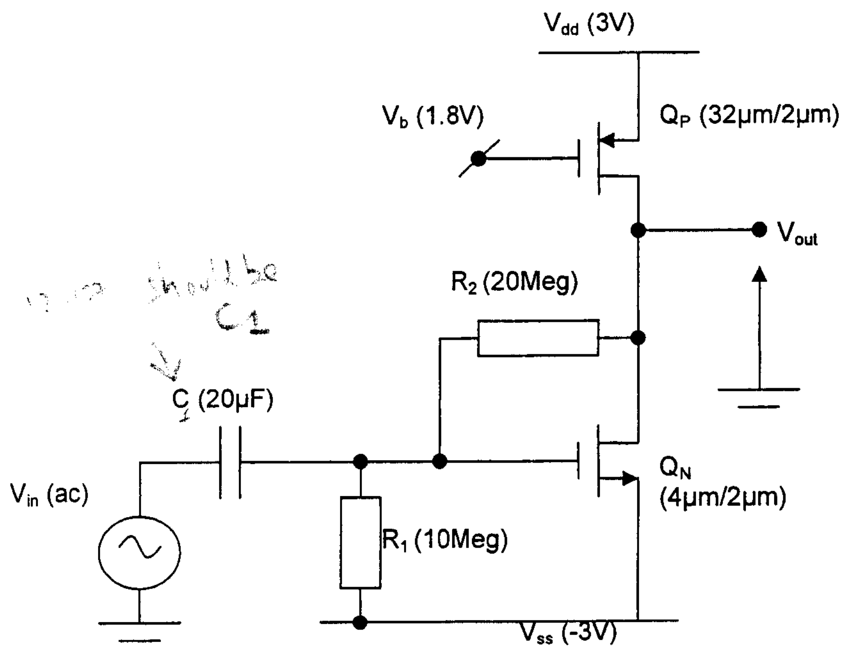

Figure 1.1

2. (a) Voltage and current-sources are key components in analogue circuit design. Sketch a typical band-gap voltage reference circuit and prove that the temperature coefficient of the output voltage V_0 is zero if $V_0 = 1.283\ V$. Assume the temperature coefficient of V_{BE} to be $-2.5mV/°C$, Boltzmanns constant $k = 1.38 \times 10^{-23}\ J/K$ and electron charge $q = 1.6 \times 10^{-19}\ C$.

[11]

(b) Calculate the fractional temperature coefficient for the constant current generator of Figure 2.1 at room temperature, given that R is a polysilicon resistor with a temperature coefficient of 1500 ppm/°C.

[5]

(c) Explain qualitatively why the four-transistor voltage potential divider of Figure 2.2 can have smaller chip area than an equivalent two-transistor voltage potential divider with the same power consumption.

[4]

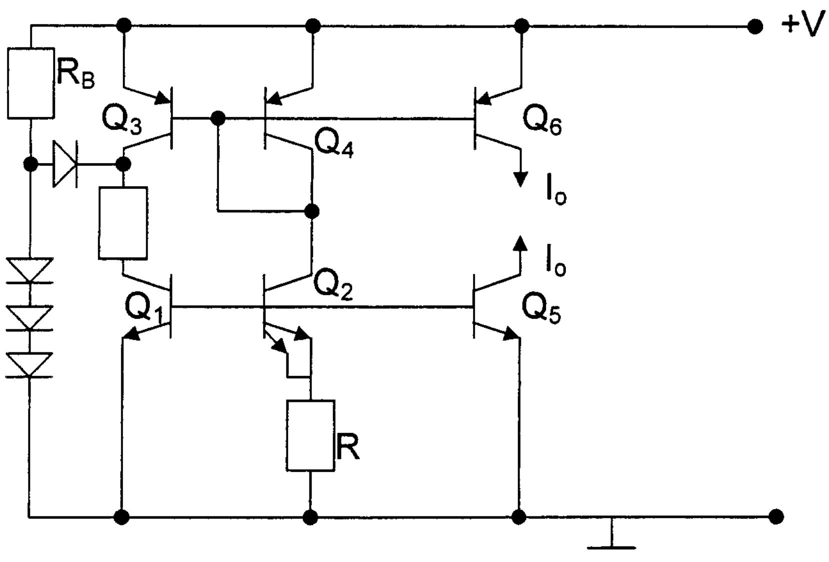

Figure 2.1

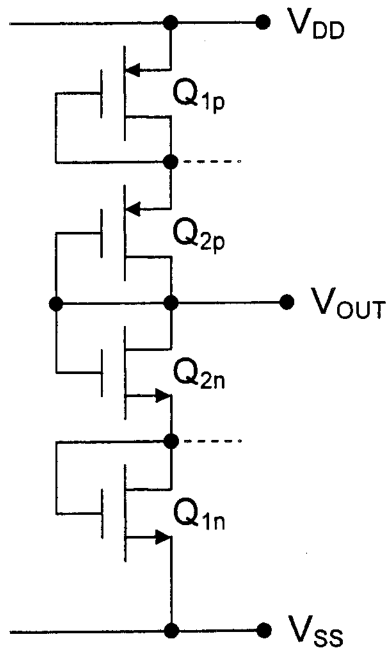

Figure 2.2

3. (a) Sketch typical circuit diagrams for a two-stage cascoded and a single-stage CMOS op-amp. Explain why the single-stage design has potentially much higher bandwidth than the two-stage design and in particular why it is not necessary to Miller compensate the single-stage architecture. Give one advantage and one disadvantage of the cascoded op-amp.

[8]

(b) Estimate the low-frequency differential voltage gain, slew rate, gain-bandwidth product and maximum positive output swing of the two-stage CMOS op-amp shown in Figure 3.1. Aspect ratios of all devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below.

[10]

(c) Explain qualitatively why the addition of a load capacitor to the output of a two-stage op-amp degrades amplifier stability, whereas an additional load capacitor connected to the output of a single-stage op-amp improves amplifier stability.

[2]

CMOS TRANSISTOR PARAMETERS

MODEL PARAMETERS	*Kp (μA/V2)*	*λ(V⁻¹)*	*V_{TO}(V)*
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

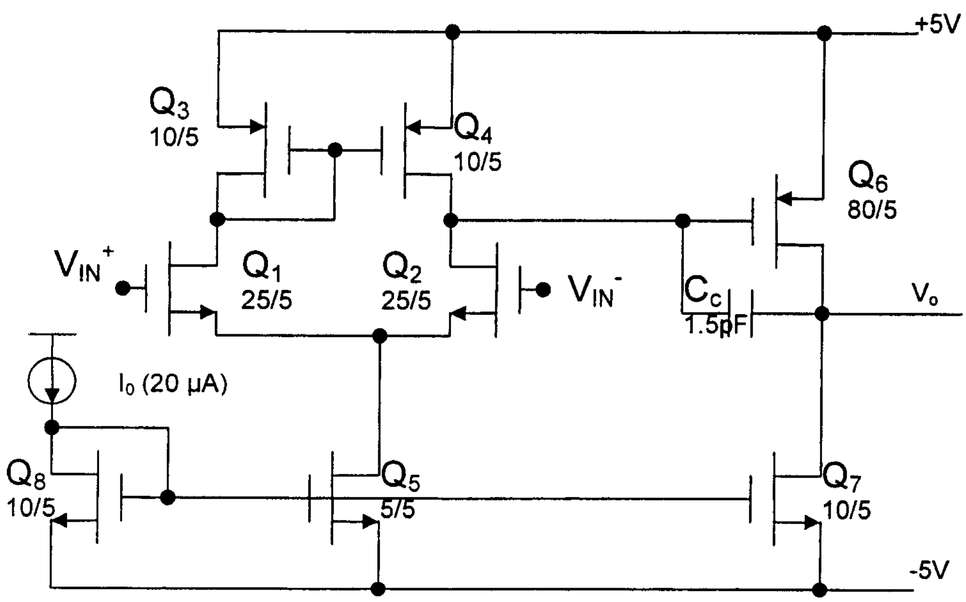

Figure 3.1

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4. (a) Under what operating conditions does the MOSFET of Figure 4.1 realise a linear floating resistor between terminals *A* and *B*? Show that under these conditions the equivalent resistance R_{AB} can be approximated by

$$R_{AB} = \frac{L}{KW(V_{GS} - V_T)}$$

stating any assumptions. All symbols have their usual meaning.

[6]

(b) Discuss three sources of non-linearity in the single MOSFET resistor realisation of Figure 4.1 and suggest one suitable circuit design to help eliminate one or more of these non-linear terms. Show all necessary circuit analysis to confirm your design.

[6]

(c) Figure 4.2 shows a fully differential continuous time integrator using a balanced double differential linear active transresistor. Derive an expression for the time constant of the integrator. You may ignore all bulk effects, and assume all MOSFETs are operating in the triode region.

[8]

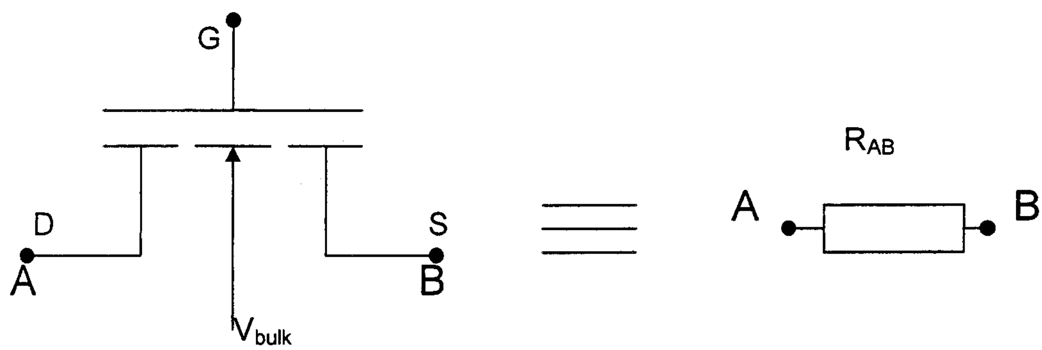

Figure 4.1

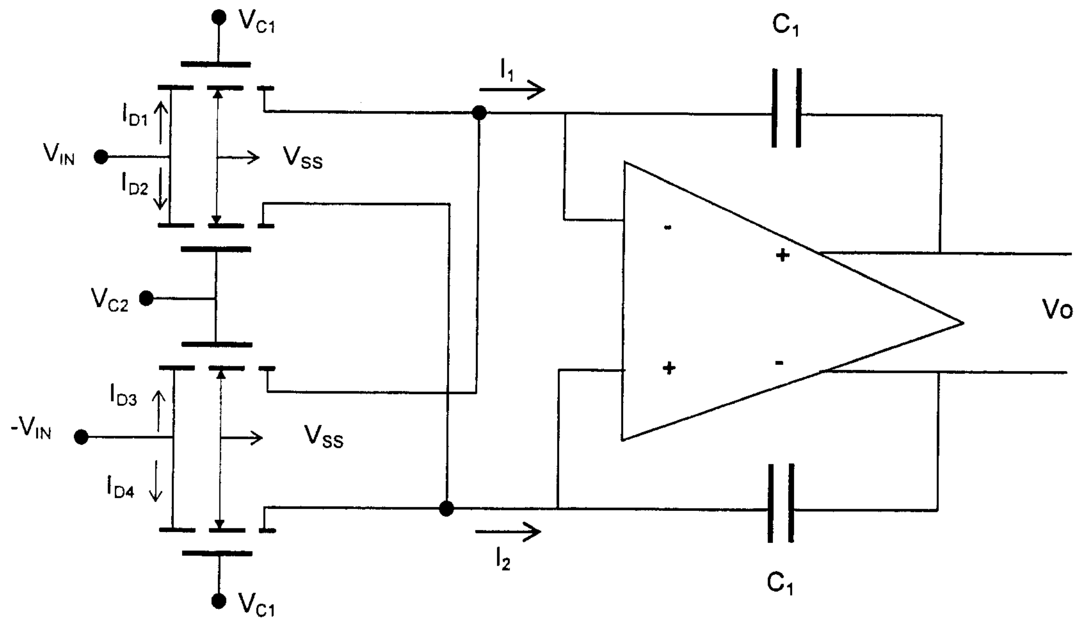

Figure 4.2

5. (a) Using two switches and a capacitor, sketch a circuit that will synthesise an active resistor. Given that the switches are driven by a pair of non-overlapping clocks running at a frequency of 100 kHz, estimate the value of a capacitor to give a resistance of 10 MΩ.

[5]

(b) A fundamental limitation imposed on the Dynamic Range (*DR*) of any high performance A/D converter will ultimately be switch noise. Prove that the fundamental limit is given by

$$DR = \frac{V_{ref}}{\sqrt{(10kTRf_c)}}$$

where V_{ref} is the reference voltage, k is Boltzmann's constant, T is absolute temperature, R is switch resistance and f_c is the maximum clock frequency of the switch. You may assume that the system settles in $10t$ (where t = time constant), over one period of the clock frequency.

[7]

(c) Figure 5.1 shows one section of a switched capacitor ladder filter. Based on this filter structure, design a 3rd-order Chebyshev low-pass filter with a cut-off frequency of 5 kHz and a 1.0 dB pass band ripple. Assume a clock frequency of 100 kHz. Passive component values for the LC prototype, normalised to 1 rad/s, are $C_1 = C_3 = 2.0236$, $L_2 = 0.994$. In your analysis assume all integrators to be lossless.

[8]

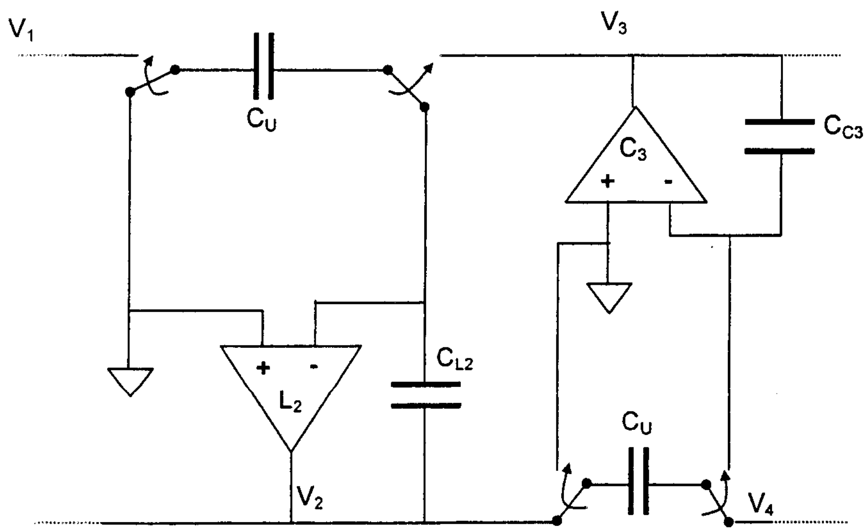

Figure 5.1

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6. (a) Give one advantage and one disadvantage of each of the three CMOS current mirror circuits shown in Figures 6.1, 6.2 and 6.3.

[6]

(b) Give reasons why it is important for CMOS current mirrors to have a high output resistance and high output voltage swing. For the current mirror of Figure 6.2 derive this voltage swing in terms of device threshold voltage V_T, clearly stating any assumptions you make.

[7]

(c) Using reasonable engineering approximations, derive an expression for the small-signal output resistance of the current mirror of Figure 6.3. In your small-signal analysis you need consider only transistors *Q1*, *Q2* and *Q3*. What is the function of transistors *Q5*, *Q6* and *Q7*?

[7]

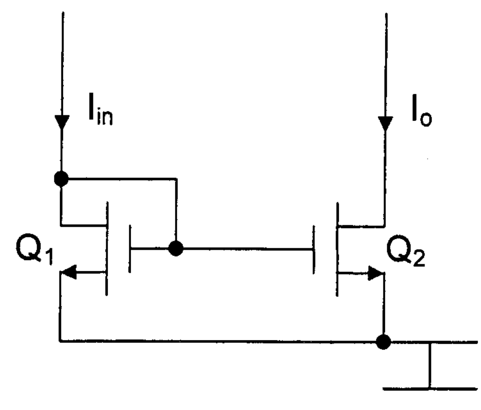


Figure 6.1

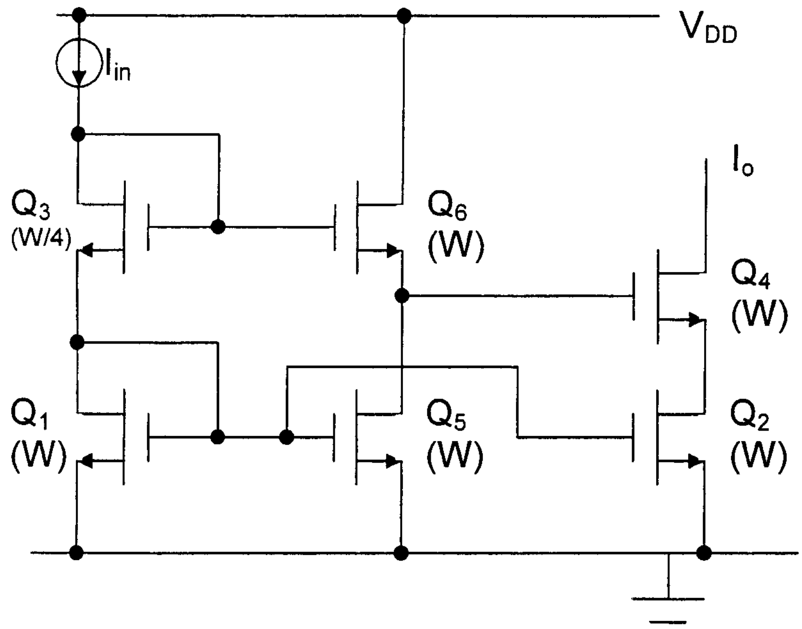


Figure 6.2

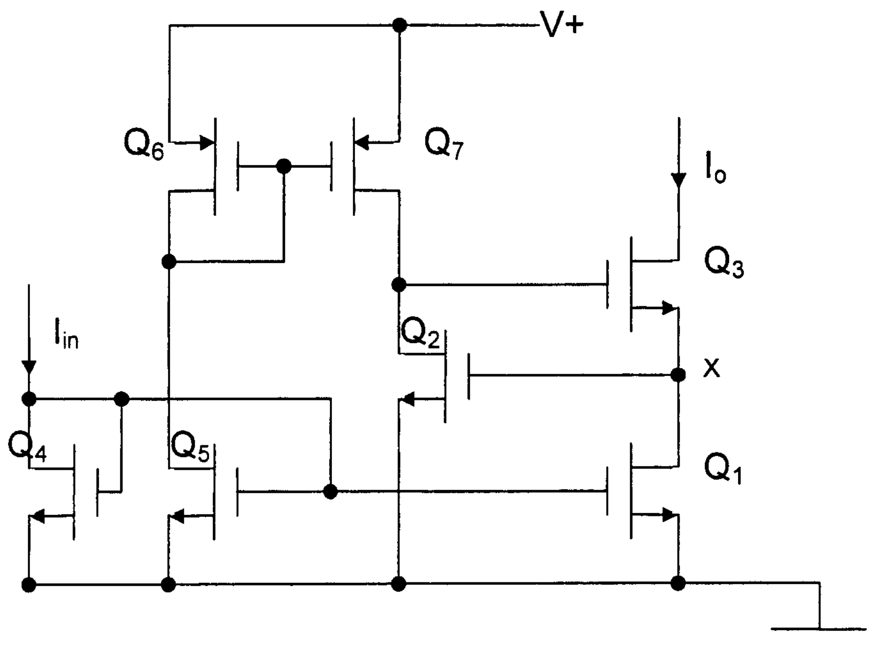
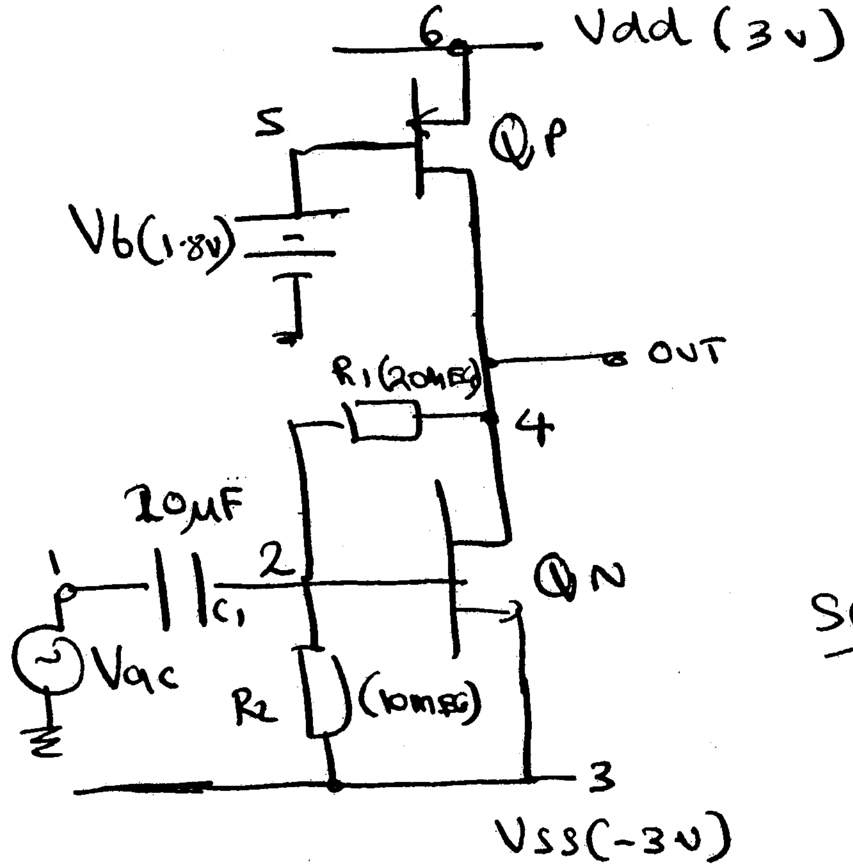


Figure 6.3

Q1 Compulsory



SPICE NETLIST

. Title inverting cmos Amplifier.

Component netlist

```
C1   1  2     20 E-6
R1   2  4     20 MEG
R2   2  3     10 MEG
M1   4  2  3  QN   W=4u   L=2u
M2   4  5  6  QP   W=32u  L=2u
Vdd  6  0  3V
Vss  3  0  -3V
Vb   5  0  1.8V
Vac  1  0  ac 1
```

sources

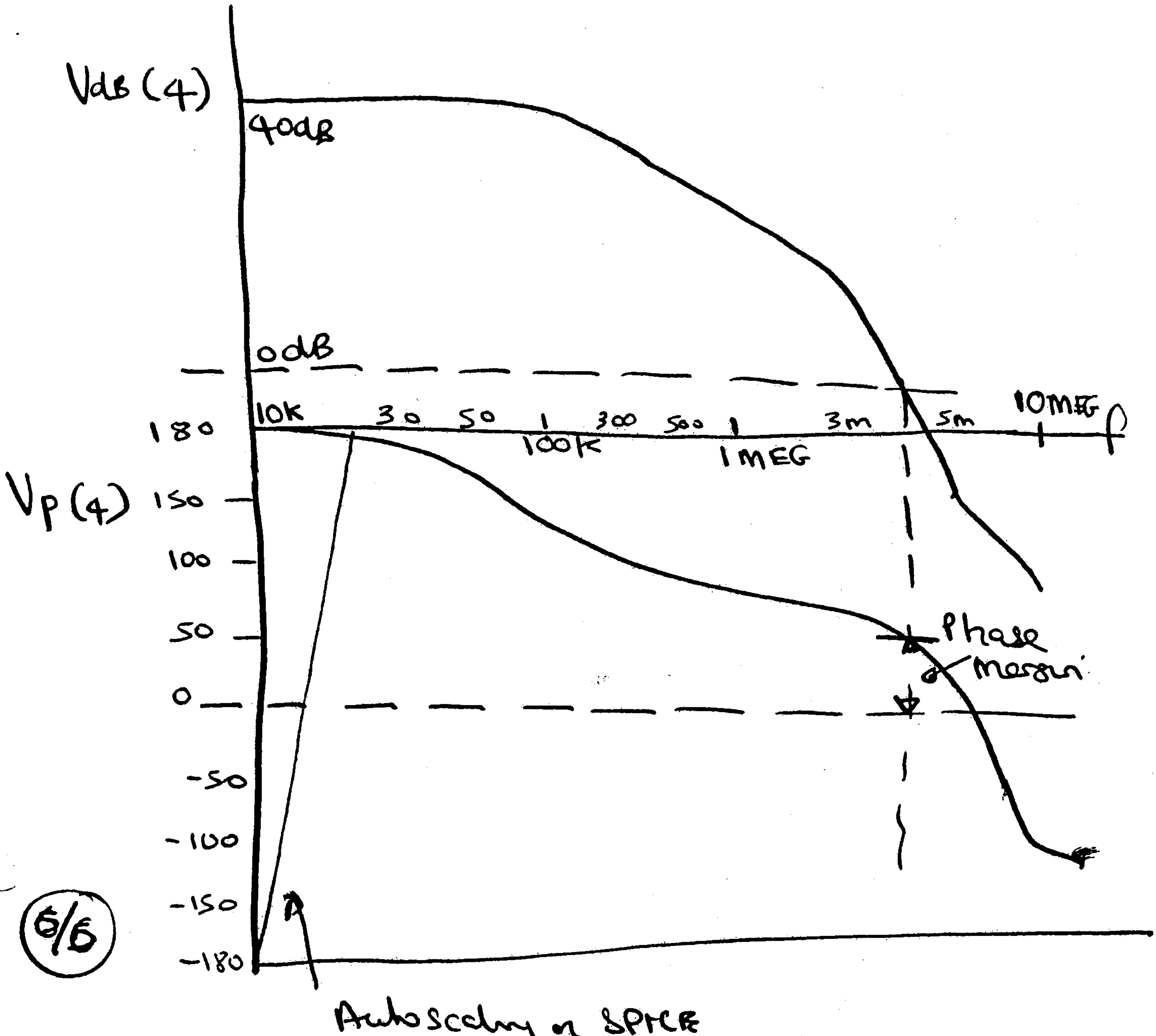
```
. model QN, QP
. op all
. option post
. ac dec 10 10K 10MEG
. PRINT ac VdB(4)
. PRINT ac Vp (4)
. END.
```

Analysis Print

10/10

Q1 (cont)

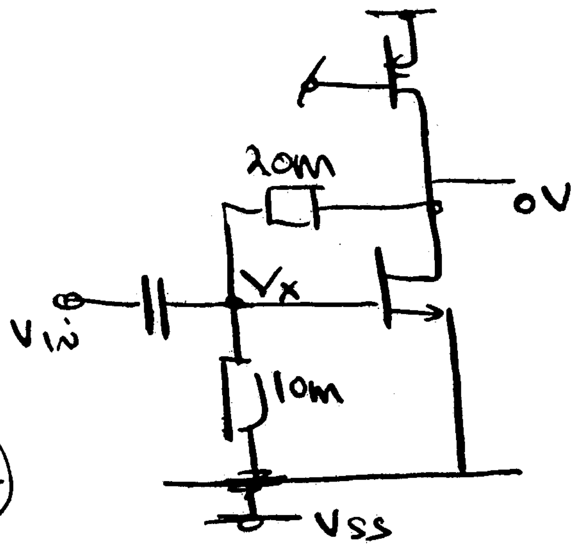
Typical SPICE output plot.



6/6

Likely that theory and simulated will differ because of approximations generally assumed in theory. Models for transistors in SPICE have inaccuracy. Also inaccuracy in parameter extraction for SPICE models.

Large passive components used for DC biasing. Sets high impedance output of amplifier at dc bias close to 0V. Large values of R used so that input and output impedance levels are not loaded. 20µF capacitor used to ac couple input. Typically



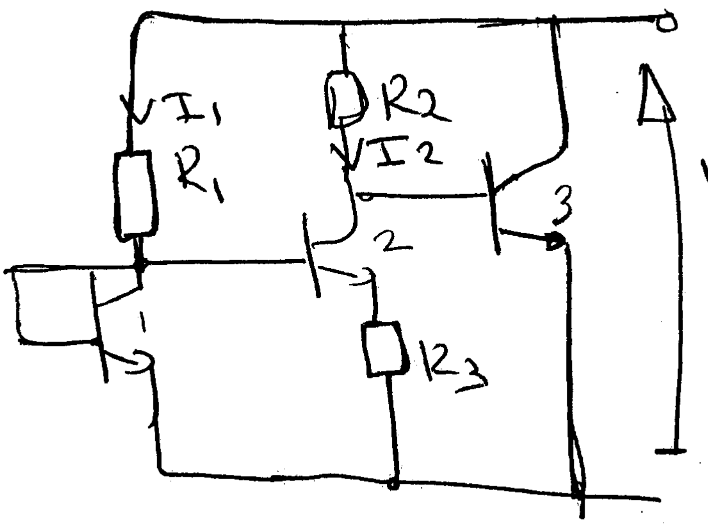
$$V_x = V_{ss} + \left(\frac{-V_{ss}}{3}\right)2$$

$$= \left[\frac{V_{ss}}{3}\right]$$

4/4

Total 20/20

Q2



Bandgap.

5/5

$V_{BE1} = V_{BE2} + I_2 R_3$

$\beta >> 1$

Since $V_{BE1} - V_{BE2} = V_T \ln(I_1/I_2)$

then $V_o = V_{BE3} + R_2/R_3 \, V_T \ln(I_1/I_2)$

$V_T \ln(I_3/I_S)$ → assume Non-temp

For $dV_o/dt = 0$, then dV_{BE3}/dT

$= \frac{V_T}{T} \frac{R_2}{R_3} \ln\left(\frac{I_1}{I_2}\right)$

Since $\frac{dV_{BE}}{dt} = -2.5 mV/°C$, $\frac{V_T}{T} = \frac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}}$

then $\left(\frac{R_2}{R_3}\right) \ln\left(\frac{I_1}{I_2}\right) = 29$ and so

6/6

$V_o = 1.283V$

For PTAT temperature coefficient of V_T cancels with negative temp coefficient of Resistor

Q2 cont

5

5/5

$\therefore T_{CF} = \frac{1}{V_T} \partial V_T/\partial T - 1/R \, \partial R/\partial T$

$= 1/T - 1500 \times 10^{-6}$ @ Room T $= 1833$ ppm/°C

Figure 2(b).

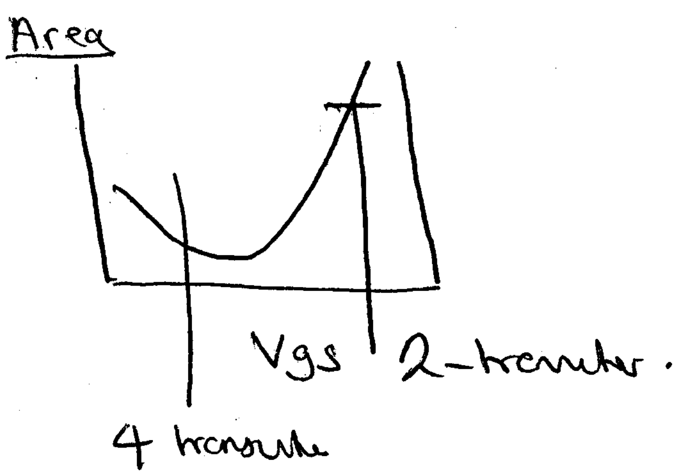
Since $I = \frac{KW}{2L}(V_{GS} - V_T)^2$

then if V_{gs} is small $\approx V_T$
then (W/L) large.

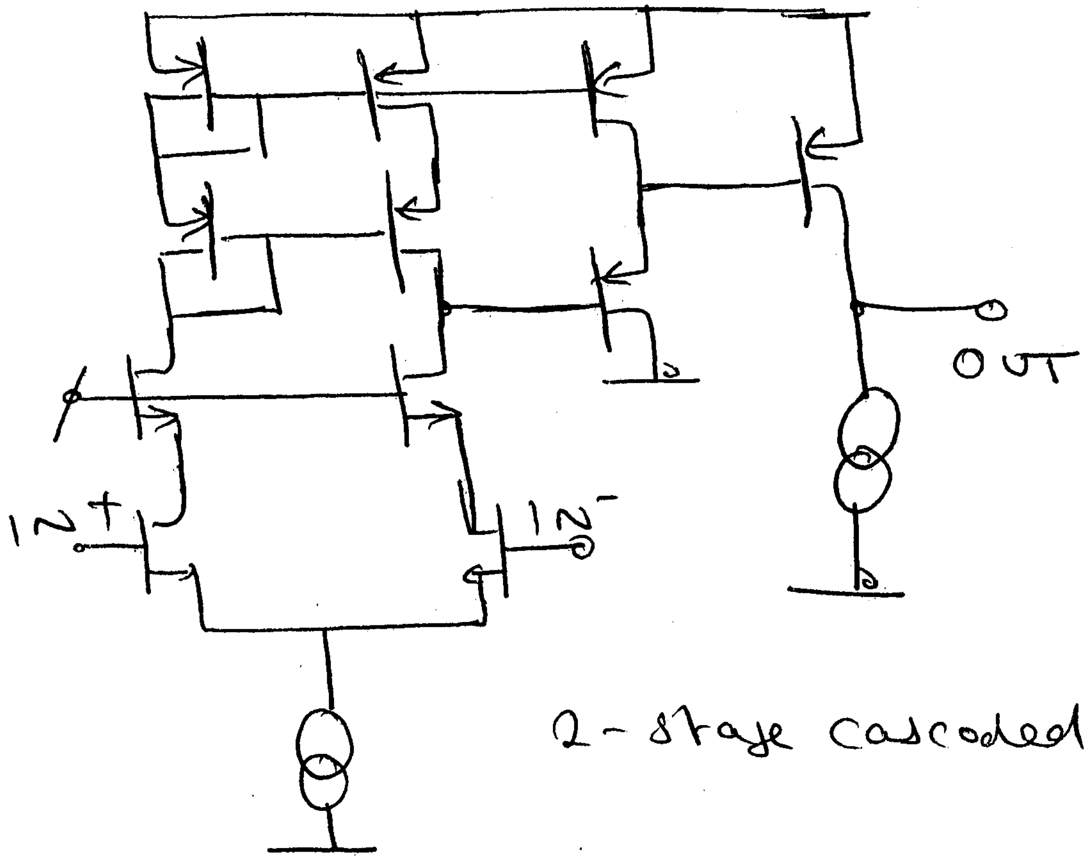
If $V_{gs} >> V_T$
then (W/L) small
small (W/L) gives large chip area

2(c)
$\therefore$ Two transistor P.D
has larger V_{GS} / transistor
than four transistor P.D for same
supply.

4/4

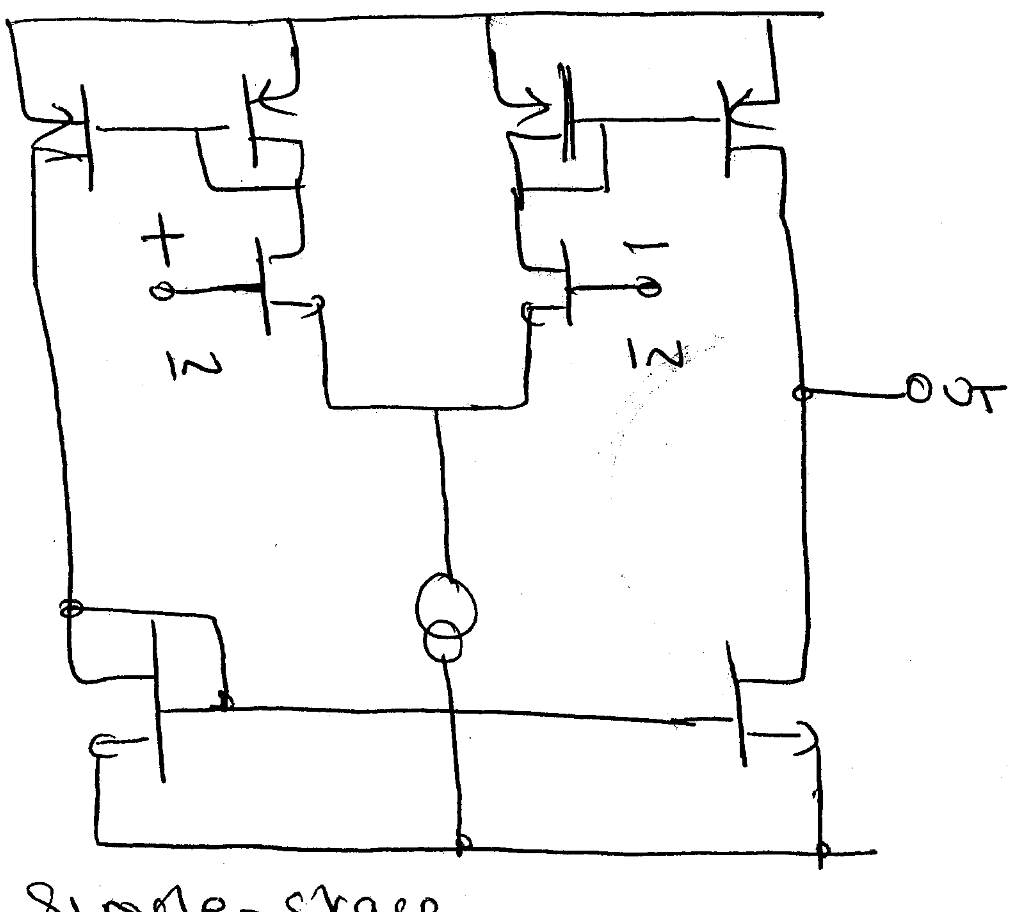


Q3



3/3

2-stage cascoded.



3/3

Single-stage.

Q3 (Cont)

In a single-stage the main high impedance node is at the output. Compensation is then provided via a load capacitance at the output. The internal poles at the lower impedance nodes are now secondary and will only affect the phase margin of the amplifier.

In a two-stage design, the requirement for a single high internal impedance to achieve voltage gain means that the amplifier requires internal frequency (Miller) compensation to be stable. Because of this compensation the bandwidth is reduced.

2/2 The main advantage of a cascoded op-amp is voltage gain, the main disadvantage is CMVR or signal swing limitations.

Op-Amp

2/2 $A_{v1} = -g_{m2}/(g_{o2}+g_{o4})$

$(g_{o2}+g_{o4}) = I_{D2}(\lambda_N+\lambda_P) =$

$5\times10^{-6}\times0.05 = 2.5\times10^{-7}\,\Omega^{-1}$

2/2 $g_{m2} = 2\sqrt{\beta_2 I_D} \Rightarrow \beta_2 = \frac{k_N}{2}\left(\frac{W}{L}\right)_2 = 7.5\times10^{-5}\,A/V$

$g_{m2} = 3.87\times10^{-5}\,S, \quad A_1 = -154.9$

$A_2 = -g_{m6}/(g_{o7}+g_{o6})$

Q3 - Cont. (8)

$$(g_{o6}+g_{o7}) = I_{D6}(\lambda_{Np}+\lambda_N) = 20\times10^{-6}\times0.05 = 10\times10^{-7}\,\Omega^{-1}$$

1/1

$$g_{m6} = 2\sqrt{\beta_6 I_{D6}} \Rightarrow \beta_6 = \frac{k_p}{2}\left(\frac{W}{L}\right)_6 = 1.6\times10^{-4}\,A/V$$

$$g_{m6} = 1.13\times10^{-4}, \quad A_2 = 113$$

$$A_{TOTAL} = A_1 A_2 = 17503$$

2/2

$$G.B_p = g_{m2}/2\pi C_c = 4.1\,MHz$$

1/1

$$S.R = I_o/C_c = \left(\frac{10}{4.5}\right) V/\mu s$$ X

MAXIMUM SWING

$$[5V - V_{SD(6)}] \Rightarrow [5 - (V_{SG6} - V_T)]$$

For schwahen,

Assume $V_{SG6} = V_{GS4} = V_{SG3}$

$$V_{SG3} = \left(V_{T(3)} + \sqrt{\frac{I_o}{4\beta_3}}\right)$$ 10μA

2/2

$$\beta_3 = \left(\frac{KW}{2L}\right)_3 \Rightarrow \text{maximum swing} \approx 4V$$

In 2-stage load is 2nd pole hence reducing load increases stability.
With single-stage load forms dominant pole hence reducing load increases bandwidth.

2/2

Q4 Assumption is that if ($V_{DS} \approx 0$) or ($V_{DS} << (V_{GS} - V_T)$) device acts in linear region. From

$$I_D = \frac{KW}{L}\left[(V_{GS}-V_T)V_{DS} - V_{DS}^2/2\right](1+\lambda V_{DS})$$

for $V_{DS} << (V_{GS}-V_T)$, then $\lambda V_{DS} << 1$

So $$I_D = \frac{KW}{L}(V_{GS}-V_T)V_{DS}$$

6/6 OR $R_{AB} = V_{DS}/I_D = L/(KW(V_{GS}-V_T))$

Three sources of Non-linearity

(i) limited due to V_{BS} changing V_T for negative V_{DS} due to body effect.

ie $V_T = V_{T0} + \gamma\left[\sqrt{-V_{BS}+2\phi_F} - \sqrt{2\phi_F}\right]$

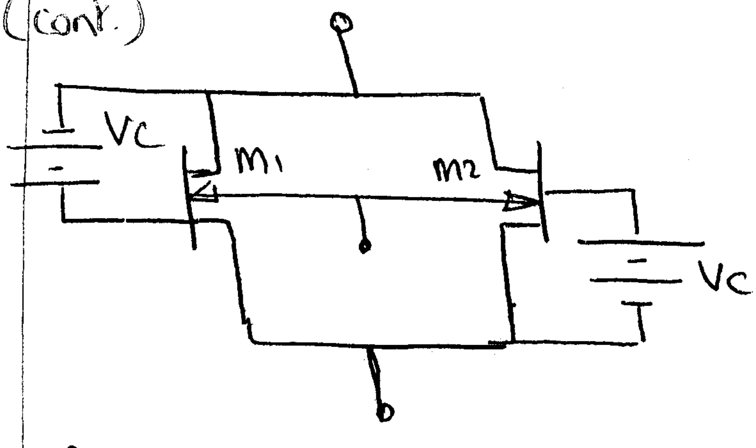
γ = bulk threshold parameter

ϕ_F = Fermi-level potential

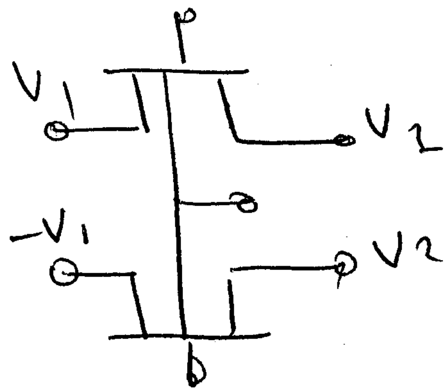
(ii) limited due to V_{DS} approaching ($V_{GS} - V_T$) hence saturation region for large positive V_{DS}.

(iii) For large values of V_{DS} the $V_{DS}^2/2$ term comes in making the results quite non-linear.

4/4

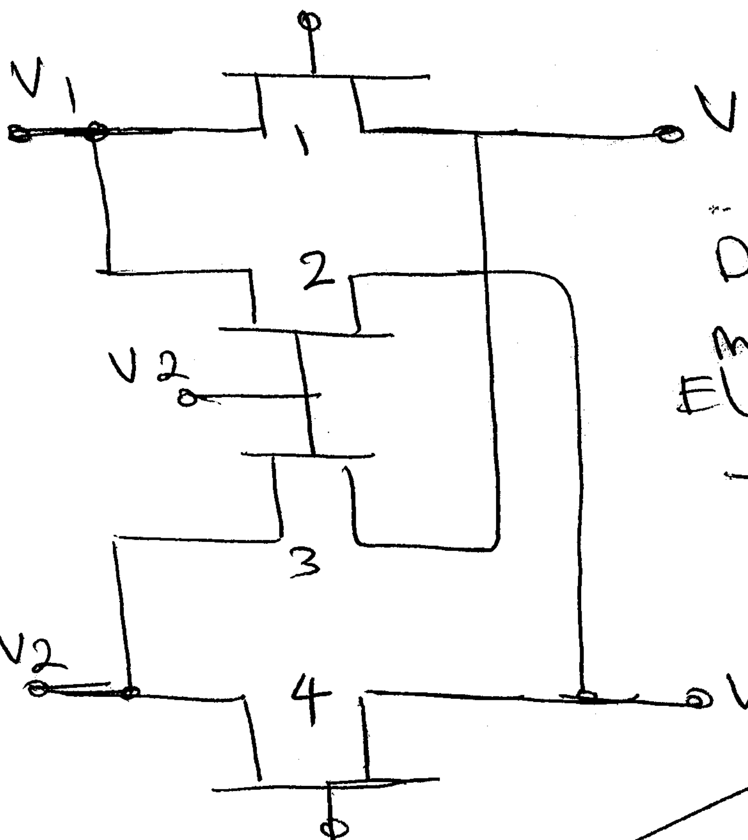


Parallel circuit - eliminates $V_{ds}^2/2$ term.



Differential scheme

Effects of V_{DS} cancelled.



Double differential MOS.
Eliminates
- V_{DS} and V_T term.

ANY one of these will do!

2/2

Q4 (cont)

Double differential integrator

$$I_{D1} = 2\beta\left[(V_{C1} - V - V_T)(V_1 - V) - \tfrac{1}{2}(V_1 - V)^2\right]$$

$$I_{D2} = 2\beta\left[(V_{C2} - V - V_T)(V_1 - V) - \tfrac{1}{2}(V_1 - V)^2\right]$$

$$I_{D3} = 2\beta\left[(V_{C2} - V - V_T)(V_2 - V) - \tfrac{1}{2}(V_2 - V)^2\right]$$

$$I_{D4} = 2\beta\left[(V_{C1} - V - V_T)(V_2 - V) - \tfrac{1}{2}(V_2 - V)^2\right]$$

Expanding it can be shown that :-

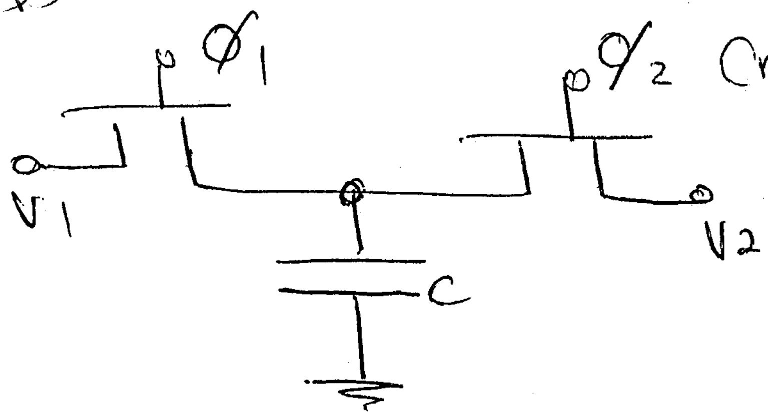
$$(V_1 - V_2)/(I_1 - I_2) = 1/2\beta(V_{C1} - V_{C2}) = R$$

Independent of both V_T and V_{DS} terms

Hence $\tau = \frac{2CR}{\cancel{2}} = \left[\frac{C}{\cancel{2}\beta(V_{C1} - V_{C2})}\right]$

8/8

Q5



Excess charge $\Delta Q = C[V_1 - V_2]$

$$I_{av} = \frac{\Delta Q}{T} = \frac{C[V_1 - V_2]}{T}$$

$$R_{eq} = \frac{(V_1 - V_2)}{I_{av}} = T/C$$

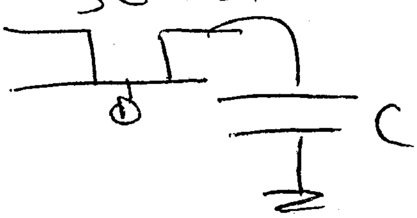
Assuming $f_{clock} \gg f_{signal}$ (3/3)

then $R_{eq} \approx \frac{1}{f_c C} \approx 10M\Omega$

$f_c = 100kHz$, $C = 1pF$ (2/2)

$DR = V_{ref} / Noise = 2^N$

switch

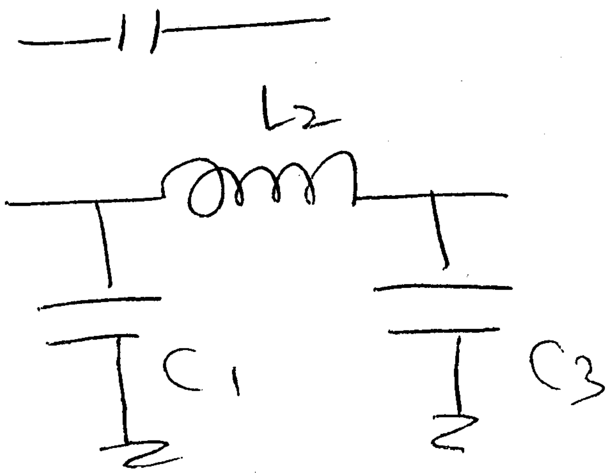


Noise $\sqrt{\frac{KT}{C}}$ (3/3)

Q5 (cont) Assume $f_c = \dfrac{1}{10 \cdot R \cdot C}$ 2/2

then solving for C gives

$$DR = 2^N = V_{reff} \Big/ \sqrt{KT\,10 R f_c}$$ 2/2



Solution for LCR prototype.

Inductance transformation $(L_2/R_s)\, f_s = C_{L2}/C_u$ 2/2

capacitor transformation $= C_{C3}/C_u = f_c R_s C_3$ 2/2

where R_s is normalized during scaling resistor,

Assuming $R_s = 1$,

$$\left.\begin{aligned} C_{C1}/C_u &= f_c C_1 \\ C_{C3}/C_u &= f_c C_3 \\ C_{L2}/C_u &= f_c L_2 \end{aligned}\right\} \text{general transformation.}$$

Q5 cont

Table values of C_1, L_2 and C_3 are normalized to 1 rad/s $\div 2\pi f_p$ ($f_p = 5kHz$) (14)

$$C_1 = C_3 = 2.0236 / (2\pi\, 5\times10^3) = 6.44\times10^{-5} F$$

$$L_2 = 0.994 / (2\pi\, 5\times10^3) = 3.164\times10^{-5} F$$

No termination resistors (ie loss in input and output interface.) 2/2

assume $C_u = CR_i' = CR_o = 1pF$

then $C_{C1} = C_{C3} = \underline{6.44 pF}$

$C_{L2} = \underline{3.164 pF}.$ 2/2

TOTAL 10/20

Q6

Figure 6(a) – Simple-mirror

Advantages – High frequency performance
– High output swing.

2 – Disadvantage – Very inaccurate

Figure 6(b) – High swing cascode

Advantage – Higher output swing than cascode

2 – Dissadvantage – Complex, poor frequency response.

Figure 6(c) – Regulated Cascode Mirror.

2 – Advantage – Highest output swing
Highest output impedance

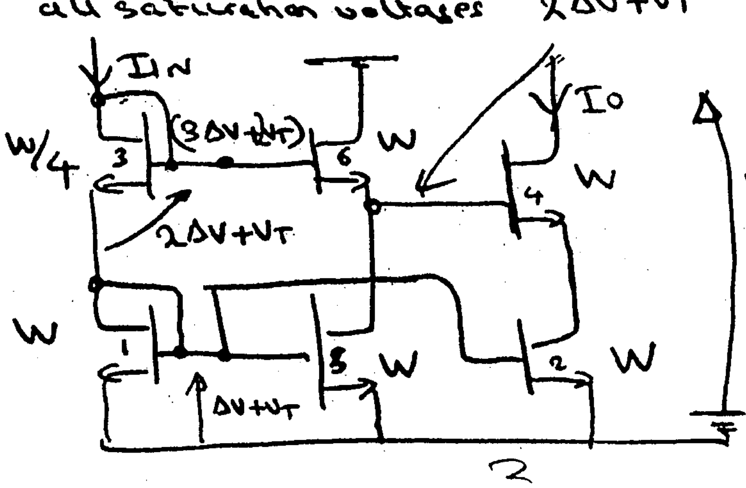
Dissadvantage – inaccuracy of simple mirror.
– feedback leading to potential instability.

2 – For precision analog signal processing on the same chip as digital circuitry it is important that the analog part can perform well in the low supplies of the digital parts. In most cases the precision of the analogue part will be determined by the quality of a current-source, active loads of amplifiers etc, it's thus important that the mirror maintains its high output resistance over a wide supply margin.

OUTPUT SWING

Circuit including all saturation voltages

5 –



Assume equal L's,
$I_O = I_{IN}$.

$\beta_1 = \beta_2 = \beta_4 = \beta_5 = \beta_6 = \beta$

$\beta_3 = \beta/4$

$\therefore V_{sat(3)} = 2(V_{gs} - V_T)$

Note $(\Delta V = V_{gs} - V_T)$

OUTPUT SWING = $\underline{\underline{2\Delta V}}$

2

Q6 (cont)

Output resistance of Regulated Cascode :-

Transistor Q3 cascodes Q1, hence output resistance due to Q3 is $R_{o3} \approx r_{ds1}\, g_{m3}\, r_{ds3}$. Transistor Q2 senses change in voltage at node (x) and reduces these changes by the loop gain of the amplifier (Q2 and IB), and this further increases the output resistance of the circuit to

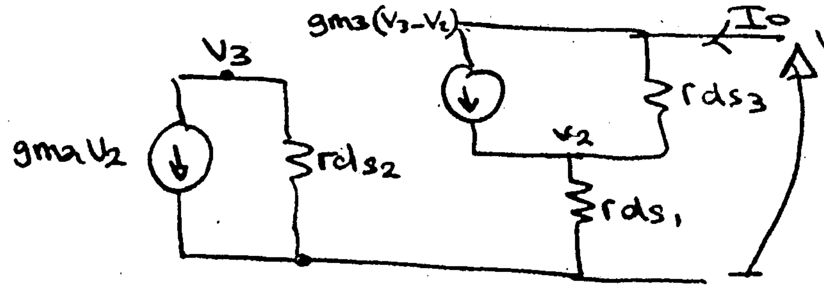
$$R_{out} \approx R_{o3}\, g_{m2}\, r_{ds2} \approx g_{m2}\, g_{m3}\, r_{ds1}\, r_{ds2}\, r_{ds3}$$

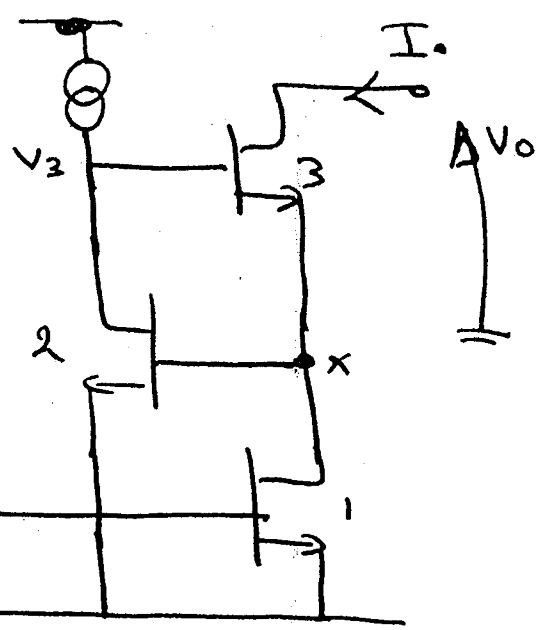
assuming matched devices then,

$$R_{out} \approx g_m^2\, r_{ds}^3 \text{ or } (g_m^2 / g_o^3).$$

ALTERNATIVE

small-signal model :- OUTPUT - PORTION





$$V_o = (I_o - g_{m3}(V_3 - V_2))\, r_{ds3} + V_2$$

$$V_2 = I_o\, r_{ds1}$$

$$V_3 \approx -g_{m2}\, r_{ds2}\, V_2$$

$$\therefore V_o = I_o\, r_{ds3} + g_{m2}\, g_{m3}\, r_{ds2}\, r_{ds3}\, r_{ds1}\, I_o + g_{m3}\, r_{ds1}\, r_{ds3}\, I_o + I_o\, r_{ds2}$$

Since 2nd term is the more dominant then,

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$$V_o / I_o \approx R_{out} \approx g_{m2}\, g_{m3}\, r_{ds2}\, r_{ds3}\, r_{ds1}$$

$$\boxed{\approx g_m^2\, r_{ds}^3}$$

Function of Q5, Q6 and Q7 is to ensure that V_{gs2}, hence saturation voltage of Q1 tracks changes in input current. Simply Q6 and Q7 mirror the input current which [illegible]