Paper Number(s): **E3.01**
AC1

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2002

MSc and EEE PART III/IV: M.Eng., B.Eng. and ACGI

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Monday, 22 April 10:00 am

There are SIX questions on this paper.

Answer FOUR questions.

Time allowed: 3:00 hours

Examiners responsible:

First Marker(s): Toumazou,C.

Second Marker(s): Lucyszyn,S

Corrected Copy

Special instructions for invigilators:	None
Information for candidates:	None

1. *Figure 1* shows two popular biasing schemes typically used in analogue integrated systems. Briefly outline the main feature of each of these circuits. [3]

For the bandgap voltage reference circuit of Figure 1(a), show that $\delta V_0 / \delta T = 0$ (where T is temperature) if $(R_2/R_3)\ln [I_1/I_2] = 29$ for $V_0 = 1.283$ V.

Assume the temperature coefficient of V_{BE} to be -2.5mV/°C, the collector current of transistor Q_3 is 100 μA and the device saturation current is $I_s = 1.2 \times 10^{-13}$ A. Boltzmanns constant $k = 1.38 \times 10^{-23}$ J/K and the electron charge is $q = 1.6 \times 10^{-19}$ C. [6]

Calculate the fractional temperature coefficient in ppm/°C for the current generator of *Figure 1(b)* at room temperature, given that R is a polysilicon resistor with a temperature coefficient of 1500 ppm/°C. [3]

Show that the circuit of *Figure 1(b)* can be developed into a current source with output current directly proportional to absolute temperature and virtually independent of supply voltage. It is likely that on power-up the output current will fall into a zero current state. Sketch a suitable start-up circuit that ensures that this condition will not occur and explain the operation of the circuit. [8]

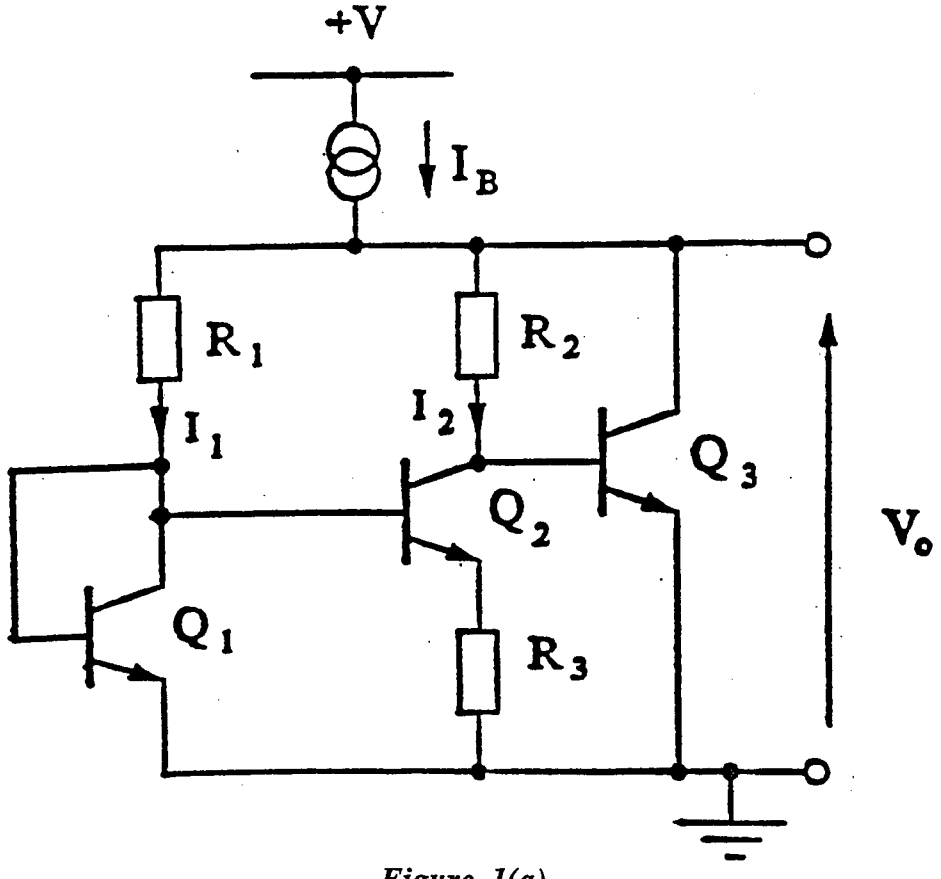

Figure 1(a)

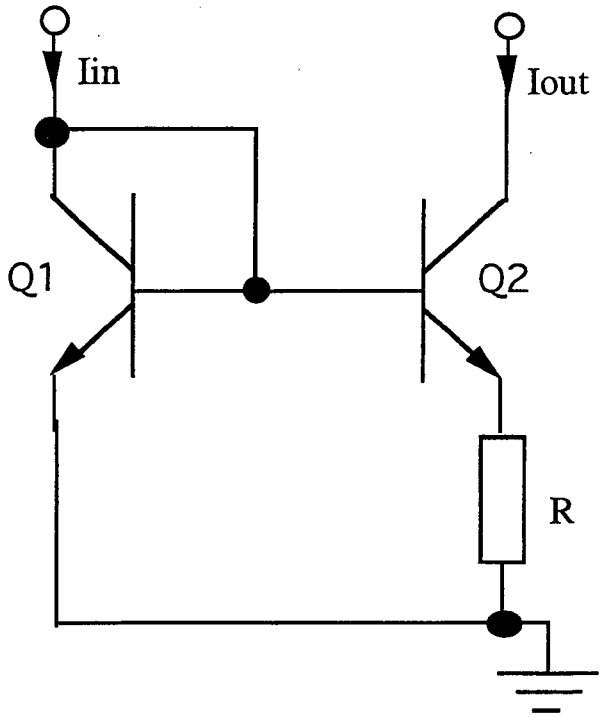

Figure 1(b)

2. Give two advantages of differential output compared to single ended output op-amps, and briefly explain what is meant by the term 'common-mode feedback' in relation to differential output circuits. [5]

Sketch the basic architecture of a fully differential folded cascode CMOS op-amp with common-mode feedback circuitry included and give an approximate expression for small signal voltage gain of the amplifier. To simplify your circuit assume all current sources are ideal. What is the main advantage of this architecture over the classical 2-stage op-amp ? [8]

An application of the fully differential op-amp is the tunable continuous-time integrator shown in *Figure 2* employing an input differential MOS resistor arrangement. Derive an expression for the time-constant of the integrator. You may ignore all bulk effects and assume all mosfets are operating in their triode-region. [7]

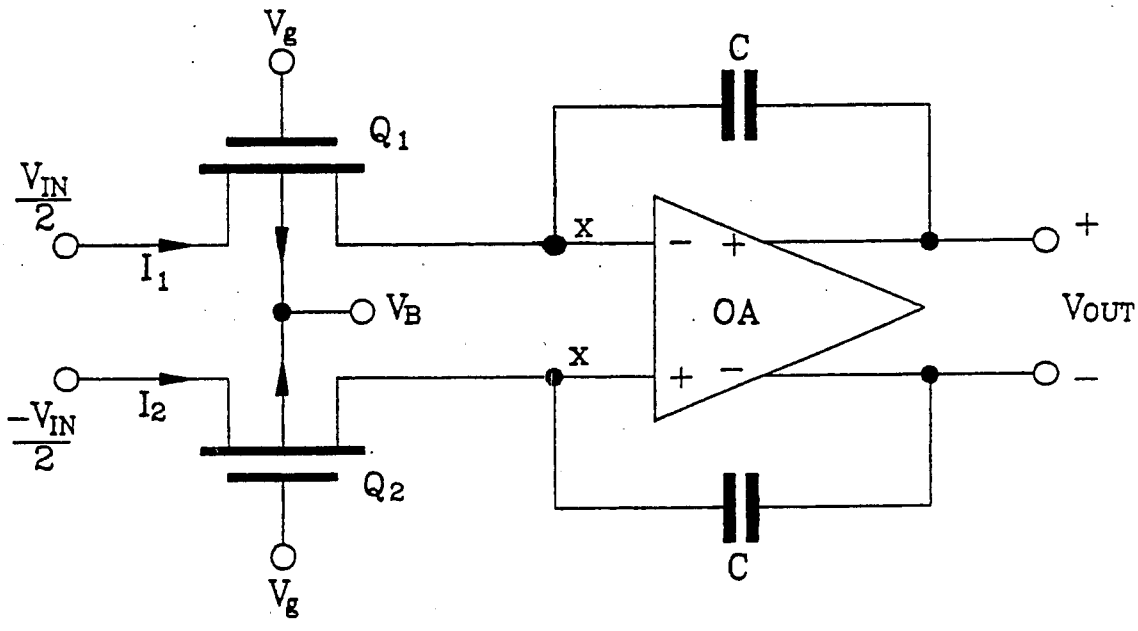

Figure 2

3. Give one advantage and one disadvantage of switched capacitor filters relative to integrated continuous-time filters. [3]

Figure 3 shows three typical switched capacitor circuits. In all the circuits you may assume the switches are driven by non-overlapping clocks with a clock frequency higher than the maximum input signal frequency. Also assume the switches are ideal.

For the switched capacitor resistor of *Figure 3(a)*, estimate the clock frequency required to realise a resistor of 10MΩ between terminals 1 and 2. What is the main advantage of this resistor over a standard passive resistor ? [4]

Derive an expression for the transfer function of the differential integrator of *Figure 3(b)*. Explain why the circuit is parasitic insensitive. [6]

Sketch and label a typical switched capacitor integrator frequency response, clearly indicating the effect on the ideal response when the input frequency approaches the integrator clock frequency. [2]

Figure 3(c) shows the basic design of a 3rd-order Chebyshev low pass ladder filter with a cut-off frequency of 5 kHz. Assume a clocking frequency of 100 kHz. From the circuit, estimate normalised passive component values for the original double-terminated LC prototype of the filter. All values should be normalised to 1 rad/s. [5]

Values of $C_{C1} = C_{C3} = 5.08$ pF and $C_{L2} = 3.49$ pF

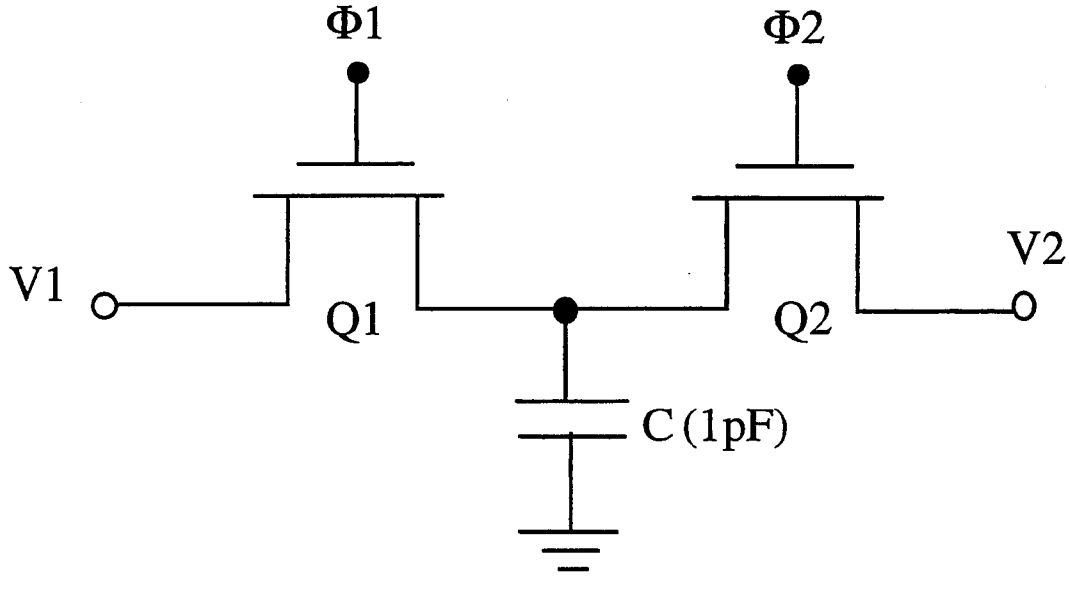

Figure 3(a)

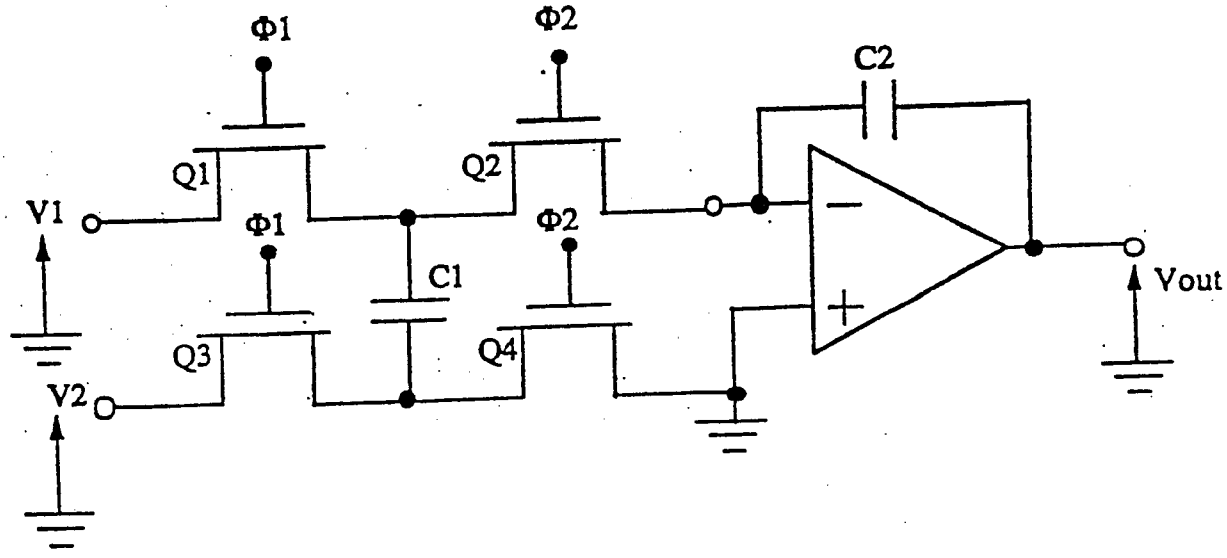

Figure 3(b)

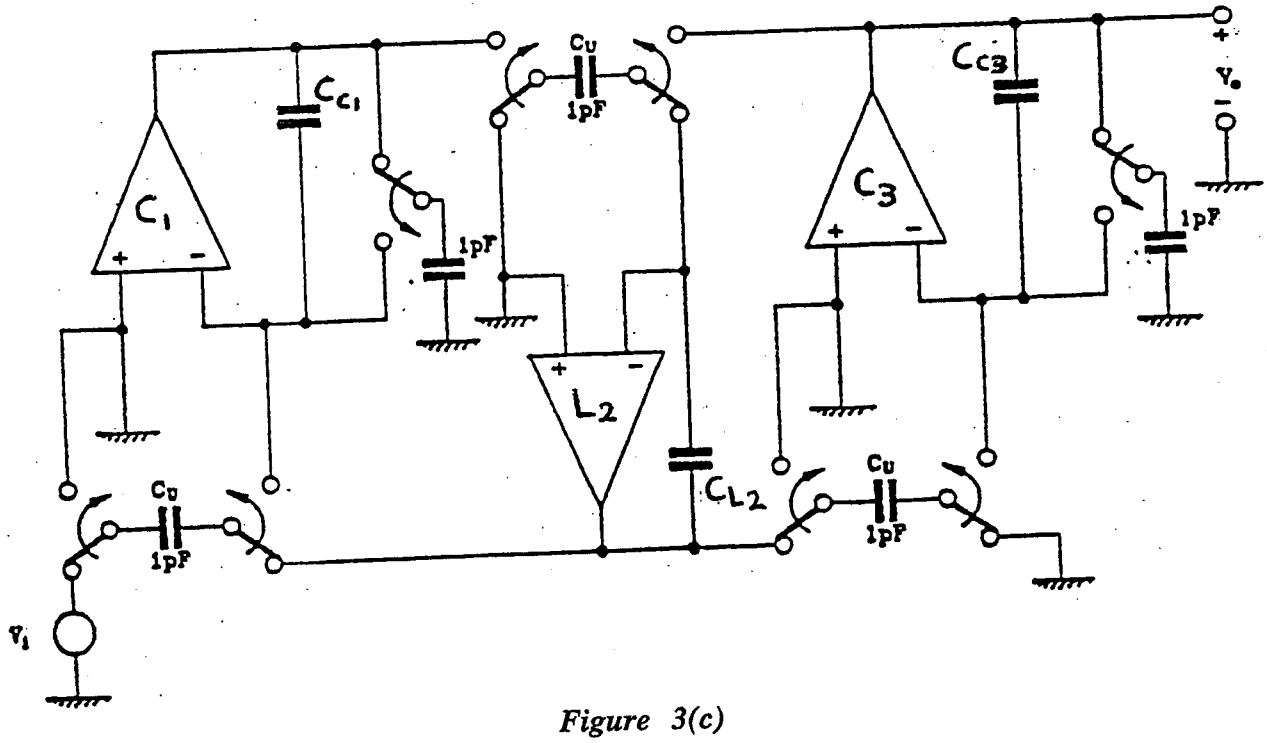

Figure 3(c)

4. State one advantage and one disadvantage of a single stage over a two-stage op-amp. [2]

Figure 4 shows a two-stage CMOS op-amp. Estimate the low-frequency differential voltage gain and gain-bandwidth product of the amplifier. Aspect ratios of all devices are shown on the circuit diagram. Assume all bulk effects are negligible. The device model parameters are given below. [8]

With the addition of one NMOS and PMOS transistor show how the amplifier gain of *Figure 4* can be significantly increased. What is the performance penalty for this increase in gain ? [3]

Finally, sketch a single stage push-pull op-amp architecture and explain why load capacitance improves amplifier stability. Sketch a suitable gain-frequency plot to aid your explanation. [7]

CMOS TRANSISTOR PARAMETERS

MODEL PARAMETERS	Kp ($\mu A/V^2$)	λ (V^{-1})	V_{To} (V)
PMOS	20	0.03	- 0.8
NMOS	30	0.02	1.0

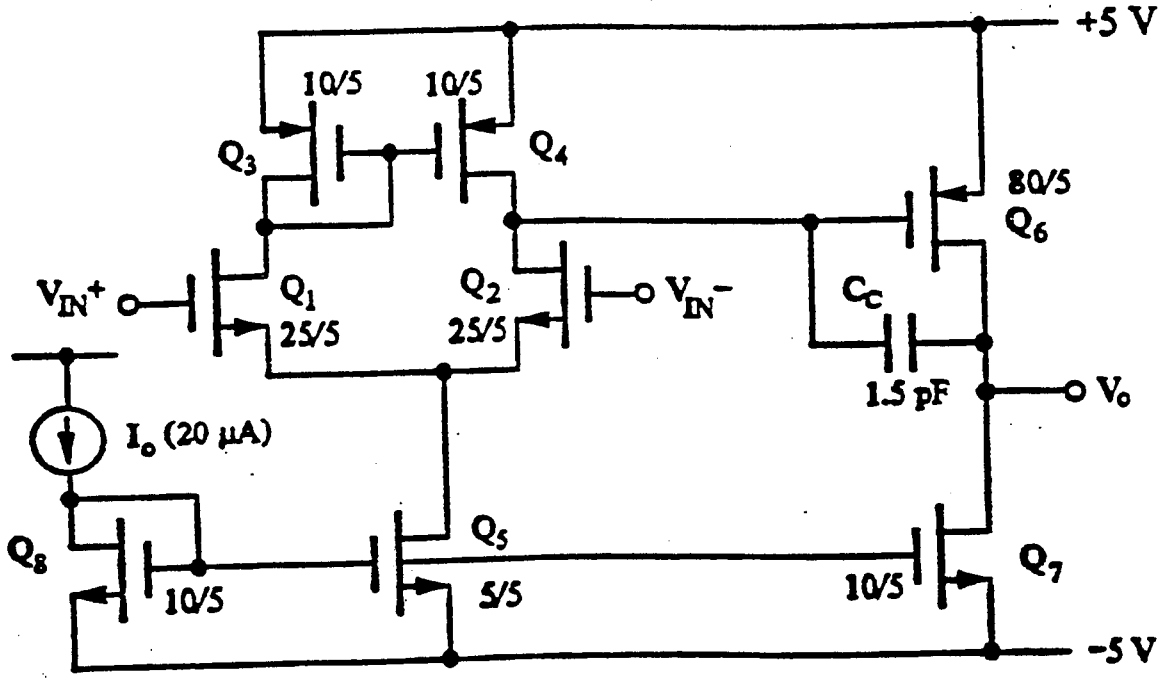

Figure 4

5. In mixed-mode ASIC design, the process technology is to be chosen to optimise digital performance specifications. Give one example of the constraints this places upon analogue circuit design performance. [2]

A fundamental limitation imposed on the Dynamic Range (DR) of any high performance A/D converter will ultimately be switch noise. Prove that the fundamental limit is given by,

$$DR = \frac{V_{ref}}{\sqrt{(10kTRf_c)}}$$

where V_{ref} is the reference voltage, k is Boltzmann's constant, T is absolute temperature, R is switch resistance and f_C is the clock frequency of the switch. You may assume that the system settles in 10τ (where τ is the time constant), over one period of the clock frequency. [6]

A very high resolution analogue-to-digital converter is the oversampling converter sometimes referred to as the sigma-delta modulator. Sketch a typical architecture for such a converter and explain its principles of operation, in particular the feedback noise shaping mechanism.

[12]

6. Under what operating conditions does the MOSFET of *Figure 6*(a) realise a linear floating resistor between terminals A and B ? Show that under these conditions the equivalent resistance R_{AB} can be approximated by

$$R_{AB} = \frac{L}{KW(V_{GS} - V_T)}$$

stating any assumptions. All symbols have their usual meaning. [5]

Discuss three sources of non-linearity in the single MOSFET resistor realisation of *Figure 6(a)* and suggest one suitable circuit design to help eliminate one or more of these non-linear terms. Show all necessary circuit analysis to confirm your design. [5]

For the current mirror of *Figure 6*(b) estimate the minimum output voltage while still maintaining saturated devices. Derive this voltage swing in terms of device threshold voltage V_T, clearly stating any assumptions you make. [6]

Finally, sketch a regulated cascode current-source and explain why the output resistance of the current source is higher than a standard cascode mirror. [4]

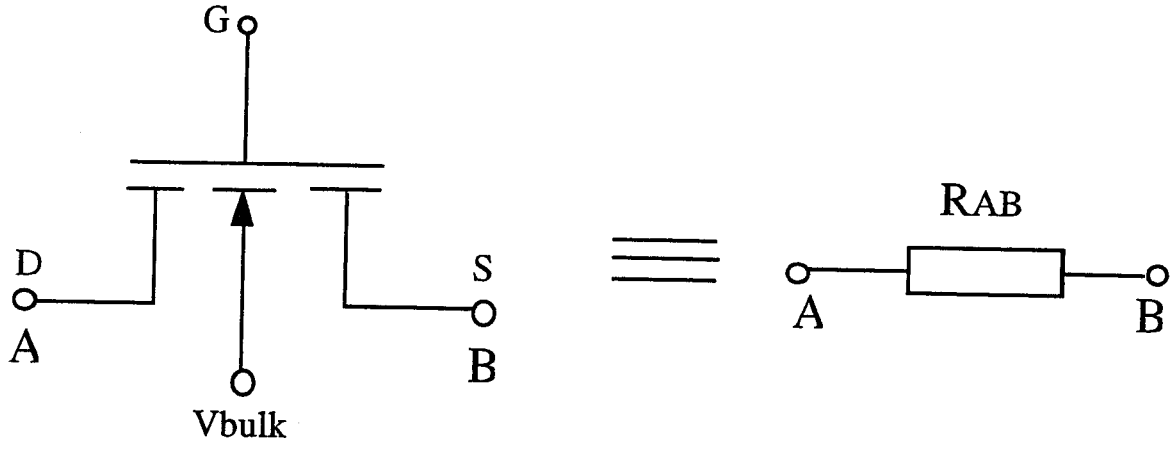

Figure 6(a)

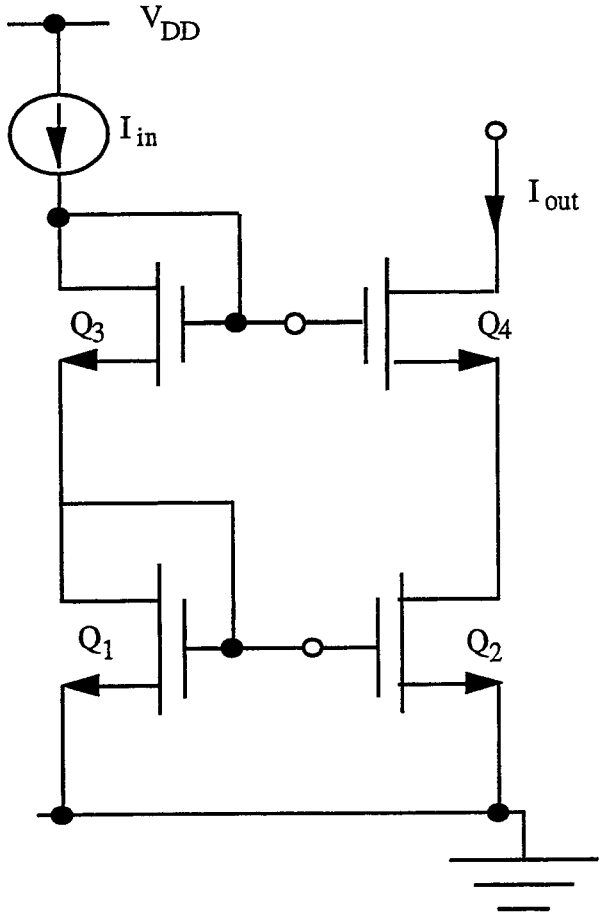

Figure 6(b)

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Q.1

Figure 1a – Bandgap voltage-reference circuit has almost zero temperature coefficient. Used mainly as stable voltage reference in ICs. (2)

Figure 1b – PTAT (Proportional to Absolute temperature) current generator. Output current is virtually insensitive to power supply voltage. Used as main biasing circuit in most precision ICs. (2)

For bandgap reference :- $V_{BE1} = V_{BE2} + I_2 R_3$ $(\beta \gg 1)$

since

$$V_{BE1} - V_{BE2} = V_T \ln(I_1/I_2)$$

then $V_O = V_{BE3} + R_2/R_3 \, V_T \ln(I_1/I_2)$

/ $V_T \ln[I_3/I_S]$ → assume room temp.

for $dV_O/dt = 0$, then $dV_{BE3}/dT = \frac{V_I}{T} \frac{R_2}{R_3} \ln \frac{I_1}{I_2}$

Since $\frac{dV_{BE}}{dt} = -2.5\,mV/°C$, $\frac{V_T}{T} = \frac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}}$

then $\left(\frac{R_2}{R_3}\right) \ln\left(\frac{I_1}{I_2}\right) = 29$ and so

(8)

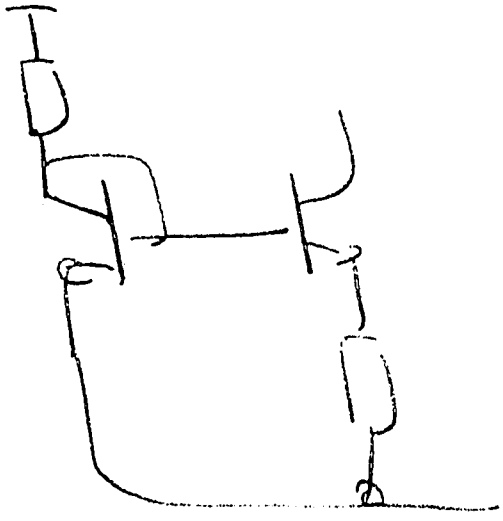
$$V_O = 1.283\,V.$$

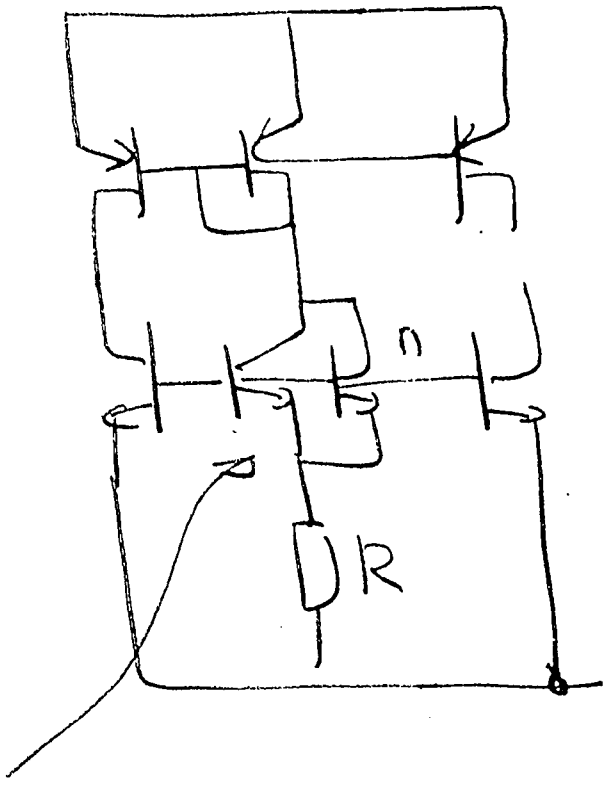
For PTAT temperature coefficient of V_T cancelled with negative temperature coefficient of resistor

$$\therefore TCF = \frac{1}{V_T} \cdot \partial V_T/\partial T - 1/R \; \partial R/\partial T$$

(4) $$= 1/T - 1500 \times 10^{-6} \text{ @ Room } T = 1833 \text{ ppm/°C}$$

ORIGINAL



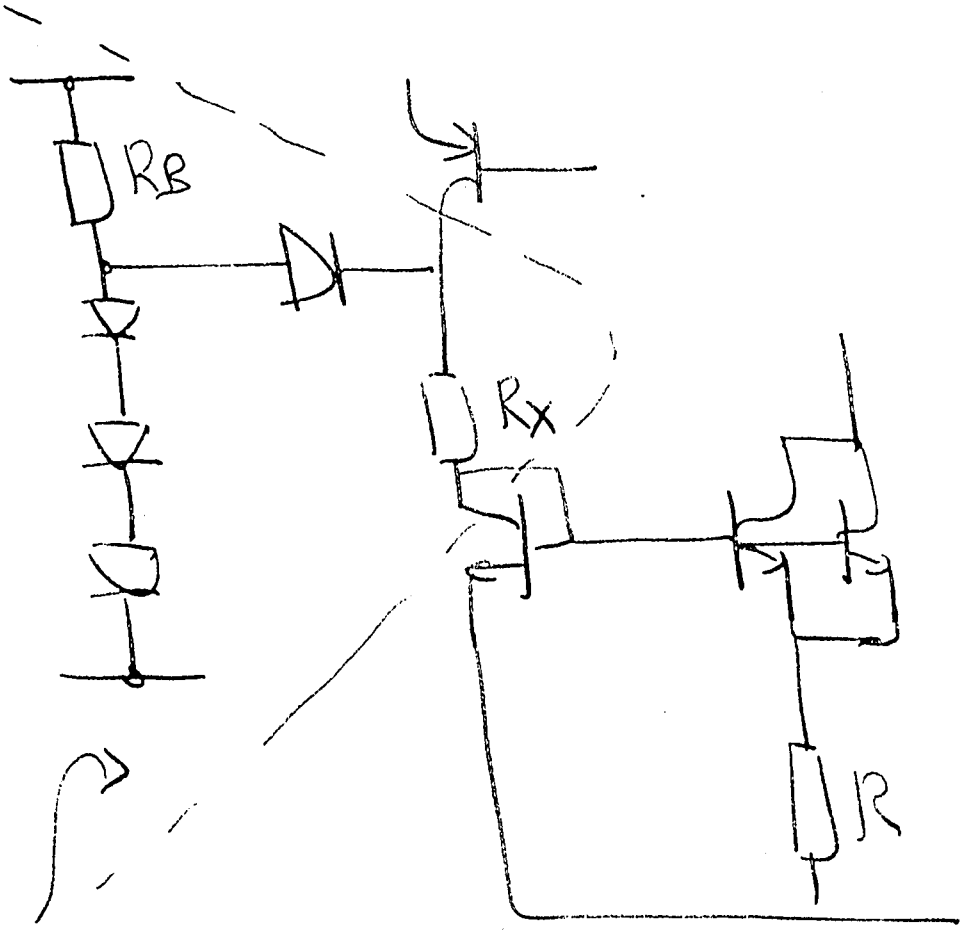


(3) n emitter

Self biasing scheme requires start-up circuit.

$$I_O = V_{TLn}[n/R]$$

Automatic Start-up Circuit.



(6) Start-up Circuitry

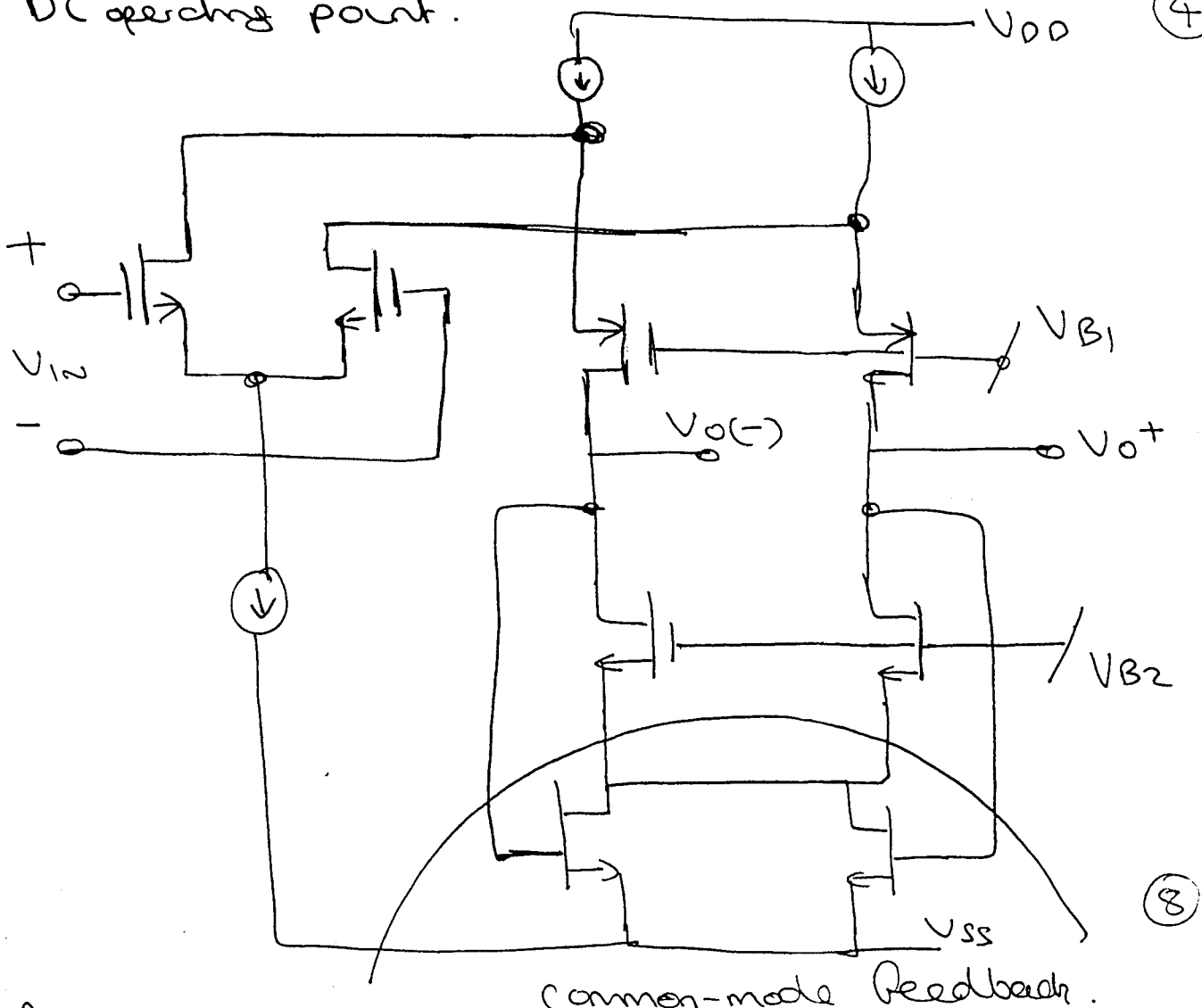
25

Question 2.

Advantages of Differential output.

① Rejection of common-mode output signals.
② Reduces power supply noise.
③ Cancels offsets, non-linearity, noise etc. (2)

Differential output amplifiers with high gain have no way of stabilization since outputs are undefined. Common-mode feedback - sensing common-mode output and via negative feedback controls the current through the output stage to ensure output voltages do not drift from quiescent DC operating point. (4)



Common-mode feedback.

Main advantage

Single dominant pole at output hence high frequency performance, no internal compensation (frequency) required. (2)

Question 2 continued.

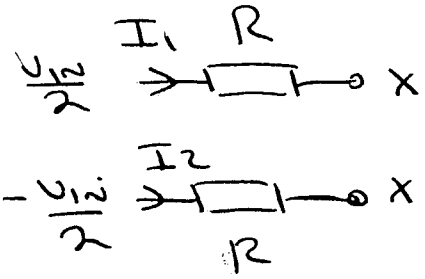
Differential Resistor

Assume all FETs are in their triode region then

$$I_1 = 2\beta\left(\left[V_g - V_x - V_T\right]\left(\frac{V_{IN}}{2} - V_x\right) - \frac{1}{2}\left(\frac{V_{IN}}{2} - V_x\right)^2\right)$$

$$I_2 = 2\beta\left(\left[V_g - V_x - V_T\right]\left(-\frac{V_{IN}}{2} - V_x\right) - \frac{1}{2}\left(-\frac{V_{IN}}{2} - V_x\right)^2\right)$$

equivalent



$$I_1 = \left(\frac{V_{IN}}{2} - V_x\right)/R$$

$$I_2 = \left(-\frac{V_{IN}}{2} - V_x\right)/R$$

$$I_1 - I_2 = \frac{V_{in}}{R} \Rightarrow R = \left(\frac{V_{IN}}{I_1 - I_2}\right)$$

$I_1 - I_2 = 2\beta\left[V_g - V_T\right]V_{in}$ all other terms cancel

$$\therefore R = \frac{1}{2\beta\left(V_g - V_T\right)}$$

Net result is a linear differential resistor whose value can be controlled by V_g.

Time constant of integrator

$$\tau = RC = C/2\beta\left(V_g - V_T\right) \quad -*$$

(9)

My slip-up

TOTAL (25/25)

3. Advantages of SC filters

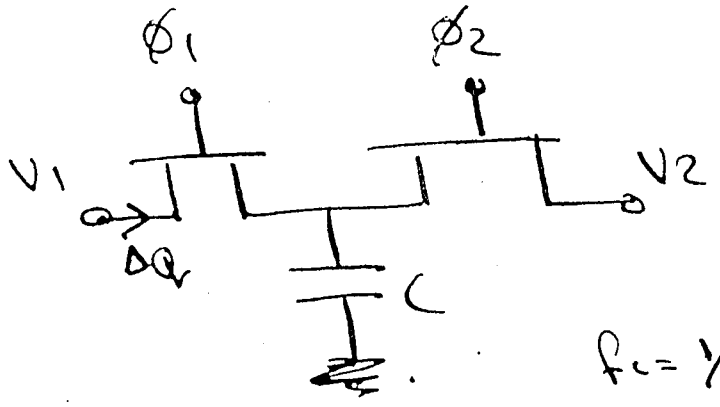
(i) Precision – sets by capacitor ratios < 0.1%
(ii) Exploit MOS VLSI technology [integration]
(iii) Use closed loop op-amps (stable)
(iv) No external tuning.

(2/2)

Disadvantages

(i) Low frequency
(ii) Clocks / clock generators
(iii) Effects on clock feedthrough etc.

(2/2)



Excess charge

$\Delta Q = C[V_1 - V_2]$

$i_{AV} = \frac{\Delta Q}{T} = \frac{C[V_1 - V_2]}{T}$

$\therefore R_{eq} = \frac{V_1 - V_2}{i_{av}} = \frac{T}{C}$

$f_c = 1/T$

Non-overlapping clock ⇒ assuming $f_{clock} \gg f_{signal}$

then

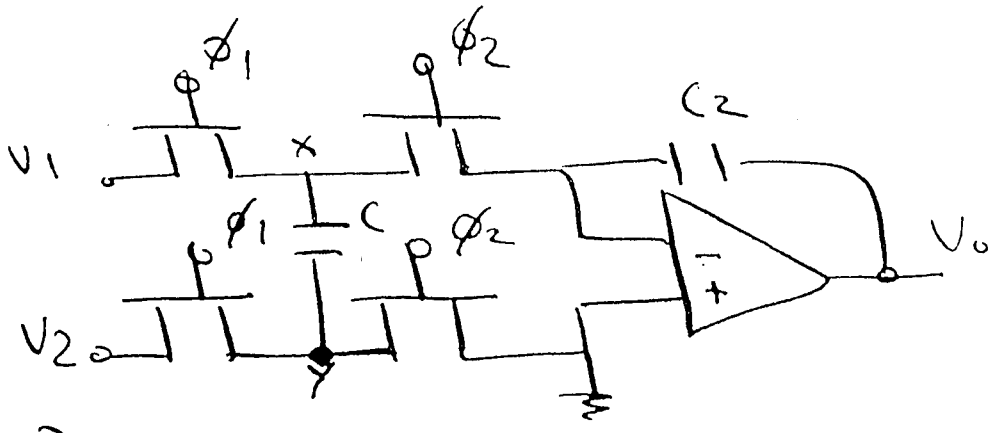
$$R_{eq} \times \left[\frac{1}{f_c \times C}\right] = 10M\Omega.$$

(3/3)

$\therefore$ for $C = 1pF \Rightarrow f_c = 100KHz$

(2/2)

Main advantage over passive resistor is huge reduction in chip area. Typically saving of (100 – 500) units^2 of chip area.



During ϕ_1

$$Q = C[V_1 - V_2]$$

$$I_{average} = f_c C_1 [V_1 - V_2]$$

ϕ_2 $\quad I_{av\,(q-cre)} = -f_c C_1 [V_1 - V_2]$

$$\therefore V_o = \left(\frac{-1}{j\omega C_2}\right) f_c C_1 [V_1 - V_2]$$

(5/5) $\dfrac{V_o}{(V_1 - V_2)} = \left[\dfrac{-f_c C_1}{j\omega C_2}\right] \Rightarrow$ differential integrator.

(2/2) Schemes in parasitic insensitive because Drain parasitics at nodes x and y are shorted out during both clock phases. All parasitics are driven by voltage source OR connected to ground / virtual ground potential.

SC filter example.

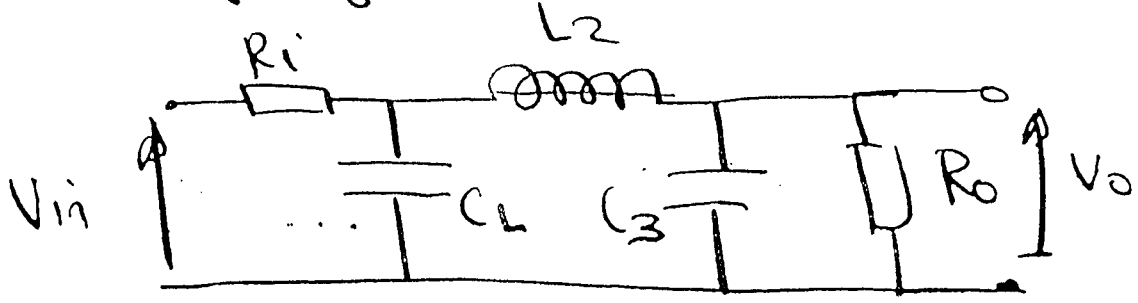
General transformation rules for Ladder prototypes

$$\frac{f_c L_2}{R_S} = \frac{C_{L2}}{C_u}, \qquad C_{c3}/C_u = f_c R_S C_3$$

↑ INDUCTOR $\qquad$ ↑ CAPACITOR

R_S = dummy scalar.

RLC prototype



For SC equivalent —

$C_{C1} = C_{C3} = 5.08\,pF$, $C_{L2} = 3.49\,pF$

$C_4 = 1\,pF$.

Assume scaling $R_S = R_i = R_o = 1\,\Omega$.

$$\therefore L_2 = \frac{C_{L2}}{f_c} = \frac{3.49}{100 \times 10^3} = 3.49 \times 10^{-5}\,H$$

Normalised rad/s $\Rightarrow \times 2\pi f_o$

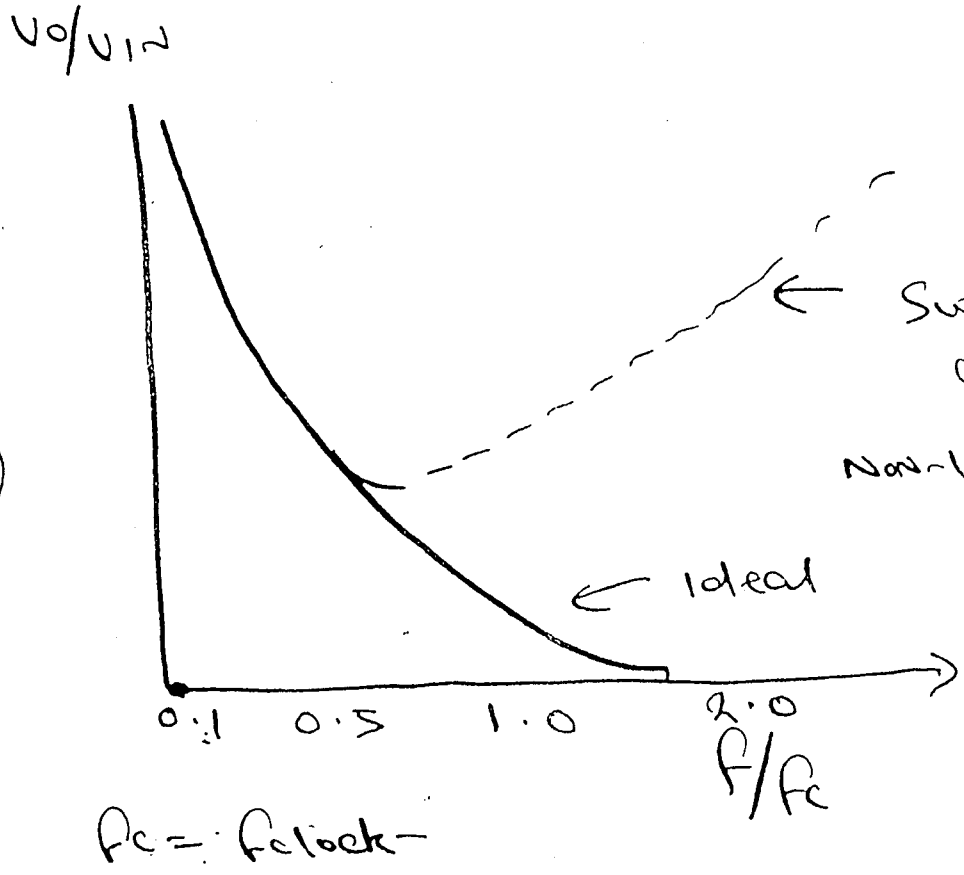
$= \times 2\pi \times 5\,kHz = \underline{1.096}$

$$C_1 = C_3 = \frac{C_{C3}}{f_c} = \frac{5.08}{100 \times 10^3} = 5.08 \times 10^{-5}\,F$$

Normalised $\times 2\pi f_o = \underline{1.596}$

8/8

$C_1 = C_3 = 1.596$, $L_2 = 1.096$



2/2

$f_c = f_{clock}$

Term 25/26

(4)

Single - stage

(1) Advantage : High speed
Good Phase Margin

(1) Disadvantage : low gain
low CMVR

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op-amp

(2) Voltage gain = $-g_{m2}/(g_{o2}+g_{o4})$

$(g_{o2}+g_{o4}) = I_{D2}(\lambda_N+\lambda_P) = 5\times10^{6}\times0.05 = 2.5\times10^{-7}$ S

(2) $g_{m2} = 2\sqrt{\beta_2 I_{D2}} \Rightarrow \beta_2 = \frac{k_N}{2}\left(\frac{W}{L}\right)_2 = 7.5\times10^{-5}$ A/V

$g_{m2} = 3.87\times10^{-5}$ S $\Rightarrow A_1 = -154.9$

$A_2 = -g_{m6}/(g_{o6}+g_{o7})$

$(g_{o6}+g_{o7}) = I_{D6}(\lambda_N+\lambda_P) = 20\times10^{-6}\times0.05 = 10\times10^{-7}$ S

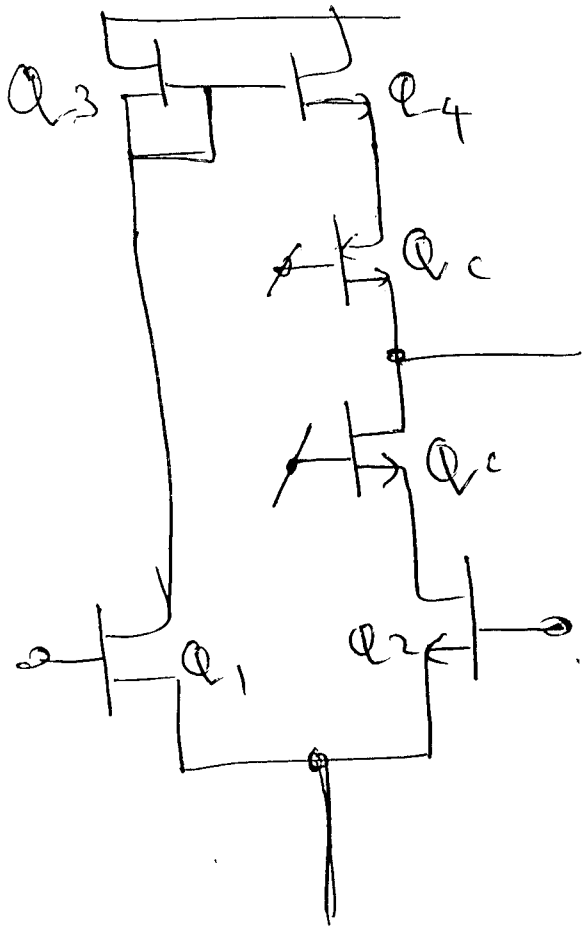
(2) $g_{m6} = 2\sqrt{\beta_6 I_{D6}} \Rightarrow \beta_6 = \frac{k_P}{2}\left(\frac{W}{L}\right)_6 = 1.6\times10^{-4}$ A/V

$g_{m6} = 1.13\times10^{-4} \Rightarrow A_2 = -113$

(4) $A_{TOTAL} = 17503$, $GB_P = \frac{g_{m2}}{2\pi C_C} = 41$ MHz

Increasing gain

2 ways (input)



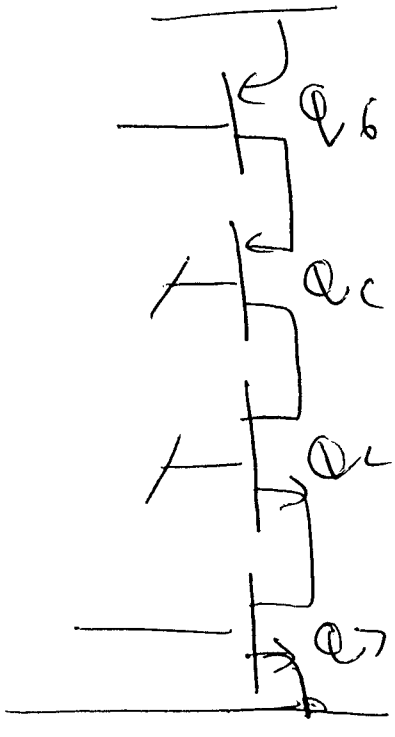
Cascoded input stage

Penalty

Common-mode voltage Range

Cascoding output stage

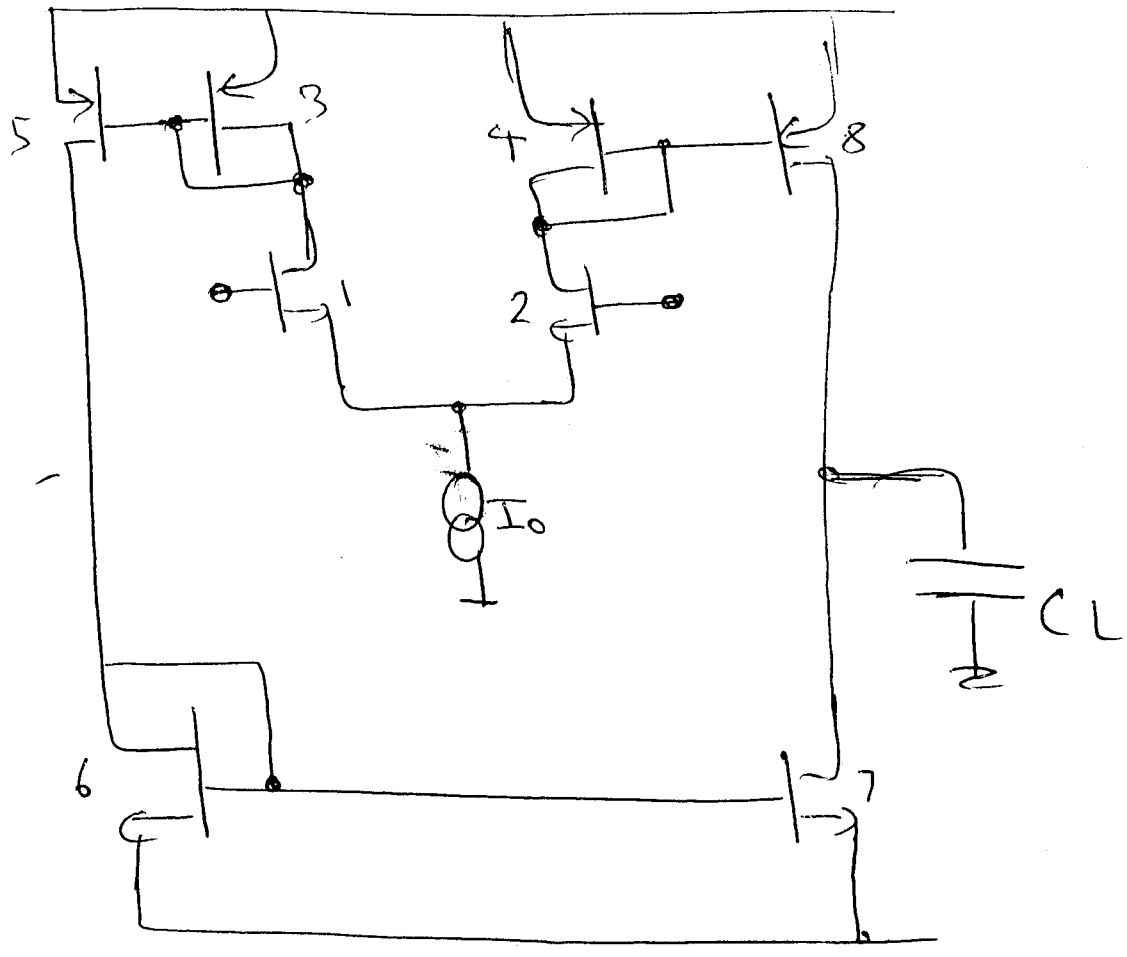
OUTPUT



Penalty

- Noise performance
- OUTPUT voltage swing.

Push-pull op-amp

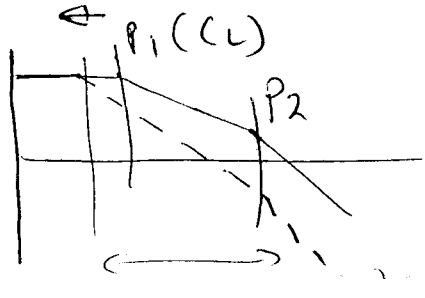


(5) 5

Another load capacitance sets dominant pole of op-amp. Non-dominant pole created at diode connected nodes.

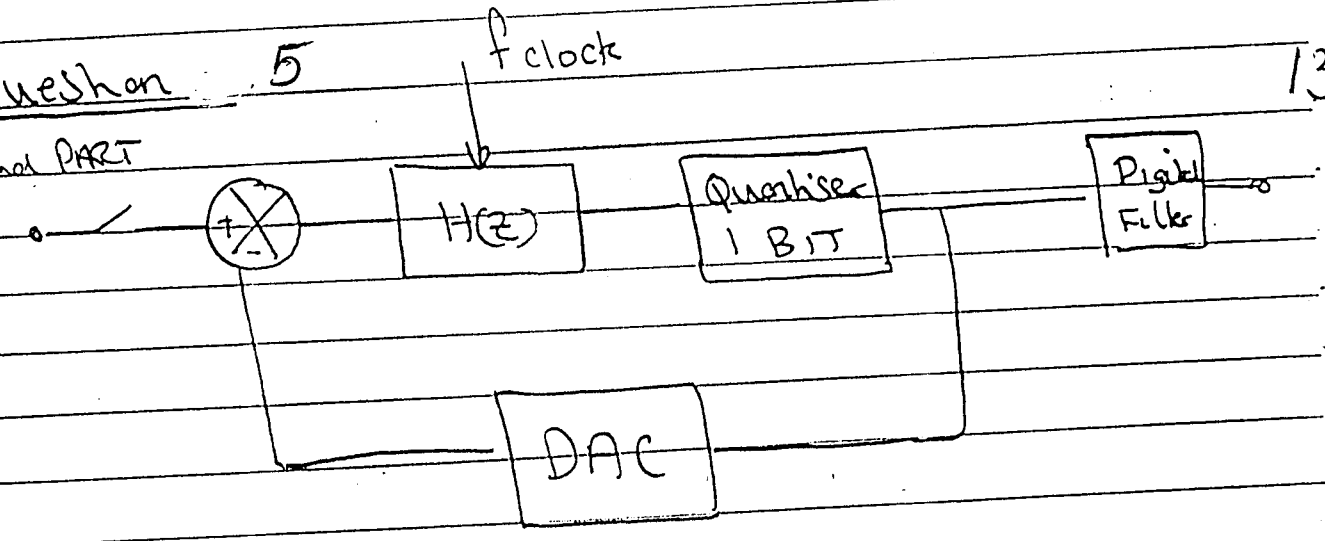
Hence as C_L is increased 3

(3) (P_1) is reduced in frequency and phase margin decreased.



Question 5

2nd PART

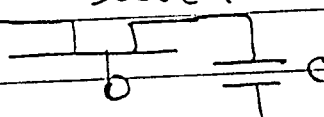


(8/8)

Basic idea is that coarse quantisation noise gets shaped by 1/H(z) via feedback. Generally H(z) is an integrator so noise is shaped differentially. This reduces requirements upon component accuracy. The architecture includes a negative feedback loop producing the coarse estimate that oscillates about the true value of input, the digital filter averages this coarse estimate to produce a fine approximation. The feedback DAC and forward integrator force the quantisation error to have a high frequency spectrum. The output of the digital filter is down sampled and gives a multibit digital representation. High frequency quantisation noise is reduced.

(10/10)

1.5 Part Dynamic Range Δ Vref / noise $= 2^N$



RMS noise of switch driving capacitor $= \sqrt{\frac{KT}{C}}$

$\therefore DR = \frac{Vref}{\sqrt{\frac{KT}{C}}} = 2^N$

(8/8)

Assume $f_c = \left(\frac{1}{10.RC}\right)$, then solving for C gives

$\therefore DR = 2^N = Vref / \sqrt{KT\ 10RF_c}$

Question 5. continued.

1st Part.

Contraints

(3) 1/ Low voltage - low dynamic Range
2/ Non-linear process technology - Distortion.

Q6 Assumption is that if ($V_{DS} \approx 0$) or ($V_{DS} << V_{GS} - V_T$) device acts in linear region. From

$$I_D = \frac{KW}{L}\left[(V_{GS}-V_T)V_{DS} - V_{DS}^2/2\right](1+\lambda V_{DS})$$

for $V_{DS} << (V_{GS}-V_T)$, then $\lambda V_{DS} << 1$

So $$I_D = \frac{KW}{L}(V_{GS}-V_T)V_{DS}$$

6/6 OR $$R_{AB} = V_{DS}/I_D = L/(KW(V_{SS}-V_T))$$

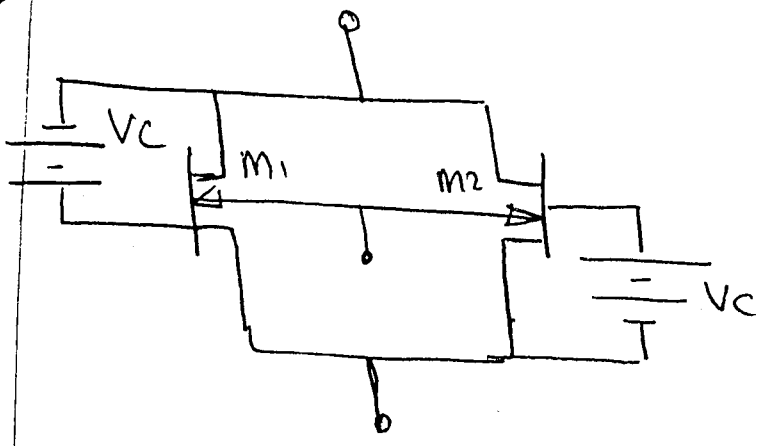
Three sources of Non-linearity

(i) limited due to V_{BS} changing V_T for resistive V_{DS} due to body effect.
ie $V_T = V_{TO} + \gamma\left[\sqrt{-V_{BS}+2\phi_F} - \sqrt{2\phi_F}\right]$
γ = bulk threshold parameter
ϕ_F = Fermi-level potential

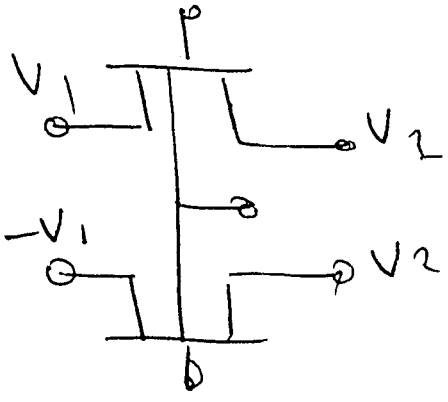
(ii) limited due to V_{DS} approaching $(V_{GS}-V_T)$ hence saturation region for large positive V_{DS}.

(iii) For large values of V_{DS} the $V_{DS}^2/2$ term comes in making the resistor quite non-linear.

4/4

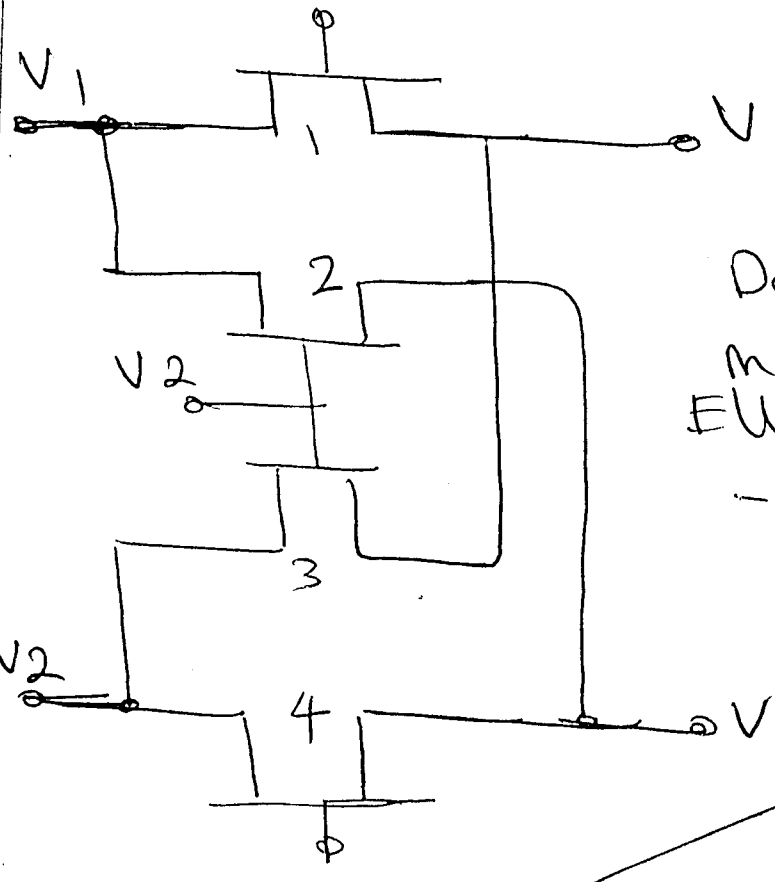


Parallel circuit – eliminates $V_{ds}^2/2$ term.



Differential scheme

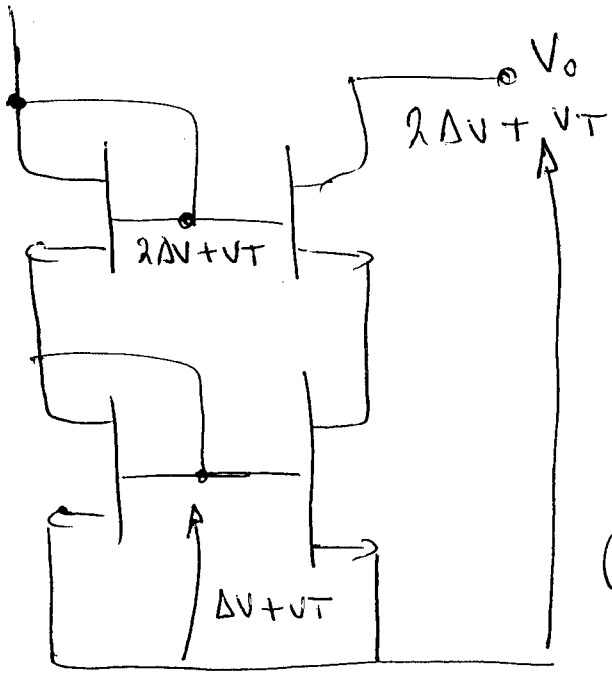
Effects of Vos cancelled.



Double differential nos.
Eliminates
– Vos and V_T term.

(2/2)

Any one of these will do!



Assume

$\Delta V = V_{GS} - V_T$

For Sat

$V_{DS} \geq V_{GS} - V_T$

$V_D = V_G - V_T$

$(V_o)_{min} = 2(\Delta V + V_T) - V_T$

$= \underline{2\Delta V + V_T}$

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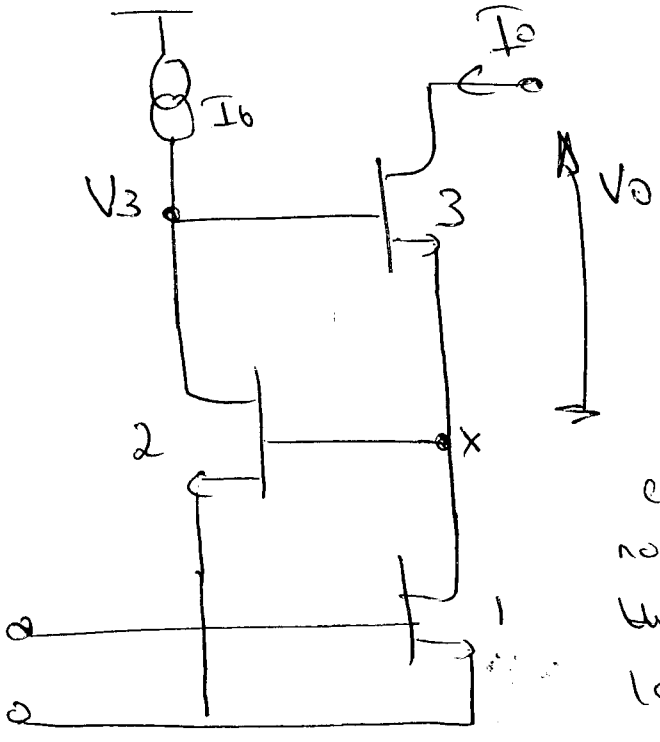

Transistor Q_3 Cascodes Q_1, hence output resistance due to Q_3 is $R_{O3} \geq r_{ds1}\, g_{m3} r_{ds3}$

Transistor Q_2 senses change in voltage at node (X) and reduces these changes by the loop gain of the amplifier (Q_2 and I_B)

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hence this feature increases the output resistance of the circuit to

$R_{out} = R_{O3}\, g_{m2} r_{ds2} \geq g_{m2} g_{m3} r_{ds1} r_{ds2} r_{ds3}$

assuming matched devices then

$R_{out} \geq g_m^2 r_{ds3}^2$ or (g_m^2 / g_{o3})

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