Paper Number(s): **E3.01**
AC1

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2001

MSc and EEE PART III/IV: M.Eng., B.Eng. and ACGI

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Tuesday, 1 May 10:00 am

There are SIX questions on this paper.

Answer FOUR questions.

Time allowed: 3:00 hours

Corrected LG Q3, Q4.

Examiners: Toumazou,C. and Papavassiliou,C.

Special instructions for invigilators: None

Information for candidates: None

1. *Figure 1* shows two bipolar integrated circuits.

For the bandgap voltage reference circuit of *Figure 1(a)*, show that $dV_o/dT = 0$ (where T is temperature) if $I_1 = I_2 \exp [29 R_3/R_2]$, and for this condition $V_o = 1.283$ V. Assume the temperature coefficient of V_{BE} to be -2.5 mV/°C, the collector current of transistor Q_3 is 100 μA and the device saturation current $I_s = 1.2 \times 10^{-13}$A. Boltzmanns Constant $k = 1.38 \times 10^{-23}$J/K and electron charge $q = 1.6 \times 10^{-19}$ C. [10]

For the circuit of *Figure 1(a)*, design a suitable current source I_B of value 300 μA, which is virtually independent of power supply voltage and directly proportional to absolute temperature. Sketch the circuit and ignore any automatic start-up circuitry. [7]

Figure 1(b) shows a high swing low voltage cascode current-mirror. Estimate the minimum output voltage swing V(min) which ensures that all devices remain in saturation. Given the following data, calculate V(min): $I_o = 100\mu A$, $K = 40\ \mu A/V^2$, and (W/L) = 1 for all devices. [8]

What is the new value of V(min) if (W/L) is increased to 10?

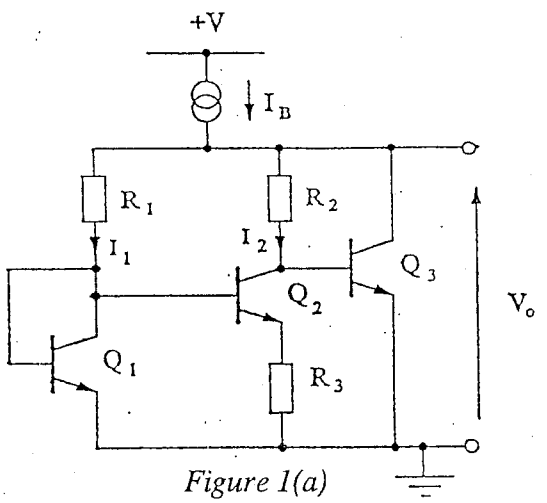

Figure 1(a)

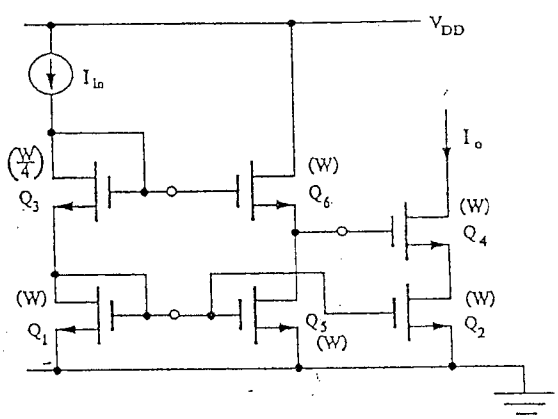

Figure 1(b)

2. Briefly explain the operation of each of the biassing circuits in *Figure 2.* [10]

For the circuits of *Figure 2(a)* and *Figure 2(b)* calculate a value for resistor R to yield an output current I_0 of 10 μA and use this example to show that the circuit of *Figure 2(b)* has a lower fractional temperature coefficient. You may assume that the circuits are operating at room temperature. The forward saturation current of the transistor $I_S = 10^{-14}$ A, the temperature coefficient of V_{BE} = -2 mV/°C and R is a polysilicon resistor with a temperature coefficient of 1500 ppm/°C. [6]

It is likely that on power-up the output currents of *Figure 2(a)* and *Figure 2(b)* will fall into a zero current state. Sketch a suitable start-up circuit for one of these two circuits to ensure this condition will not occur. [3]

Finally, using reasonable engineering approximations, give an expression for the output resistance of the circuit of *Figure 2(c).* You only need consider trsnsistors Q1, Q2, Q3 and Q7 since the remaining transistors are purely for biassing purposes. [6]

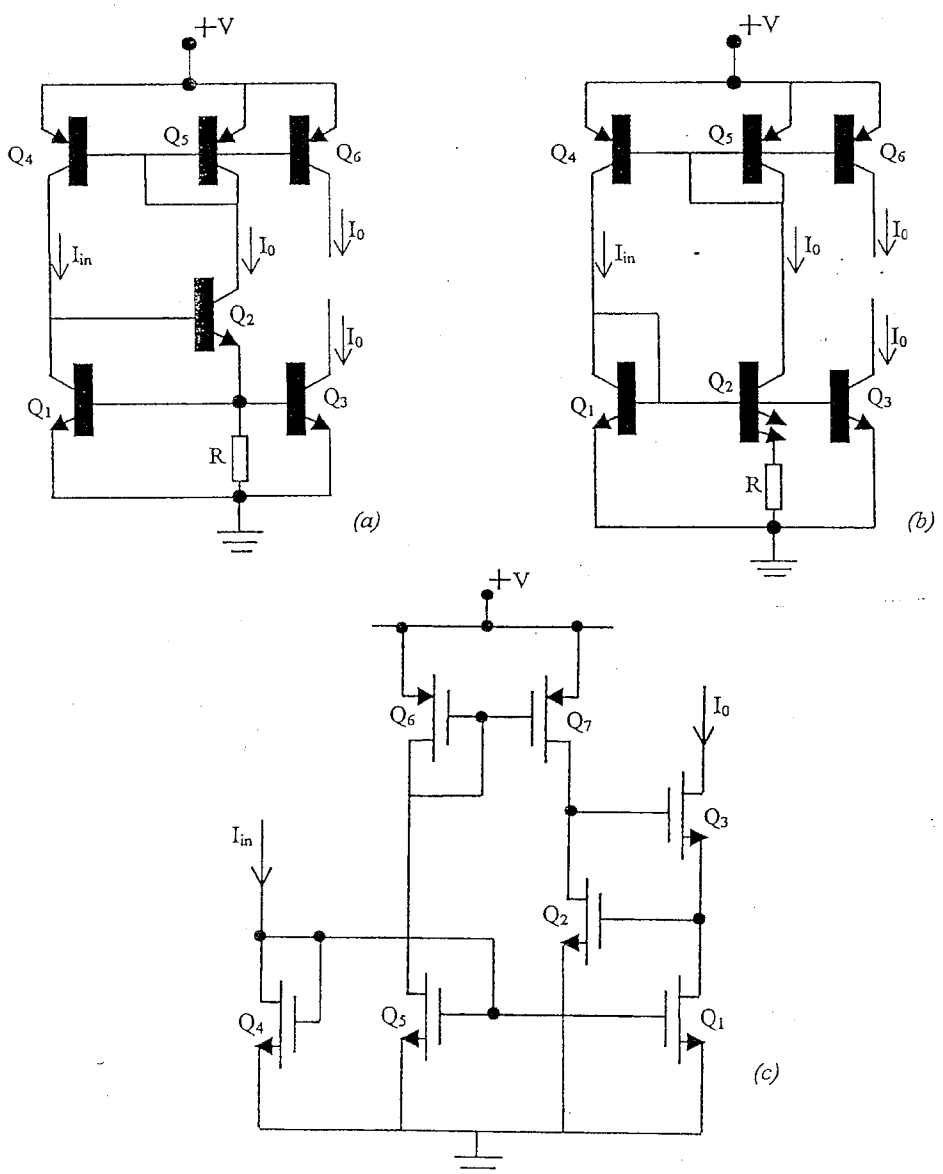

Figure 2

3. *Figure 3* shows a partially-designed two-stage CMOS op-amp required to give a voltage gain of approximately 80 dB, a slew-rate of 5 V/μs and a gain-bandwidth product of 3 MHz. Given that the technology is a fixed 5 μm length double metal CMOS process, design the channel widths of transistors Q1, Q2 and Q6 for the op-amp to meet the above performance specifications. Aspect ratios of all other devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below. [16]

After simulation you find that the phase margin of your op-amp is below specification. *Qualitatively*, discuss a sequence of parameter changes that would lead to improvement in phase margin; you are willing to sacrifice amplifier gain-bandwidth product. [5]

Finally, give a reason why the introduction of a single integrated resistor in series with the compensation capacitor should significantly improve the amplifier's phase margin. [4]

CMOS TRANSISTOR MODEL PARAMETERS

MODEL PARAMETERS	K_P (μA/V^2)	λ (V^{-1})	V_{To} (V)
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

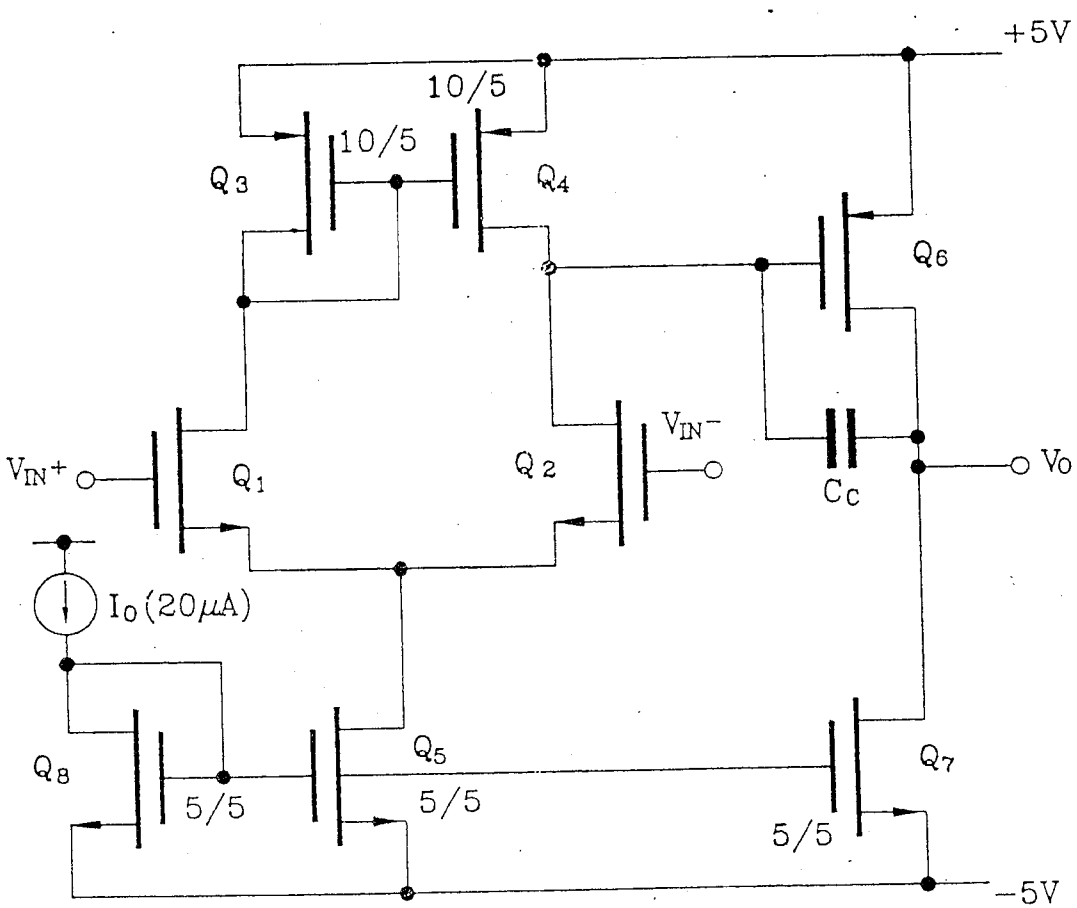

Figure 3

4. Using two switches and a capacitor, sketch a circuit that will synthesise an active resistor. Given that the switches are driven by a pair of non-overlapping clocks running at a frequency of 100 kHz, estimate the value of a capacitor to give a resistance of 10 MΩ. [8]

A fundamental limitation imposed on the Dynamic Range (DR) of any high performance A/D converter will ultimately be switch noise. Prove that the fundamental limit is given by,

$$DR = \frac{V_{ref}}{\sqrt{(10kTRf_c)}} \qquad [7]$$

10.47

where V_{ref} is the reference voltage, k is Boltzmann's constant, T is absolute temperature, R is switch resistance and f_C is the maximum clock frequency of the switch. You may assume that the system settles in 10t (where t = time constant), over one period of the clock frequency.

Finally, *Figure 4* shows one section of a switched capacitor ladder filter. Based on this filter structure, design a 3rd-order Chebyshev low-pass filter with a cut-off frequency of 5 kHz and a 1.0 dB pass band ripple. Assume a clock frequency of 100 kHz. Passive component values for the LC prototype, normalised to 1 rad/s, are $C_1 = C_3 = 2.0236$, $L_2 = 0.994$. In your analysis assume all integrators to be lossless. [10]

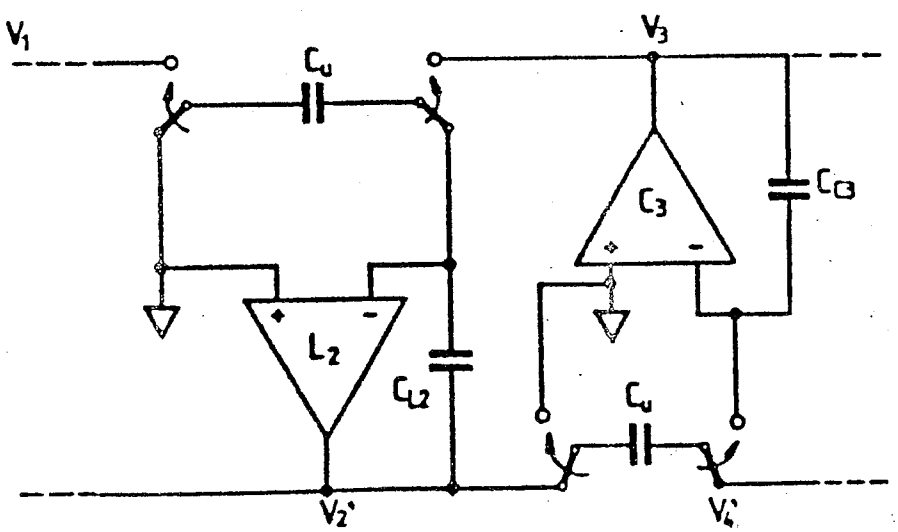

Figure 4

5. Classical CMOS operational amplifiers (op-amps) are either single-stage or two-stage designs. Based on the two stage design of *Figure 3* sketch a typical architecture for a two-stage cascoded output op-amp and a single-stage fully differential folded cascode op-amp. Briefly describe the operation of each of these op-amps and give one peformance advantage and disadvantage of each compared to the basic op-amp architecture of *Figure 3*. Ignore common-mode feedback circuitry in the folded cascode op-amp. [18]

Finally, what is the function of the circuit of *Fig. 5(a)* ? [7]

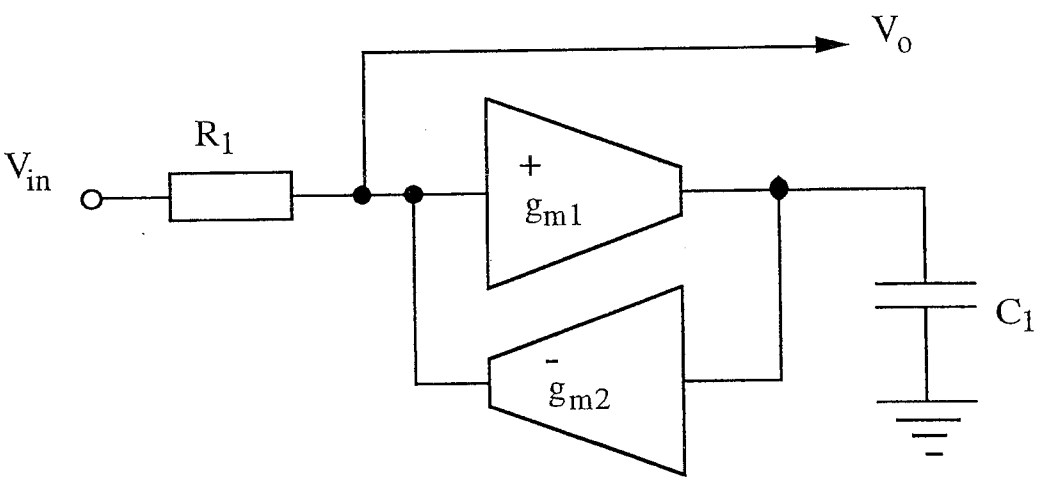

Figure 5(a)

6. In mixed-mode ASIC design, process technology is being optimised for digital performance specifications. Give one example of the constraints this places upon analogue circuit design performance.
Two high-performance analogue-to-digital converters are the current-mode algorithmic converter and the sigma-delta converter. Sketch a typical architecture for one of these converter types and explain its principles of operation. [18]

When prototyping high frequency amplifiers, why is a good ground plane important? [4]

Why is a x10 scope probe used for measuring high frequency signals on the oscilloscope ? [3]

ANALOGUE INTEGRATED CIRCUITS & SYSTEMS

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Q1 For the bandgap voltage reference

$V_{BE1} = V_{BR2} + I_2 R_3 \quad (\beta >> 1)$

Since $V_{BE1} - V_{BE2} = V_T \ln (I_1/I_2)$

Then $V_o = V_{BE3} + (R_2/R_3) V_T \ln (I_1/I_2)$

For $dV_o/dt = 0$ → assumes V_{be} has -ve temp coefficient

then $dV_{BR3}/dT = V_T/T (R_2/R_3) \ln (I_1/I_2)$

Since $dV_{BE3}/dT = -2.5 mV/°C$

and $\frac{V_T}{T} = k/q = 1.38 \times 10^{-23} / 1.6 \times 10^{-19}$

$= 8.625 \times 10^{-5}$

$\therefore (R_2/R_3) \ln (I_1/I_2) = 28.98 \simeq 29$ — [5]

rearranged gives

$$I_1 = I_2 \exp [29 R_3/R_2]$$

To calculate V_o → require V_{BE} of Q3

and $V_T = 300 \times 8.625 \times 10^{-5} = 25.9 mV$

$$V_{BE} = V_T \ln \left[\frac{I_{C3}}{I_S}\right] = 25.9 \times 10^{-3} \ln \left[\frac{100 \times 10^{-6}}{1.2 \times 10^{-13}}\right]$$

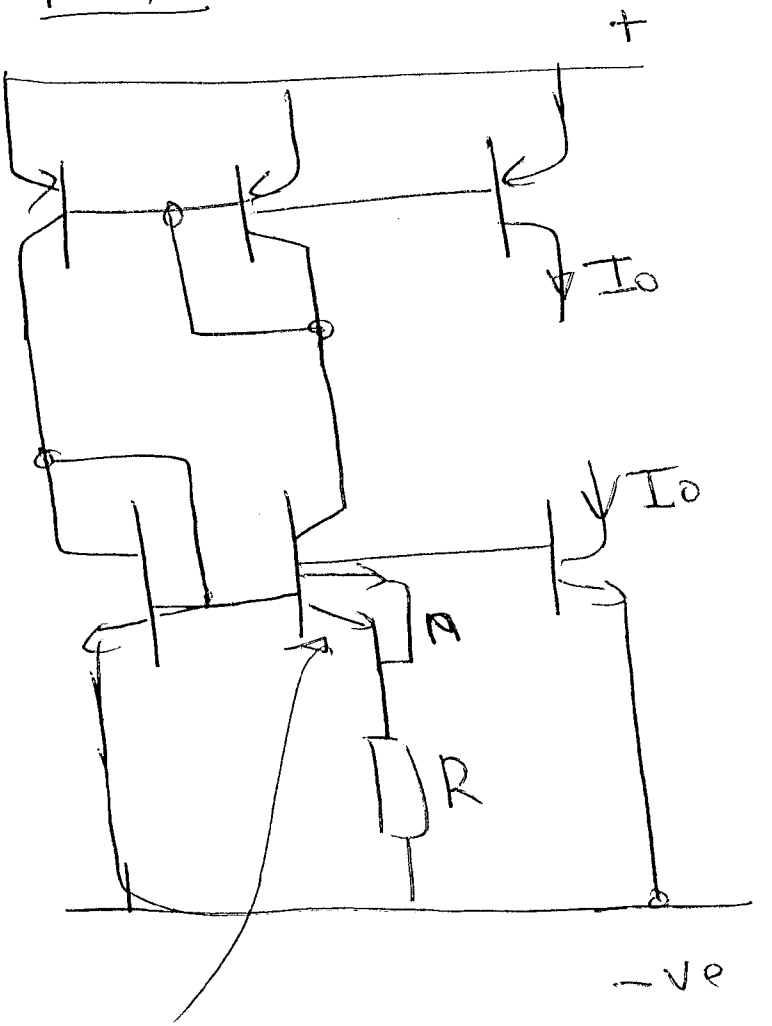
$= 0.532$

$\therefore V_o = 0.532 + [28.98](25.9 \times 10^{-3})$

$\simeq \underline{1.283 \text{ volts}}$ — [5]

Q1 Cont

PTAT



[7]

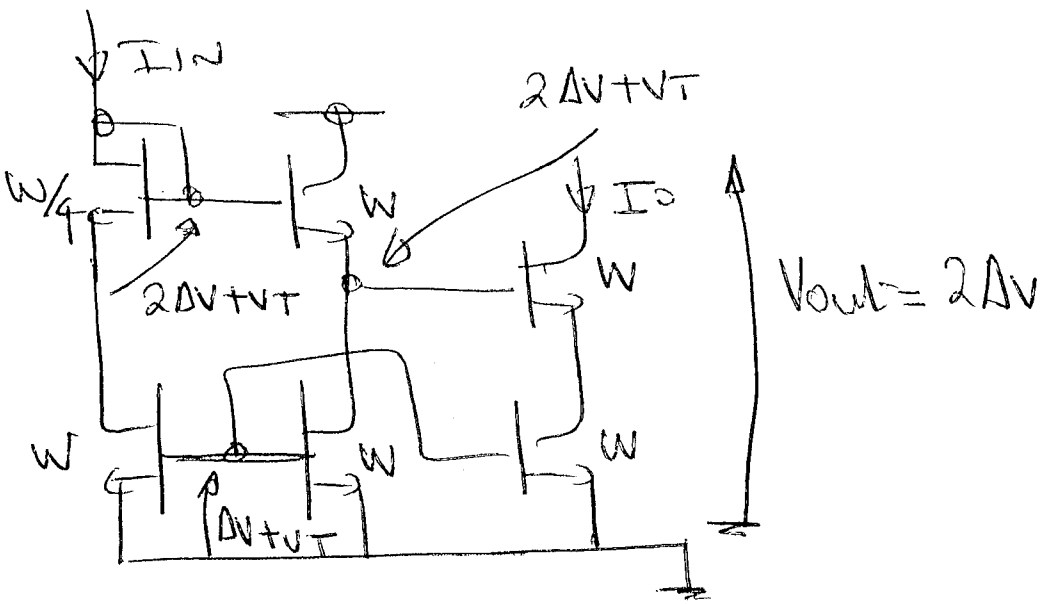
n-emitter - self biasing scheme requires start-up circuit.

$I_O = V_T \ln [n/R] = 300\mu A$

for $n = 2$

$\therefore R = 60\Omega$.

Q1 cont



Assume equal L_s

$I_O = I_{IN}$, $\beta_1 = \beta_2 = \beta_4 = \beta_5 = \beta_6 = \beta$

$\beta_3 = \beta/4$

$V_{sat3} = 2(V_{GS} - V_T)$

where $\Delta V = (V_{GS} - V_T)$

since $I_O = \beta(V_{GS} - V_T)^2$.

then $(V_{GS} - V_T) = \sqrt{I_O/\beta} = \sqrt{\frac{100\times10^{-6}}{40\times10^{-6}/2}}$

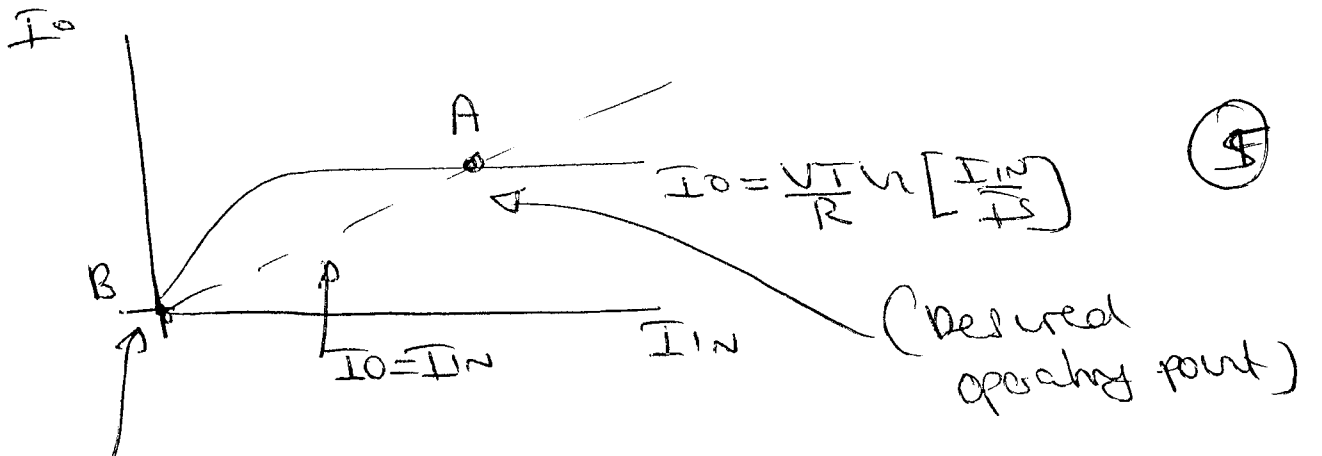
$\Delta V = 1.414V$

[8]

TOTAL 25/25.

Q2

Fig 2a is a self biased Vbe referenced current source and sink. Output current is virtually power supply independent since $I_O = V_{be1}/R = V_{be2}/R = \frac{V_T \ln(I_{IN}/I_{S1})}{R}$. Since I_{IN} appears in the log and I_O sets I_{IN} then I_O is almost insensitive to power supply. However 2 stable states exist. I_O & $\ln(I_{IN})$ and $I_O = I_{IN}$.



Circuit requires start-up to avoid zero current state B does not occur.

Figure 2(b), has the same function of supply independent biasing as Figure 2(a) and is known as a PTAT (proportional to Absolute Temp) constant current-source / sink. The output current is now given by the difference between V_{be1} and V_{be2}, i.e. $I_O = \frac{V_{be1} - V_{be2}}{R}$

$$= \frac{V_T}{R} \ln\left[\frac{I_{IN}}{I_O} \times \frac{I_{S2}}{I_{S1}}\right]$$

Qu 2 (cont

Since Q2 has twice the emitter area of Q1 then $I_{S2} = 2I_{S1}$, $I_O = \frac{V_T}{R} \ln 2$

$I_O = I_{IN}$ from current-mirror Q4, Q5.

Some disadvantage as figure 2(a), requires automatic start-up circuit.

Note output current now much less dependent upon I_{IN}. Also PTAT results in lower temperature coefficient than V_{BE} reference source because of positive temperature coefficient of V_T.

Fig 2(a) $\Rightarrow V_{be1} = V_T \ln\left[\frac{10\times10^{-6}}{10^{-14}}\right] = 0.539V$

Since $I_O = V_{be}/R \Rightarrow R = 53.9k\Omega$

$$Tcf = \frac{1}{V_{be1}}\frac{\partial V_{be1}}{\partial T} - \gamma_R \partial R/\partial T$$

$$= \frac{1}{0.539} \times (-2mV) - 1500\times10^{-6} = -0.52\%/^\circ C$$

$$= \text{OR} \quad -5200 ppm/^\circ C \qquad (3)$$

Fig 2 b $I_O = \frac{V_T \ln 2}{R} \Rightarrow R = 1.8k\Omega$

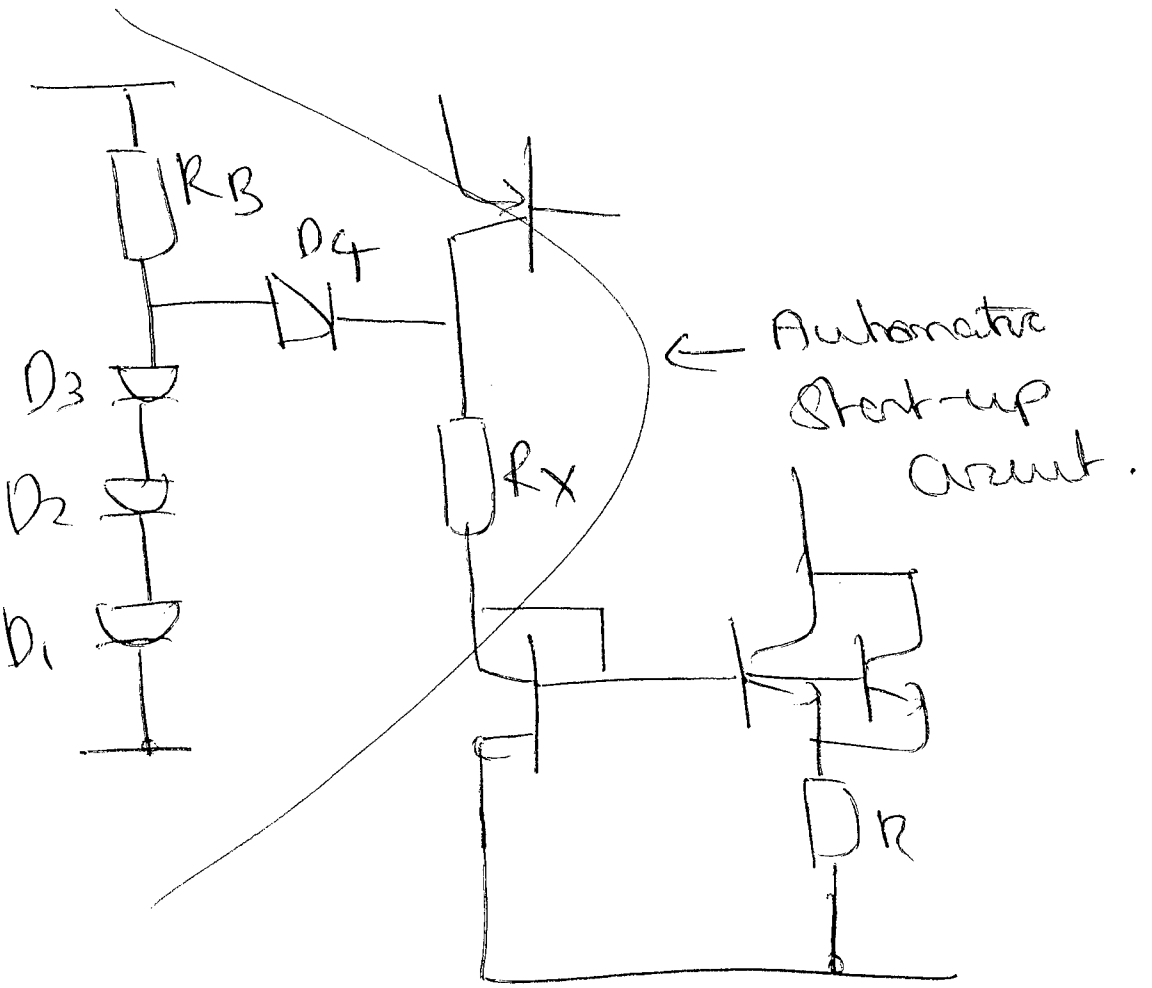
$$Tcf = \frac{1}{V_T}\frac{\partial V_T}{\partial T} - 1/R\, \partial R/\partial T$$

$$= \gamma_T - 1/R\, dR/\partial T = \frac{1}{300} - 1500\times10^{-6} = 0.18\%/^\circ C$$

OR 1833 ppm/°C $\Rightarrow$ lower

5 of 17 (3)

Q2 cont



(3)

last part Fig 2c

Transistor Q3 cascodes Q1

thus $r_{O3} = r_{ds1}\, g_{m3} r_{ds3}$

Q2 provides negative feedback which reduces the output resistance of circuit to $r_{out} = g_{m2}(r_{ds2} // r_{ds7}) \times g_{m3} r_{ds3}$

assuming equal g_m and r_{ds}

then $r_{out} = g_m^2 \frac{r_{ds}^2}{2}$

(6)

Turn 25/23

Question 3

Specs $A = 80\,dB$, $SR = 5\,V/\mu S$, $G\cdot B = 3\,MHz$.

$A_1 = g_{m2}/(g_{o2}+g_{o4})$

$(g_{o2}+g_{o4}) = I_{D2}[\lambda_N+\lambda_P] = 10\times10^{-6}[0.05]$
$= 5\times10^{-7}\ \Omega^{-1}$

$g_{m_2} = \sqrt{\beta_2 I_{D2}} \Rightarrow$ but $G\cdot B = g_{m2}/2\pi C_c$

Hence to calculate g_{m2} require C_c. Since
$S.R = I_o/C_c$ then $C_c = 4pF \Rightarrow g_{m2} = 7.54\times10^{-5}\ A/V$
$\therefore A_1 = 150.8$ From $g_{m2} \Rightarrow \beta_2 = 1.42\times10^{-4} = \left(\frac{kW}{2L}\right)$
$\therefore (W/L)_2 = 9.47$ OR $\approx (47/5)$
$(W/L)_1 = (W/L)_2 = 47/5$. (8)

Since $A_1 = 150.8$, $A_2 = (3981/80) \simeq 66.3$
Now $A_2 = g_{m6}/(g_{o7}+g_{o6})$
$(g_{o7}+g_{o6}) = I_{D7}(\lambda_N+\lambda_P) = 20\times10^{-6}(0.05)$
$= 1\times10^{-6}\ \Omega^{-1}$
$g_{m6} = 6.63\times10^{-5} \Rightarrow \beta_6 = \left(\frac{g_{m6}}{2}\right)^2 \frac{1}{I_{D6}} = 5.5\times10^{-5}$

$\therefore (W/L)_6 = \frac{2\beta_6}{k} = 5.5$ OR $(2705/5)$ (8)

Failed Phase Margin

Possible sequences.

- (1) Increase C_c [reduce G.B and SR]
- (2) Increase I_o to increase S.R. [traded A_1]
- (3) Increase (W_2) hence g_{m2} to increase A_2.

(5)

- Reduce $W_1 = W_2$
- increase W_6

2-step solution

(1) Reduce $W_1 = W_2$ [reduces g_{m2} hence G.B and A_1]
(2) Reduce I_o [increased A_1, but reduced S.R]
(3) Can afford to increase G.B, increase C_c to increase S.R. [Further reduced G.B].

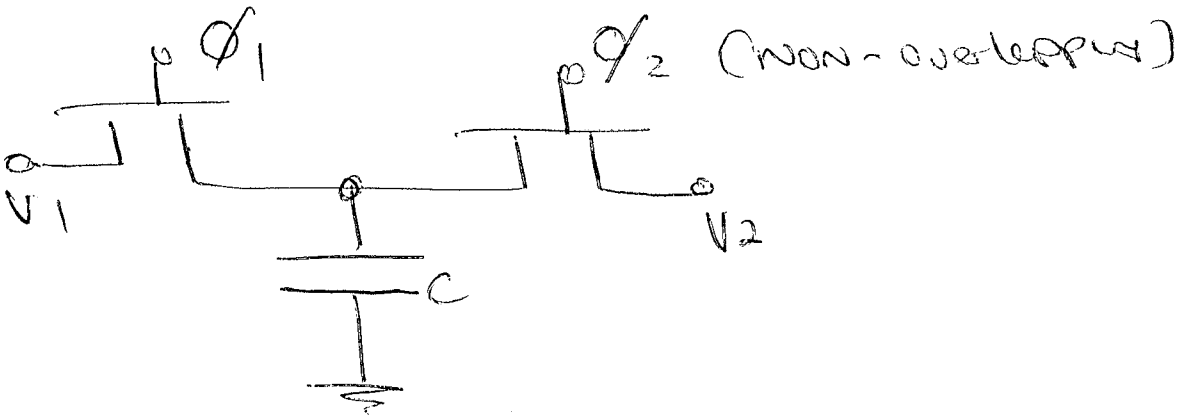
for IT

PTO

Introduction of a series R with C introduces a tunable R.H.P zero which can either be adjusted ($1/g_{m6}$) w.r.t a L.H.P zero added phase lead compensation or used to cancel the amplifiers non-dominant pole.

(24)

Qu 4



Excess charge $\Delta Q = C[V_1 - V_2]$

$$I_{av} = \frac{\Delta Q}{T} = \frac{C[V_1 - V_2]}{T}$$

$$R_{eq} = \frac{(V_1 - V_2)}{I_{av}} = T/C$$

5/3

Assuming $f_{clock} \gg f_{signal}$

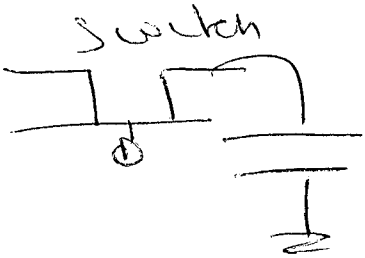
then $R_{eq} \approx \frac{1}{f_c C} \approx 10M\Omega$

$f_c = 100kHz$, $C = 1pF$

3/3

$DR = V_{refl}/Noise = 2^N$

switch



Noise $\sqrt{\frac{KT}{C}}$

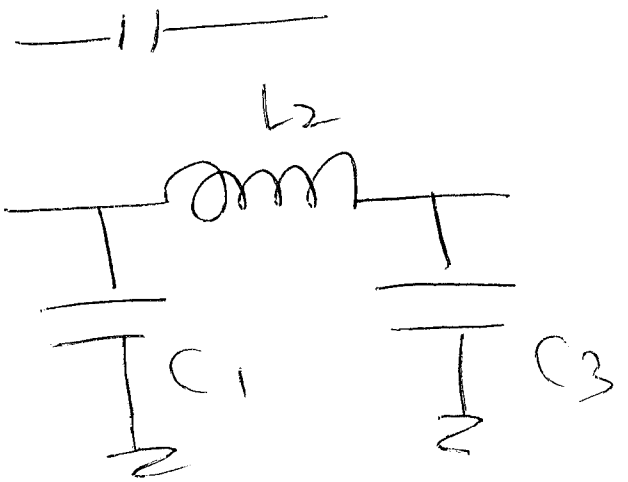
3/3

Q4 cont

Assume $f_c = \frac{1}{10 \cdot R \cdot C}$ (2/2)

Then Solving for C gives

$$DR = 2^N = V_{reff} \sqrt{\frac{}{KT\,10Rf_c}}$$ (2/2)



Solution for LCR prototype.

Inductive transformation $(L_2/R_s)f_s$ (3/3)

$= C_{L2}/C_u$

Capacitive transformation $= C_{C3}/C_u = f_c R_s C_3$ (3/3)

Where R_s is normalized during scaling resistor.

Assuming $R_s = 1$.

$C_{C1}/C_u = f_c C_1$
$C_{C3}/C_u = f_c C_3$
$C_{L2}/C_u = f_c L_2$

} general transformation.

Qu 4 cont

Table values of C_1, L_2 and C_3 are normalized to $1 \text{ rad/s} \div 2\pi f_p$ ($f_p = 5\text{kHz}$)

$C_1 = C_3 = 2.0236 / (2\pi 5 \times 10^3) = 6.44 \times 10^{-5} F$

$L_2 = 0.994 / (2\pi 5 \times 10^3) = 3.164 \times 10^{-5} F$

For termination resistors (ie load in input and output matching.) 1/2

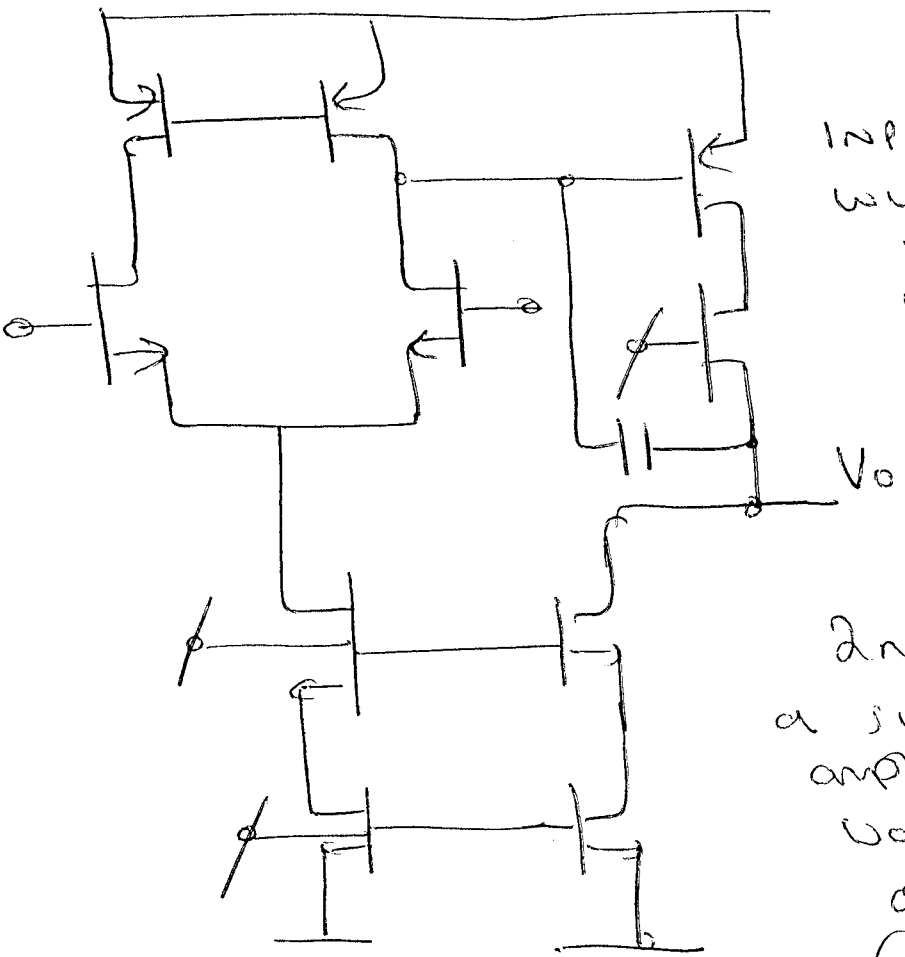
assume $C_u = C_{R_i} = C_{R_o} = 1pF$

then $C_{C_1} = C_{C_3} = \underline{6.44pF}$

$C_{L_2} = \underline{3.164 pF}$. 2/2

TOTAL 25/25

Qu 5



INPUT – Diff pair with CM active load provides voltage gain of the order of $g_m/2g_o$. Diff to single ended conversion

2nd gain stage is a single cascode amplifier with a voltage gain of the order of $(g_m/g_o)^2 1/2$.

Main advantage

- Increase in overall voltage gain. [5]

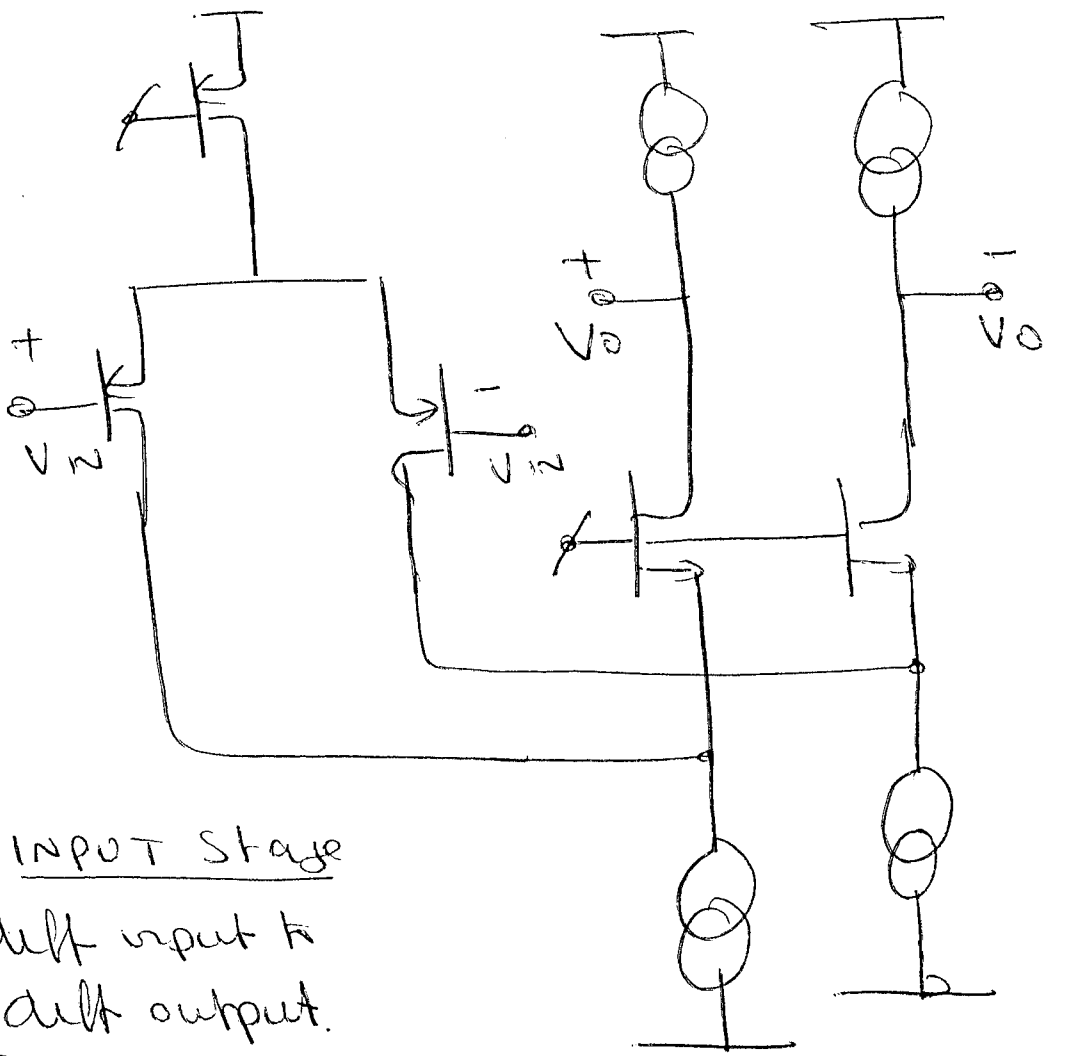
Disadvantages

- Phase margin reduced due to reduction in output pole frequency
- Output voltage swing reduced due to cascode
- Higher noise due to lower gain at input stage.

[4]

Q4 S cont

Folded cascode amplifier.



INPUT Stage

diff input &
diff output.

Single path folded & output

Gain of the order of $gm^2/2go^2$ [5]

Main disadvantage

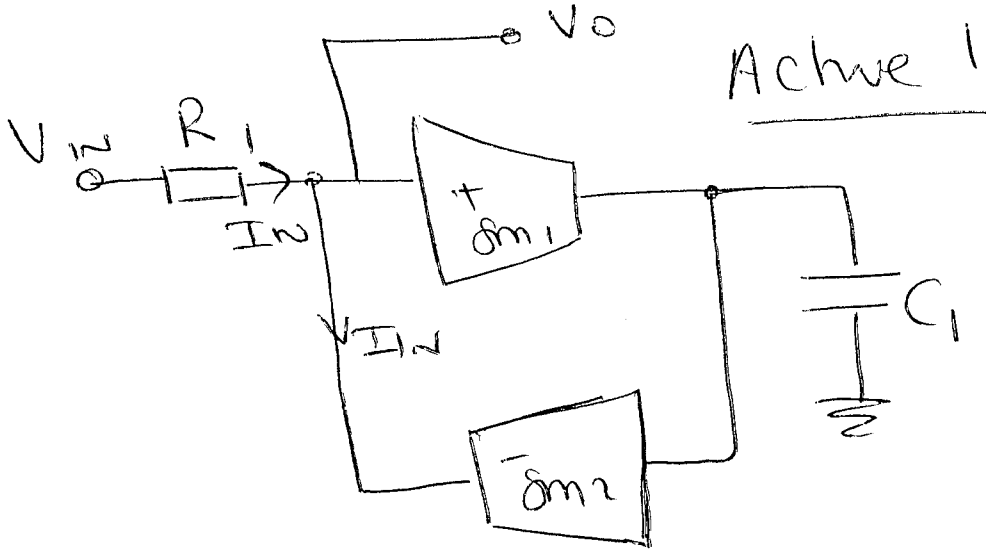
Output swing limited

Main advantages [4]

- Single high impedance at node of output (high speed)
- Good PSRR performance
- High CMVR
- Low noise – wideband
- Fully differential

Q5 cont

Active Inductor



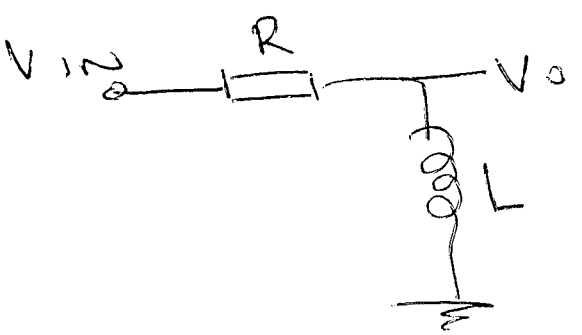
$$I_{IN} = g_{m2} V_o$$

$$V_o = \frac{g_{m1} V_{IN}}{sC}$$

$$\therefore I_{IN} = \frac{g_{m1} g_{m2} V_{IN}}{sC}$$

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{sC}{g_{m1} g_{m2}} \qquad [5]$$

$$Z_{IN} = sL = sC/g_{m1} g_{m2} \Rightarrow L = \frac{C}{g_{m1} g_{m2}}$$



1st Low pass filter of

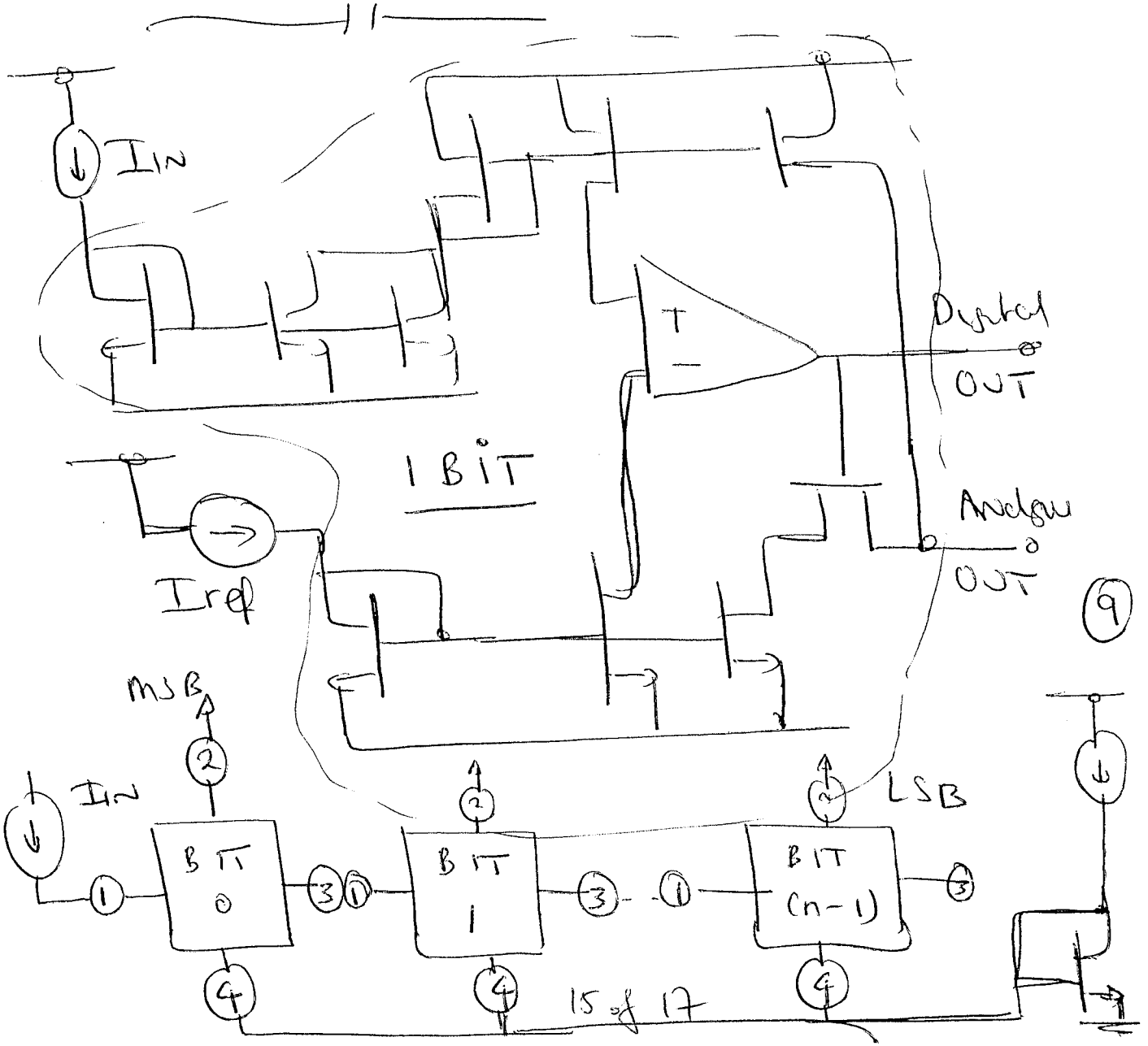
$$f = \frac{1}{2\pi R \left[\frac{g_{m1} g_{m2}}{C}\right]}$$

[2]

TOTAL 25/25

Qu 6/.

Examples :- Feature sizes will constantly shrink while threshold voltage will be lowered limiting performance of analog switches (ii) Logic gate leakage will prevent ophmum switched-capacitor circuit performance (iii) As power supply voltages reduce, dynamic range of analog parts will be limited (4)



(9)

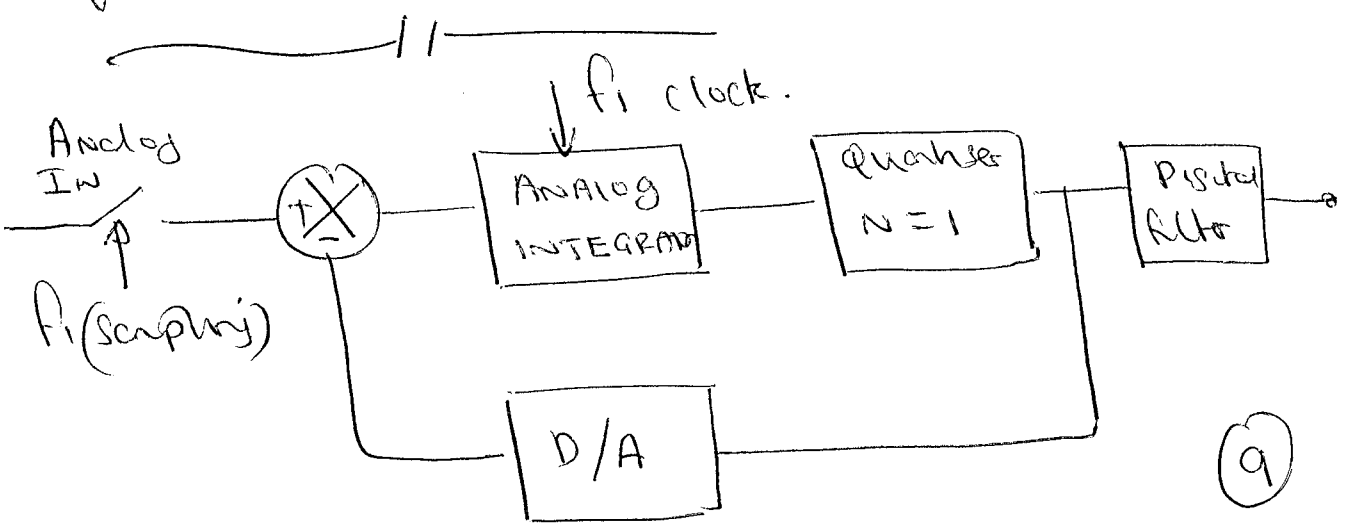
Qu 6 cont

Basic Architecture

Operation

$2I_{IN}$ on +ve terminal of comparator compares with I_{ref} (-ve) terminal. If $2I_{IN} < I_{ref}$, comp output goes low, digital output = 0 and Analogue output $2I_{IN}$. If $2I_{IN} > I_{ref}$, Comp output goes high, digital output = 1, and analogue out $2I_{IN} - I_{ref}$.

Analogue output continuously feeds into following bit 'cell' which performs exactly the same function. The process is continued as many times as possible to achieve the required resolution. (4)



(9)

Qu 6/ cont

In the $\Sigma\Delta$ modulator, coarse quantization at high sampling rate is combined with -ve feedback and digital filtering to achieve increased resolution at low sampling rates. This reduces requirements upon component accuracy. The architecture includes a negative feedback loop producing a coarse estimate that oscillates about the true value of input, the digital filter averages this coarse estimate to produce a linear approximation. The feedback A/D and integrator force the quantization error to have a frequency & frequency spectrum. The output of the digital filter is down sampled and gives a multibit digital representation. All high frequency quantization noise is simply reduced.

(9)