UNIVERSITY OF LONDON
IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2003

BEng Honours Degree in Computing Part II
MEng Honours Degrees in Computing Part II
BEng Honours Degree in Information Systems Engineering Part II
MEng Honours Degree in Information Systems Engineering Part II
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER C210=I2.3

ARCHITECTURE II

Thursday 15 May 2003, 14:30
Duration: 120 minutes

Answer THREE questions

Corrected Copy

Paper contains 4 questions
Calculators required

1 The MIPS processor has 32 general-purpose registers. Each MIPS instruction is 4 bytes in length. The opcode occupies 6 bits for all instructions. R-type instructions have two source register fields, one destination register field, one shift-amount field, and one 6-bit function code field; I-type instructions have one source register field, one destination register field and one data field; and J-type instructions have one jump address field.

a Label each field and the corresponding bit length for an R-type instruction. Repeat this step for an I-type instruction and a J-type instruction.

b The MIPS Plus processor has 64 general-purpose registers instead of 32. Each MIPS Plus instruction is 4 bytes long, and it follows the same opcode and function code as those in the MIPS processor. However, the number of bits for other fields can be different from those of the MIPS processor. Explain how this change will affect the R-type, I-type and J-type instructions. For each type of instruction, label each field and the corresponding bit length as in Part a.

c The MIPS Minus processor has 16 general-purpose registers. Each MIPS Minus instruction is 28 bits long, and it follows the same opcode and function code as those in the MIPS processor, although the number of bits for other fields can be different from those of the MIPS processor. For each of the R-type, I-type and J-type instructions, label each field and the corresponding bit length as in Part a. State two advantages and one disadvantage of the MIPS Minus processor, comparing it against the MIPS processor.

The three parts carry, respectively, 15%, 40%, and 45% of the marks.

2 This question concerns the following machines, each with a different architecture:

M1 has a load-store architecture, with n general-purpose registers ($n > 2$),

M2 has an accumulator architecture,

M3 has a stack architecture,

M4 has a memory-memory architecture.

a Given that variables P, Q and R are in main memory, provide an instruction sequence implementing the statement R=P+Q for each of the above four machines.

b i) Given that variables P, Q and R are in main memory, provide an instruction sequence for each of the above four machines implementing the statements

$$\begin{aligned} P &= P-R \\ R &= P+Q \end{aligned}$$

ii) Given that the four machines have the same opcode size of α bytes, the same memory address size of β bytes, and all data operands are of γ bytes, where α, β and γ are integers. All instructions are an integral number of bytes in length, and there are 32 registers in M1. There are no optimisations to reduce memory traffic, and all variables are placed initially in memory. For the instruction code sequences in i), calculate the code size and the data size for each of the four machines.

The two parts carry, respectively, 20% and 80% of the marks.

3 Consider a simple 4-bit Arithmetic Logic Unit (ALU) which can perform increment and bit-wise Boolean NOT operation for numbers in two's complement representation.

a Describe the function of a halfadder, and show how a 4-bit incrementer can be built using halfadders.

b Draw:

i) a circuit diagram showing the internal structure of a component ALUB which can be replicated 4 times to form the ALU. Do not show the internal structure of multiplexors and halfadders;

ii) a circuit diagram showing how the ALU can be built from 4 copies of ALUB. Label the signal values on all the wires in the diagram when the ALU processes the number 0011 (3 in base ten).

c A 4-bit circuit ABS is required for computing the absolute value of a number in two's complement representation.

i) Design a circuit A, containing only an exclusive-or gate and a halfadder, which can be replicated to form ABS.

ii) Show how ABS can be built from 4 copies of A. Label the signal values on all the wires in your circuit for the input 1111.

d The ALU in Part b will be extended to produce the absolute value of its input. The extended ALU contains 4 copies of the component ALUBA.

i) Show how the circuit ALUB in Part b and the circuit A in Part c can be combined to form ALUBA.

ii) Show how the extended ALU can be built from 4 copies of ALUBA.

The four parts carry, respectively, 15%, 25%, 30%, and 30% of the marks.

4a Explain the write-through and the write-back strategies in the context of a memory hierarchy. Which one is adopted in virtual memory systems, and why?

b In a memory hierarchy involving a TLB, virtual memory and cache, a memory reference can encounter three different types of misses: a cache miss, a TLB miss, and a page fault. Provide a table showing all possible combinations of these three events, and explain:

i) why some combinations depend on only two of the events,

ii) why some combinations may not occur.

c The cache in a machine M1 has hit time h, miss rate m, and a miss penalty of p cycles. What is the average memory access time for M1?

d A machine M2 has a two-level cache. The level one cache has hit time h and miss rate m (same values as those for M1), while the level two cache has hit time αh, miss rate βm, and miss penalty p cycles.

i) What is the average memory access time for M2?

ii) Derive an expression for p, if the average memory access time for M2 is k times shorter than that for M1.

The four parts carry, respectively, 30%, 30%, 10%, and 30% of the marks.