

July 07

Paper Number(s): **E2.1**

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2007

EEE/ISE PART II: MEng, BEng and ACGI

DIGITAL ELECTRONICS 2

Monday, 4 June 2:00 pm

There are FOUR questions on this paper.

Q1 is compulsory.

Answer Q1 and any two of questions 2-4.

Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Time allowed: 2:00 hours

Examiners responsible:

First Marker(s): D.M. Brookes D.M. Brookes

Second Marker(s): T.J.W. Clarke T.J.W. Clarke

Information for Candidates:

Notation: *Unless explicitly indicated otherwise, digital circuits throughout this paper are drawn with their inputs on the left and their outputs on the right. The notation $X_{2:0}$ denotes the three-bit number X_2 , X_1 and X_0 . The least significant bit of a binary number is always designated bit 0. Signed binary numbers use 2's complement notation.*

1. (a) *Figure 1.1* shows the state table for a state machine which has a single input A and a state that is represented by the value of the unsigned 2-bit number S1:0. The table entries are of the form D1,D0 / X,Y where D1:0 denotes the next state and X and Y are the output signals during the current state. Draw the state diagram for the circuit and complete the timing diagram shown in *Figure 1.2* by showing the state of the circuit during each clock cycle as a decimal number and the waveforms of X and Y. State transitions occur on the rising edges of CLOCK which have been numbered on the diagram for convenience. The state sequence for the first four cycles is as shown in *Figure 1.2*.

[8]

S1,S0	A=0	A=1
00	00/00	01/10
01	11/11	11/11
10	00/00	10/00
11	00/10	10/10

Figure 1.1

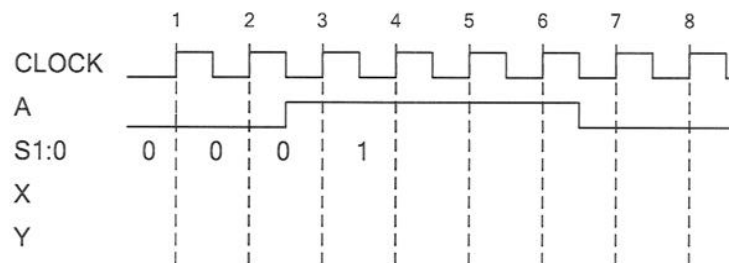


Figure 1.2

- (b) In the circuit of *Figure 1.3* the propagation delays of the inverter, logic block and flip-flops are t_g , t_d and t_p respectively and the flipflops have setup and hold times of t_s and t_h . The clock signal C is symmetrical with period T .
- Write the setup and hold inequalities that apply to the rightmost flip-flop.
 - Find the maximum clock frequency for the circuit if the timing parameters (in ns) are: $t_p = 6$, $t_s = 1$, $t_h = 3$, $t_g = 2$ and $4 \leq t_d \leq 25$

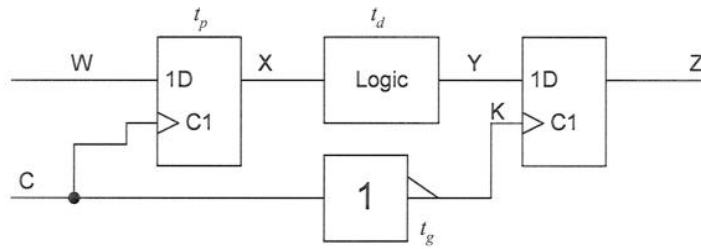


Figure 1.3

[8]

- (c) *Figure 1.4* shows a flash analogue-to-digital converter comprising three identical resistors, four comparators and a logic block. The output of a comparator is high whenever the voltage at the “+” input is greater than that at the “-“ input. The output X2:0 is an unsigned number whose value depends on the input voltage Z (in volts) as follows: [8]

$$X_{2:0} = \begin{cases} 0 & Z < 1 \\ 1 & 1 \leq Z < 3 \\ 2 & 3 \leq Z < 5 \\ 3 & 5 \leq Z < 7 \\ 4 & 7 \leq Z \end{cases}$$

- (i) Show the value of A, B, C and D for each of the input voltage ranges defined above.
- (ii) Derive simplified Boolean expressions for X2, X1 and X0.

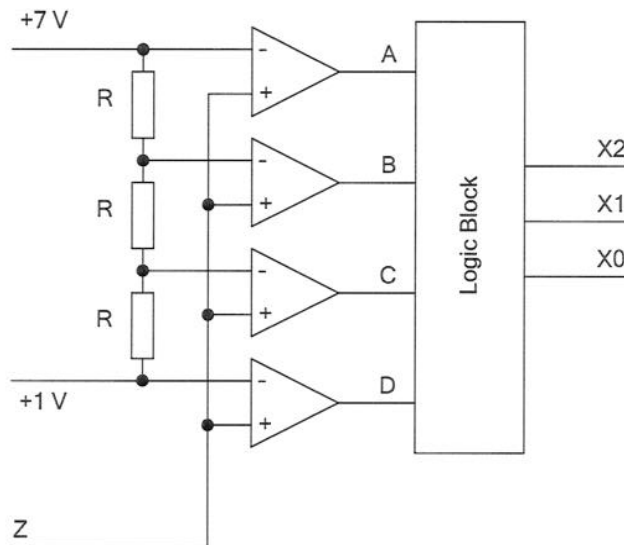


Figure 1.4

- (d) *Figure 1.5* shows a circuit that adds together four multi-bit numbers to give $Y = W + X = A + B + C + D$. The input numbers lie in the following ranges: $20 \leq A \leq 29$, $20 \leq B \leq 29$, $-19 \leq C \leq 0$, $-99 \leq D \leq -1$. [8]
- (i) For each of the numbers A, B, C, D, W, X and Y say whether it should be represented as an unsigned number or a signed 2's complement number and determine the number of bits needed to represent it without overflow.
- (ii) Determine how many full-adder stages are required for each adder. Do not include stages whose output is constant.

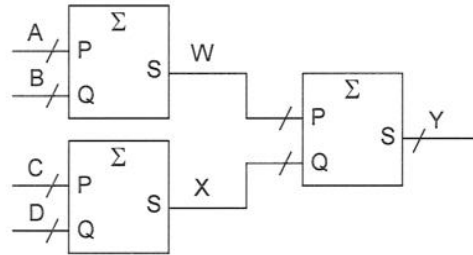


Figure 1.5

- (e) *Figure 1.6* shows part of a microprocessor system containing a Random Access memory (RAM) and a Read-Only memory (ROM). [8]

The outputs of the decode logic are as follows:

$$CEA = (\overline{A15} + \overline{A14}) \cdot (A15 + A14 + A13 + A12 + A11 + A10 + A9 + A8)$$

$$CEB = A15 \cdot A14 \cdot (\overline{A13} + \overline{A12}) + \overline{A15} \cdot \overline{A14} \cdot \overline{A13} \cdot \overline{A12} \cdot \overline{A11} \cdot \overline{A10} \cdot \overline{A9} \cdot \overline{A8}$$

Determine the ranges of hexadecimal memory addresses to which each device responds.

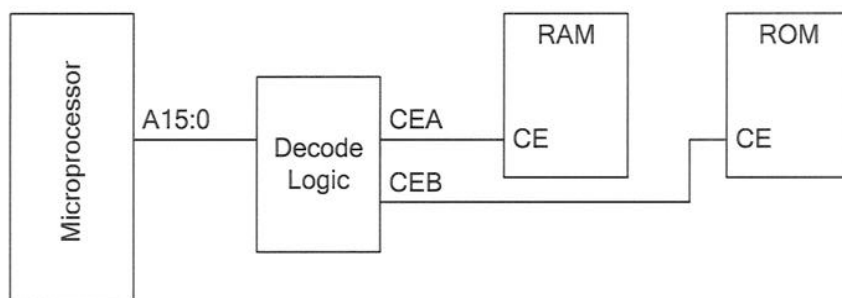


Figure 1.6

2. *Figure 2.1* shows a circuit consisting of a 6-bit carry-save adder, an 11-bit register and a $\times 2$ block. The outputs of the carry-save adder are defined by $S_i = P_i \oplus Q_i \oplus R_i$ and $C_i = P_i \cdot Q_i + P_i \cdot R_i + Q_i \cdot R_i$ for $i = 0, 1, \dots, 5$. The C5 output from the adder is not used elsewhere in the circuit. We denote by p the value of the unsigned binary number P5:0 and similarly for the other 6-bit numbers q, r , and s and the 5-bit numbers c and y .
- The “ $\times 2$ ” block calculates $q = 2y$. Give Boolean expression for Q5, Q4, ..., Q0. [2]
 - Explain why the propagation delay of a 6-bit carry-save adder is less than that of a conventional 6-bit adder. [2]
 - Show that $p + q + r = 2c + s$ provided that $p + q + r < 64$. [3]
 - Complete the timing diagram of *Figure 2.1* by giving the decimal values of q, r, c, s and $2c + s$ during each CLOCK cycle. The value of p changes shortly after the rising edge of CLOCK. [8]
 - The sequence of p values shown in *Figure 2.1* consists of three non-zero values followed by three zero values. Giving your reasons fully, determine how many zero values it is necessary to append to an arbitrary sequence of non-zero values to ensure that $c = 0$ during the last of the appended zero values. [3]
 - If a similar circuit were used to add together 128 8-bit unsigned numbers, determine the required bit-width of the carry-save adder and the total number of clock cycles needed for the addition. [2]

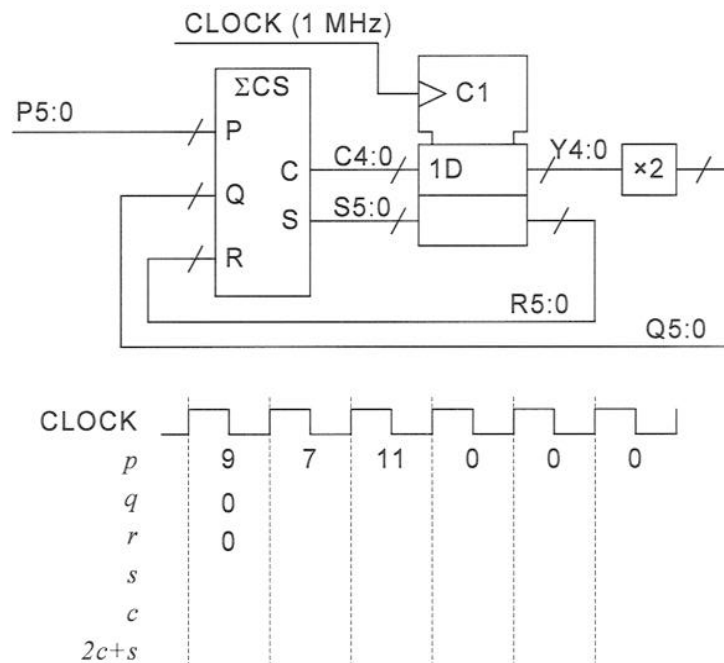


Figure 2.1

3. A synchronous state machine has a single input signal, P, which changes shortly after the rising edge of CLOCK. The state machine's two output signals X and Y change in response to the sequence of values taken by P in the previous two or three clock cycles as follows: X goes high following the sequence 0,0 and low again following either of the sequences 1,1 or 1,0,1; Y goes high following 1,1 and low again following either 0,0 or 0,1,0. In all other situations, X and Y keep their previous values. The state machine is a Moore machine, i.e. its outputs depends only on the current state.

Figure 3.1 illustrates the waveforms of X and Y for a particular input signal P.

- (a) Explain why the specifications given above mean that X and Y will never be high at the same time. [2]
- (b) Complete the timing diagram of Figure 3.1 by finding a sequence of states, a, b, c, ... that are compatible with the specifications given above. [8]
- (c) Draw the state diagram for your design ensuring that for each state, the outputs and state transitions are fully specified. [8]
- (d) Determine the shortest input sequence that will take the state machine to a state with $X=Y=0$ regardless of its initial state. [2]

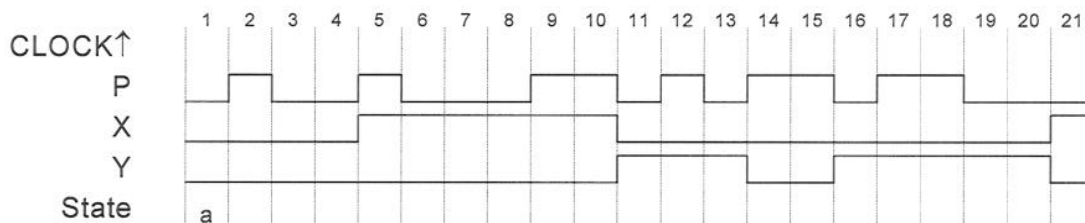


Figure 3.1

4. *Figure 4.1* shows a circuit for transposing a 4×4 matrix whose elements are 8-bit integers. The circuit includes a 6-bit binary counter, a 16×8-bit Random Access Memory (RAM), a negative-edge triggered flipflop, a logic block and a number of gates. The counter has a synchronous reset input and data is read from or written to the RAM when OE or WEN respectively are taken high. All signal transitions occur shortly after the CLOCK rising edge.

The timing diagram of *Figure 4.1* shows the operation of the circuit while performing the following matrix transposition:

$$\begin{pmatrix} 1 & 2 & 3 & 4 \\ 5 & 6 & 7 & 8 \\ 9 & 10 & 11 & 12 \\ 13 & 14 & 15 & 16 \end{pmatrix} \longrightarrow \begin{pmatrix} 1 & 5 & 9 & 13 \\ 2 & 6 & 10 & 14 \\ 3 & 7 & 11 & 15 \\ 4 & 8 & 12 & 16 \end{pmatrix}$$

Initially, RX is taken high for 32 clock cycles and the matrix elements are presented for two cycles each on DIN7:0 in the order 1, 2, 3, ..., 14, 15, 16 and are stored in the RAM in consecutive memory addresses beginning at address 0. RX is then taken low, and during the following 32 clock cycles, the matrix is then read out of the RAM in transposed order (1, 5, 9, ..., 8, 12, 16) while the signal TX is kept high. The circuit then becomes inactive until RX again goes high. The 64 clock cycles required for the operation are numbered 0, 1, ..., 63 on the timing diagram; note that in two places a number of clock cycles have been omitted and are indicated by a pair of closely-spaced parallel lines.

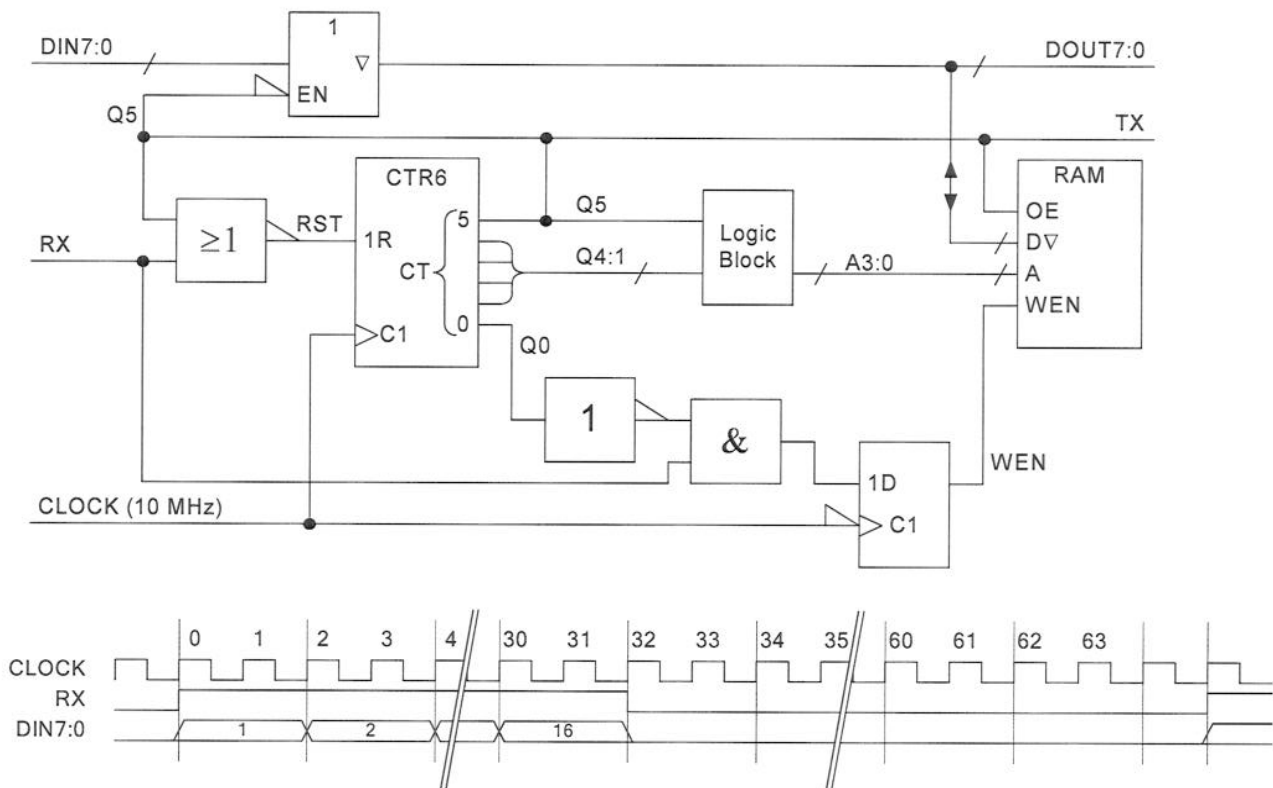


Figure 4.1

- (a) The “Logic Block” maps the counter outputs Q4:1 onto the RAM address inputs A3:0. The mapping depends on whether Q5 is low or high according to the following table:

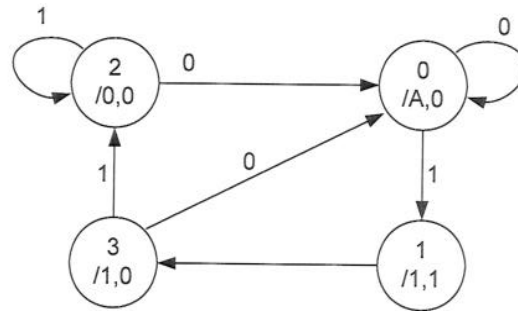
Q5=0	Q5=1
A3=Q4	A3=Q2
A2=Q3	A2=Q1
A1=Q2	A1=Q4
A0=Q1	A0=Q3

- Show how this mapping may be implemented using a multiplexer and explain how it achieves the matrix transposition. [3]
- (b) Explain why it is necessary for the input data DIN7:0 to be connected to the RAM data lines via a tri-state buffer rather than being connected directly. [2]
- (c) Explain the circumstances under which the counter will be reset and show that the counter value is equal to the clock cycle numbers given in *Figure 4.1*. Determine the value of the counter, Q5:0, during the final two cycles of the timing diagram. [3]
- (d) Complete the timing diagram by showing the waveforms of WEN and TX and the decimal values taken by A3:0 and DOUT7:0 during each cycle. You may assume that the counter is initially reset. [12]

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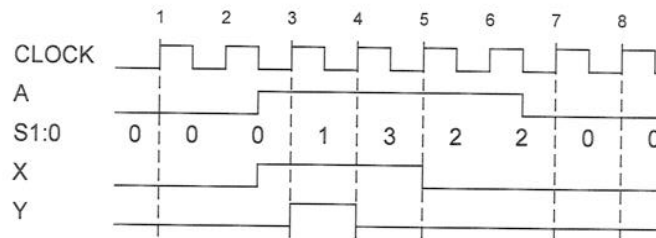
Key to letters on mark scheme: B=Bookwork, C=New computed example, A=Analysis of new circuit, D=design of new circuit

1 (a)



I/O Signals: A/X, Y

[5A]



[3A]

(b) The setup equation is:

$$t_p + t_d + t_s < t_g + \frac{1}{2}T \Rightarrow 6 + 25 + 1 - 2 < \frac{1}{2}T \Rightarrow T > 60$$

The hold time equation is:

$$t_g + t_h < \frac{1}{2}T + t_p + t_d \Rightarrow 2 + 3 - 6 - 4 < \frac{1}{2}T \Rightarrow T > -10$$

$$\text{Hence } T > 60 \text{ ns} \Rightarrow f < 16.7 \text{ MHz}$$

[8C]

(c) We can construct the following table:

Z	A,B,C,D	x	X2, X1, X0
$Z < 1$	0000	0	000
$1 \leq Z < 3$	0001	1	001
$3 \leq Z < 5$	0011	2	010
$5 \leq Z < 7$	0111	3	011
$7 \leq Z$	1111	4	100

[4A]

From which we get

$$X2 = A$$

$$X1 = C \cdot \bar{A} = A \oplus C$$

$$X0 = \bar{B}\bar{A} + D\bar{C} = \bar{A}D(\bar{B} \oplus \bar{C}) = B \oplus C \oplus D = A \oplus B \oplus C \oplus D$$

[4A]

- (d) (i) A and B require 5 bits as unsigned numbers (0 to 31), C requires 6 bits (-32 to +31) and D requires 8 bits (-128 to +127).

[5A]

$40 \leq W \leq 58$ so W requires 6 bits (0 to 63), $-118 \leq X \leq -1$ and so requires 8 bits. Finally $-78 \leq Y \leq 58$ and also requires 8 bits.

- (ii) A4 and B4 are always 1 and result in $W5=1$ always. So, we can use a 4-bit adder to add together A3:0 and B3:0 and use the carry out to generate W4.

[3A]

X requires 8 bits, but its sign bit, X7, is always 1, so we only need 7 adder stages.

Finally Y needs 8 adder stages giving a total of $8+7+4=19$.

- (e) $\bar{A}15 + \bar{A}14$ is true for the range 0000 to BFFF. However we also require $A15 + A14 + A13 + A12 + A11 + A10 + A9 + A8$ to be true and this excludes 0000 to 00FF. Thus the RAM responds to 0100 to BFFF.

[8A]

The ROM responds to two disjoint ranges: C000 to EFFF due to the term $\bar{A}15 \cdot \bar{A}14 \cdot (\bar{A}13 + \bar{A}12)$ and also to 0000 to 00FF due to $\bar{A}15 \cdot \bar{A}14 \cdot \bar{A}13 \cdot \bar{A}12 \cdot \bar{A}11 \cdot \bar{A}10 \cdot \bar{A}9 \cdot \bar{A}8$.

2. (a) $Q_{5:0} = [Y_4, Y_3, Y_2, Y_1, Y_0, 0]$ [2D]
- (b) In a carry-save adder, each bit is calculated independently with its own S and C outputs. There is therefore no delay due to the carry propagation between bit positions. [2B]
- (c) We can see from a truth table that $P_i + Q_i + R_i = 2C_i + S_i$ for any given bit position:

P_i	Q_i	R_i	C_i	S_i	$2C_i + S_i$
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	1
0	1	1	1	0	2
1	0	0	0	1	1
1	0	1	1	0	2
1	1	0	1	0	2
1	1	1	1	1	3

Since all bits are independent, it follows that $\sum_{i=0}^5 2^i (P_i + Q_i + R_i) = \sum_{i=0}^5 2^i (2C_i + S_i)$ [3A]
 and this implies that $p + q + r = 2c + s$ provided that $C_5 = 0$. C_5 can only equal 1 if at least two of P_5 , Q_5 and R_5 equal 1 and this implies that $p + q + r \geq 64$.

(d)

CLOCK	1	2	3	4	5	6
p	9	7	11	0	0	0
q	0	0	2	20	8	0
r	0	9	14	7	19	27
s	9	14	7	19	27	27
c	0	1	10	4	0	0
$2c + s$	9	16	27	27	27	27

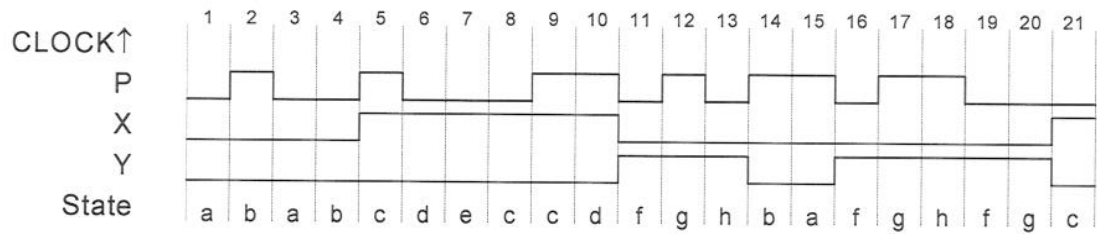
[8A]

- (e) Q_0 is always 0, so during the clock cycle containing the first of the trailing zeros, we have $P_0 = Q_0 = 0 \Rightarrow C_0 = 0$. Because Q is a shifted version of Y , this implies that during the next clock cycle $Q_1:0 = 0 \Rightarrow C_1:0 = 0$. Thus in each successive cycle one additional bit of $C_{4:0}$ is forced to 0 and during the fifth such cycle, we have $C_{4:0} = 0$. [3A]
- (f) Since $128 = 2^7$ the carry-save adder must be $8 + 7 = 15$ bits wide but the $C_{13:0}$ outputs need only be 14 bits. Thus you will need $128 + 14 = 142$ clock cycles for the addition. [2A]

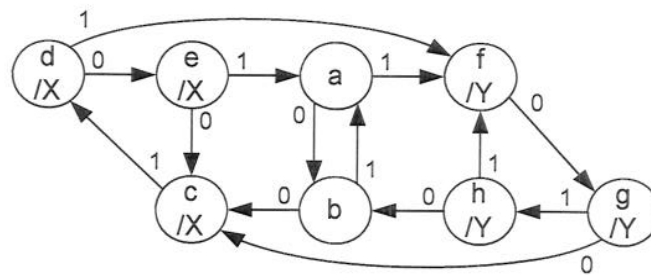
3. (a) X goes high only in response to the sequence 00 but this sequence also forces Y low. Similarly the only sequence that makes Y go high (11) also makes X go low.

[2A]

(b,c)



[8D]

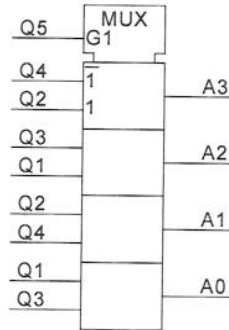


[8D]

- (d) 0,1,0,1 will always reach state "a"

[2A]

4. (a) The mapping is straightforward with a multiplexer:



When $Q5=1$, this maps $Q4:1=[0,1,2,3,4,5,\dots,15]$ onto $A3:0=[0,4,8,12,1,5,\dots,15]$ which will address the matrix elements in the correct order to read out its transpose.

[3D]

- (b) During the first half of the operation, $Q5=0$ so the tri-state buffer will be enabled and $DIN7:0$ will be connected to the RAM data inputs. However during the second half, when $Q5=1$, the RAM output enable signal (OE) will be high and the RAM will drive its data lines. To avoid a conflict, the input tri-state buffers will be turned off.

[2B]

- (c) The counter reset input, RST, will be high when RX and $Q5$ are both low, i.e. when no input data is available and the counter is not in the range 32,...,63. Since RX goes high slightly after the CLOCK edge, the counter will remain at 0 until the next rising edge when it will increment to 1 as shown on the timing diagram. When the counter reaches 32, RX goes low. However, since $Q5$ is now high, the counter will continue counting until it wraps around to zero in the penultimate cycle of the timing diagram. RST will now go high and so the counter will remain at 0 until the cycle after RX goes high. Thus $Q5:0$ will equal 0 for both of the final two cycles.

[3A]

- (d) WEN goes high on the falling edge of CLOCK when $RX=1$ and the counter value is even. The ? values of $DOUT7:0$ are equal to the value of $DIN7:0$.

[12A]

