IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2006

EEE/ISE PART I: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 1

Corrected Copy

Monday, 5 June 10:00 am

Time allowed: 2:00 hours

There are FOUR questions on this paper.

Q1 is compulsory.
Answer Q1 and any two of questions 2-4.
Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : A.S. Holmes, .
Second Marker(s) : S. Lucyszyn,

1. **This question is compulsory**. You should attempt all six parts. State clearly any assumptions made in your calculations.

   a) For the circuit in Figure 1.1, determine the operating mode of the transistor and calculate its collector current.

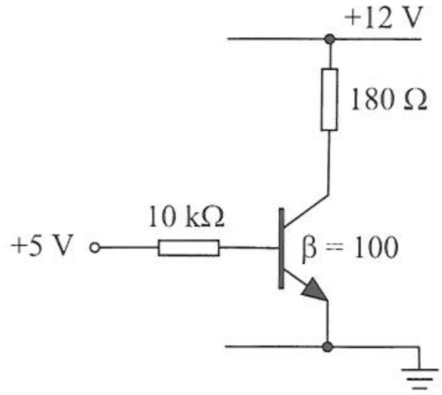


Figure 1.1 [5]

   b) State the operating modes of both MOSFETs in Figure 1.2, and determine the value of the voltage V.

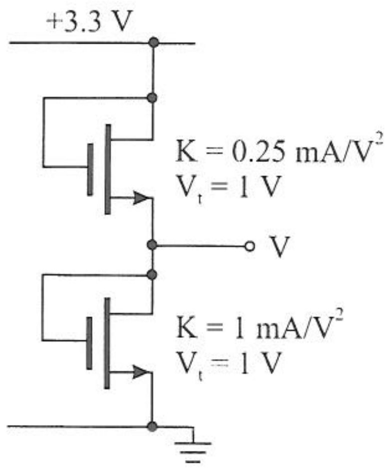
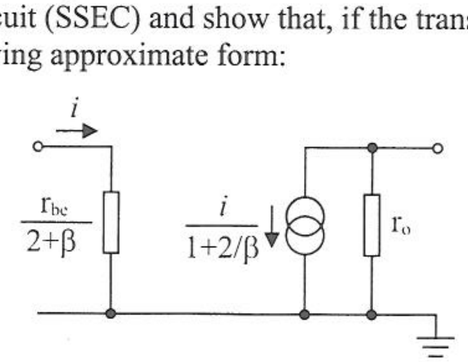


Figure 1.2 [5]

   c) Draw the circuit for a simple BJT current mirror. Also draw the corresponding small-signal equivalent circuit (SSEC) and show that, if the transistors are matched, it can be reduced to the following approximate form:



[8]

Question 1 continues on the next page...

d) Figure 1.3 shows a differential amplifier based on a pair of matched BJTs. Starting from the large signal transistor equations, derive the large signal input-output relationship for the amplifier when both transistors are active. Hence draw a dimensioned sketch showing the variation of V_{OUT} with V_{IN} covering the input voltage range $-0.5\text{ V} \leq V_{IN} \leq +0.5\text{ V}$.

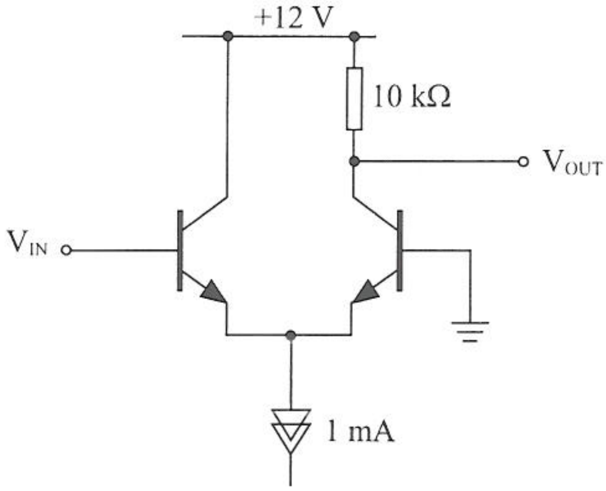


Figure 1.3 [10]

e) The voltage V_I applied to the circuit in Figure 1.4 changes suddenly from +5 V to 0 V at time t = 0, after having been held at +5 V for a long time. Calculate duration T of the resulting output pulse, and sketch the time-variations of V_B and V_C over the time interval $-T \leq t \leq 2T$.

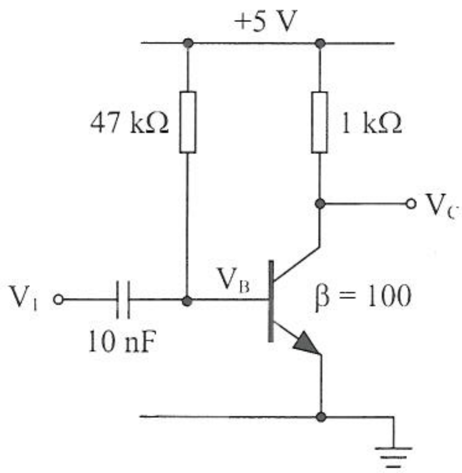


Figure 1.4 [8]

f) State and explain conditions that must be satisfied by the loop gain of a transistor circuit in order for the circuit to generate sinusoidal oscillations of stable amplitude. [4]

2. Figure 2.1 shows a common-emitter amplifier, connected between an AC-coupled signal source and a capacitive load. The circuit is to be manufactured using a transistor with a nominal β value of 100.

   a) Determine the quiescent output voltage and collector bias current for the case $\beta = 100$, stating clearly any assumptions you make. What range of collector bias currents might be expected in practice if the transistor β value is guaranteed only to lie in the range 50 to 150? [8]

   b) Draw a small-signal equivalent circuit for the amplifier, replacing the RC network in the emitter by an equivalent impedance Z_E, and show that the small-signal voltage gain may be written as:

$$A_V = \frac{-\alpha R_C}{r_e + Z_E}$$

   where R_C is the load resistance in the collector. You may neglect the small-signal output resistance of the transistors. Hence evaluate A_V both in the mid-band, where C_E is effectively short-circuit, and at low frequency where C_E is effectively open-circuit. [12]

   c) Choose the value to C_E so that the 3-dB point at the low-frequency end of the mid-band occurs at 1 kHz. Also determine the cut-off frequency associated with the load capacitor, and hence sketch a Bode plot showing the variation of the in-circuit gain v_L/v_S with frequency over the frequency range 1 Hz to 1 MHz. You should ignore the effect of the AC-coupling capacitor at the input. [10]

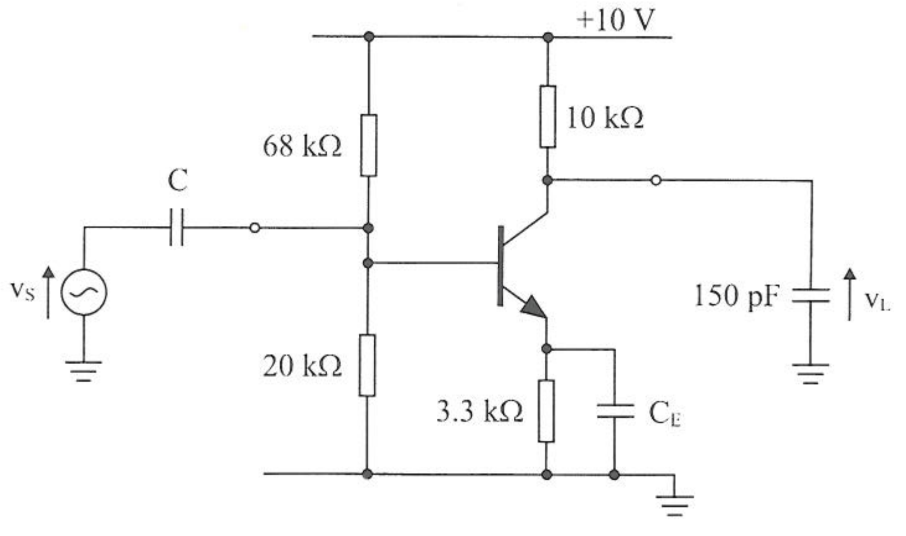


Figure 2.1

3. Figure 3.1 shows a single-stage amplifier in which a depletion MOSFET provides the active load for an enhancement MOSFET.

   a) Determine the quiescent values of the drain current and the output voltage, and verify that both transistors are in the active region of operation. What is the minimum supply voltage for which both transistors will remain active in the absence of an input signal? [9]

   b) Draw a small-signal equivalent circuit of the amplifier, and hence determine its mid-band small-signal voltage gain. Your calculation should take into account the 1 MΩ resistor. Also determine the small-signal input resistance of the circuit. [15]

   c) Describe the *body effect*, and explain its implications for a circuit of the kind shown in Figure 3.1 when implemented using NMOS technology. [6]

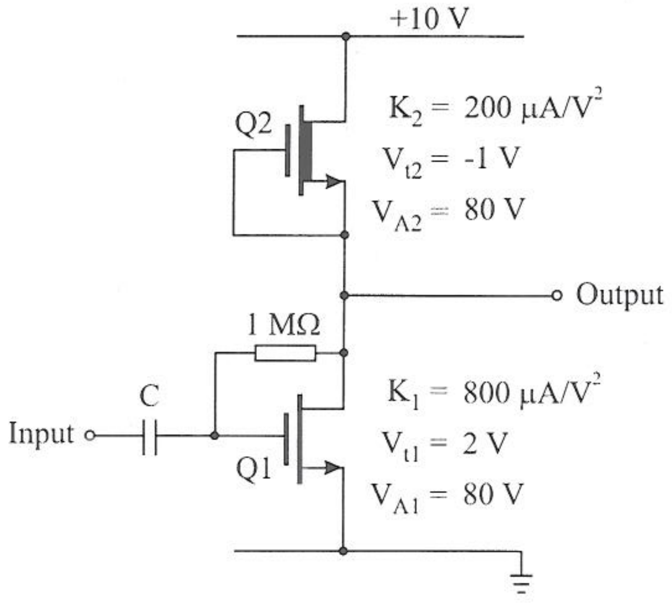


Figure 3.1

4. a) Derive an expression for the small-signal output resistance of an emitter follower (common-collector amplifier), in terms of the resistance R_S of the input source, the transistor's current gain and the transistor's emitter resistance. [10]

b) Using your answer to part a), or otherwise, show that the small-signal output resistance of the so-called Darlington pair in Figure 4.1 is given by:

$$2r_e + \frac{R_S}{(1+\beta)^2}$$

where r_e is the emitter resistance of the right-hand transistor, and both transistors have the same β value. [12]

c) The circuit in Figure 4.2 is to be used to supply a stable voltage to a variable load. What is the nominal output voltage, V, and by approximately how much will this vary when the load current changes from 500 mA to 550 mA? [8]

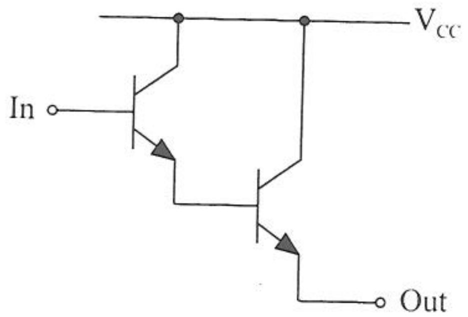


Figure 4.1

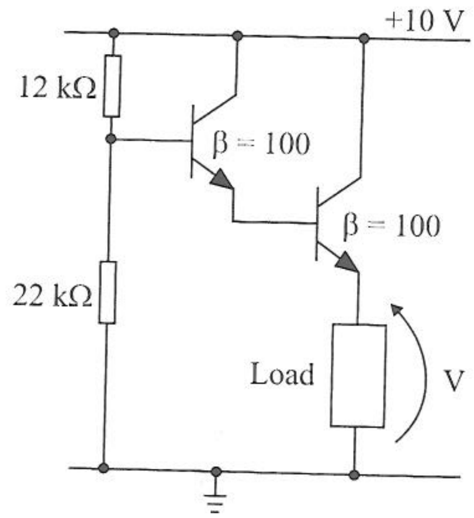


Figure 4.2

E1.4 Master solutions - June '06

Analogue Electronics I

1 a) Assuming $V_{BE} \sim 0.7V$, $I_B = (5-0.7)/10k = 0.43$ mA

If transistor active then $I_C = \beta I_B = 43$ mA

In this case $V_c = 12 - 43\times10^{-3}\times 180 = 4.26$ V

Calculated V_C is $> V_B$ ⇒ transistor is indeed ACTIVE

with $I_C = 43$ mA [5]

b) Both (enh. mode) MOSFETs have $V_G = V_D$ ⇒ active if above threshold. Also, $V_{DD} > V_{t1} + V_{t2}$ ⇒ both above threshold

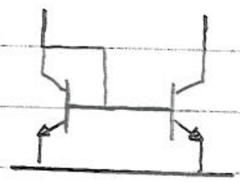
⇒ Both ACTIVE

Common I_D given by $I_D = k_1(V - V_{t1})^2 = k_2(3.3 - V - V_{t2})^2$

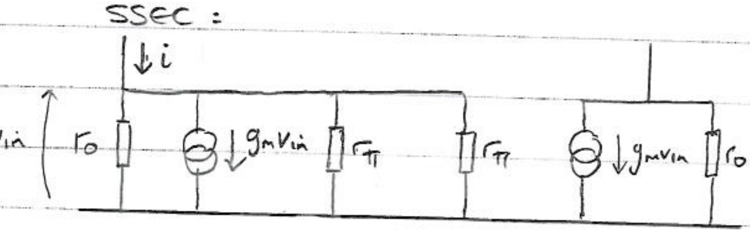
$\sqrt{}$ and rearrange ⇒ $V = \left[3.3 - V_{t2} + \sqrt{k_1/k_2}\cdot V_{t1}\right]/\left(1+\sqrt{k_1/k_2}\right)$

Putting $V_{t1} = V_{t2} = 1V$, $\sqrt{k_1/k_2} = 2$ ⇒ $V = 1.43$ V [5]

c) BJT current mirror:



SSEC:



LH current source can be redrawn as $1/g_m$ and, neglecting r_o (because $r_o \gg r_\pi, \frac{1}{g_m}$), combined resistance at input side is

$R_{in} \simeq 1/g_m \,//\, r_\pi \,//\, r_\pi = \left(\frac{\beta}{r_\pi} + \frac{1}{r_\pi} + \frac{1}{r_\pi}\right)^{-1} = \left(\frac{2+\beta}{r_\pi}\right)^{-1}$

where we have used $g_m^{-1} = r_\pi/\beta$

RH current source is $g_m v_{in} = g_m R_{in}\, i \simeq \frac{\beta}{r_\pi}\cdot\frac{r_\pi}{2+\beta}\cdot i = \frac{i}{1+2/\beta}$

⇒ SSEC reduces to form shown. [8]

d) Collector currents are $I_{C1} = I_S \exp\left(\frac{V_{IN} - V_E}{V_T}\right)$, $I_{C2} = I_S \exp\left(\frac{-V_E}{V_T}\right)$

where V_E = (common) emitter voltage

⇒ $I_{C1}/I_{C2} = \exp(V_{IN}/V_T)$ .... (1)

Neglecting base currents, $I_{C1} + I_{C2} = I$ -- (2) $(I = 1\text{mA})$

Eliminating I_{C1} from (1) & (2) ⇒ $I_{C2} = \frac{I}{1+\exp(V_{IN}/V_T)}$

Continued ..

1 d) continued

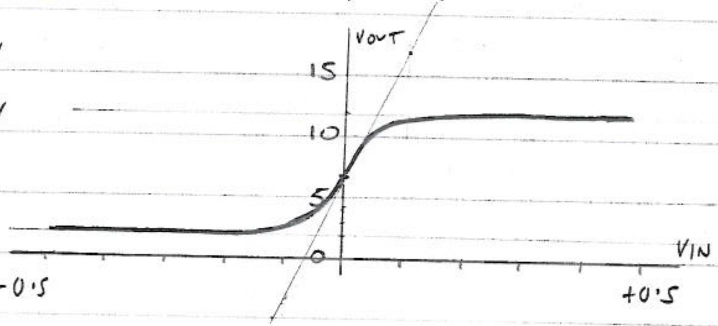
$$V_{OUT} = +12V - 10K \times I_{C2} = 12 - \frac{10}{1 + \exp(40 V_{IN})}$$

For $V_{IN} \lesssim -0.1$, $V_{OUT} \simeq +2V$

For $V_{IN} \gtrsim +0.1$, $V_{OUT} \simeq +12V$

@ $V_{IN} = 0$, $V_{OUT} = +7V$

with $\frac{dV_{OUT}}{dV_{IN}} = 100$ V/V



[10]

e) $I_{CAP} = 0$ before i/p transition (because V_1 has bee stable for a long time).

$\Rightarrow$ For $t<0$, $I_B = (5-0.7)/47k = 91.5\,\mu A$

If transistor active, then $I_C = \beta I_B = 9.15$ mA. But this would imply $V_C < 0$ $\Rightarrow$ transistor actually saturated with $V_C \sim 0.2V$.

At $t=0^-$, $V_{CAP} = V_1 - V_B \simeq 4.3$ V. V_{CAP} continuous, so at $t=0^+$ $V_B = V_1 - V_{CAP} = -4.3$ V and transistor cuts off.

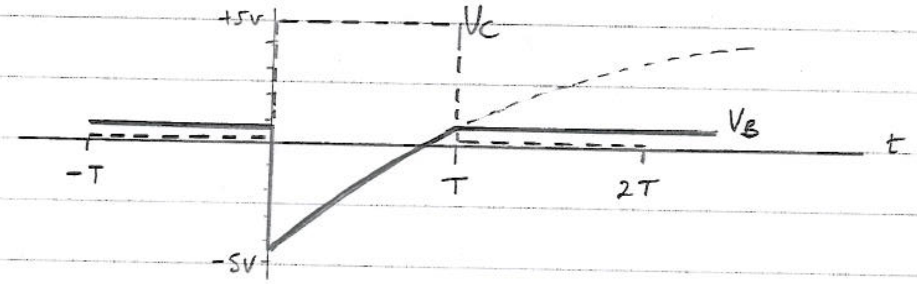
Time variation of V_B for $0 \leq t \leq T$ given by standard solution for RC network:

$$V_B = +5V + (-4.3 - 5)e^{-t/\tau} \qquad \tau = 47k \times 10nF$$

$$= 5 - 9.3e^{-t/\tau} \qquad = 470\,\mu sec$$

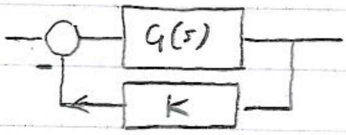
Transistor turns ON again when V_B reaches $0.7V$, ie at time T where

$$0.7 = 5 - 9.3e^{-T/\tau} \qquad T = \tau \ln\left[\frac{9.3}{4.3}\right] = \underline{\underline{363\,\mu sec}}$$



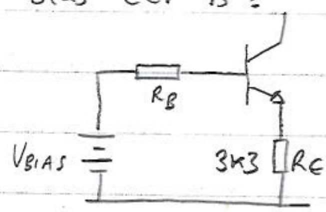
[8]

f) Assume system of form. Closed loop transfer function



is $H(s) = G(s)/[1 + KG(s)]$ and for cct to generate stable sinusoidal oscillations require $1 + KG(s) = 0$ to have one pure imaginary root and no roots with $Re(s) > 0$. [4]

2 a) Bias cct is :



where $V_{BIAS} = \frac{20}{20+68} \times 10 = 2.27\text{ V}$

$R_B = 20//68 = 15.45\text{ k}\Omega$

KVL : $I_E R_E + V_{BE} + I_B R_B = V_{BIAS}$

$\Rightarrow I_E = \dfrac{V_{BIAS} - V_{BE}}{R_E + \frac{R_B}{1+\beta}}$ .... ①

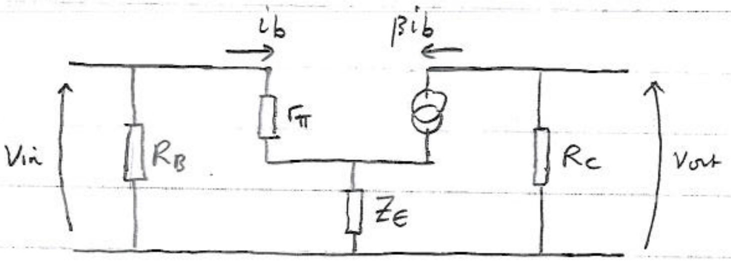
$V_{BIAS} = 2.27$, $V_{BE} = 0.7$, $R_E = 3.3\text{k}$, $R_B = 15.45\text{k}$, $\beta = 100$ $\Rightarrow$ $I_E = 0.455\text{ mA}$

$\underline{I_C = \alpha I_E = 0.45\text{ mA}}$

$V_{OUT} = +10 - I_C \times 10\text{k}$ $\Rightarrow$ $\underline{V_{OUT} = +5.5\text{V}}$

Substituting $\beta = 50, 150$ into ① $\Rightarrow$ $\underline{0.431\text{ mA} \le I_C \le 0.457\text{ mA}}$ [8]

b) SSEC :



$g_m = I_C/V_T = 0.018\text{ S}$

$r_\pi = \beta/g_m = 5.\dot{5}\text{ k}\Omega$

$r_e = I_E/V_T = 55\ \Omega$

KVL on i/p side : $v_{in} = i_b r_\pi + (1+\beta) i_b Z_E$ -- ②

KVL on o/p side : $V_{out} = -\beta i_b R_C$ ... ③

③/② $\Rightarrow$ $A_v = \dfrac{V_{out}}{V_{in}} = \dfrac{-\beta R_C}{r_\pi + (1+\beta) Z_E} = -\dfrac{\alpha R_C}{r_e + Z_E}$

where we have used $r_e = r_\pi/(1+\beta)$, $\alpha = \beta/(\beta+1)$

$Z_E = \left(R_E // \frac{1}{j\omega C_E}\right) = R_E/(1 + j\omega R_E C_E)$ where $R_E = 3.3\text{ k}\Omega$

In midband can assume $|Z_E| << r_e$ $\Rightarrow$ $\underline{A_v} \simeq -\dfrac{\alpha R_C}{r_e} = -g_m R_C = \underline{-180}$

At low frequency $\omega R_E C_E << 1$, $Z_E \simeq R_E$ $\Rightarrow$ $\underline{A_v} \simeq -\dfrac{\alpha R_C}{r_e + R_E} = \underline{-2.95}$

[12]

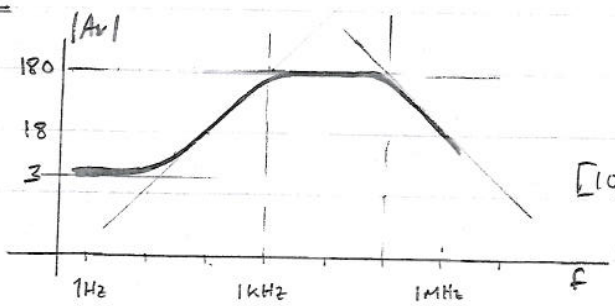
c) At lower end of midband, $Z_E \simeq \frac{1}{j\omega C_E}$ and $A_v \simeq \dfrac{-\alpha R_C}{r_e + \frac{1}{j\omega C_E}}$

3dB pt occurs at f_1 where $2\pi f_1 r_e C_E = 1$

For $f_1 = 1\text{kHz}$ require $\underline{C_E = 2.89\ \mu\text{F}}$

High-freq cut-off occurs at f_2 where $2\pi f_2 R_C C_L = 1$

$C_L = 150\text{pF}$, $R_C = 10\text{k}\Omega$ $\Rightarrow$ $\underline{f_2 = 106\text{ kHz}}$



[10]

3 a) Q2 has $V_{GS} = 0$ $\Rightarrow$ assuming active, $\underline{\underline{I_D = K_2 V_{t2}^2 = 0.2\,mA}}$

Q1 has $V_{GS} = V_{DS} = V_{OUT}$ $\Rightarrow$ active if above threshold,

with $I_D = K_1 (V_{OUT} - V_{t1})^2$ $\Rightarrow$ $V_{OUT} = V_{t1} \pm \sqrt{I_D / K_1}$

taking +ve root ($> V_{t1}$) $\Rightarrow$ $\underline{\underline{V_{OUT} = 2 + \sqrt{0.2/0.8} = 2.5\,V}}$

Check modes:

Q1 has $V_{GS} = 2.5\,V > V_t = 2\,V$ and $V_{DS} = 2.5 > 2.5 - 2$ $\Rightarrow$ ACTIVE

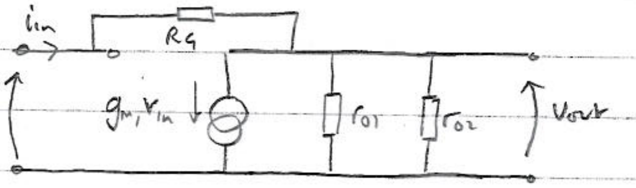
Q2 has $V_{GS} = 0\,V > V_t = -1$ and $V_{DS} = 7.5 > 0 - -1$ $\Rightarrow$ ACTIVE

While Q2 remains active, we know Q1 active with $V_{OUT} = 2.5\,V$

For Q2 to remain active require $(V_{DD} - V_{OUT}) \geq +1\,V$

Combining these, require $\underline{\underline{V_{DD} \geq 2.5 + 1 = 3.5\,V}}$ for both to remain ACTIVE [9]

b) SSEC in mid-band:



$g_{m1} = 2\sqrt{k_1 I_D} = 0.8\,mA/V$

$r_{o1} = r_{o2} = \dfrac{V_A}{I_D} = 400\,k\Omega$

$R_G = 1\,M\Omega$

KVL @ o/p: $\dfrac{V_{out}}{r_{o1}} + \dfrac{V_{out}}{r_{o2}} + \dfrac{V_{out} - V_{in}}{R_G} + g_{m1} V_{in} = 0$

Rearranging $\Rightarrow$ $A_v = \dfrac{V_{out}}{V_{in}} = -\left(g_{m1} - \dfrac{1}{R_G}\right) \cdot \left(r_{o1} \| r_{o2} \| R_G\right)$

$\Rightarrow$ $\underline{\underline{A_v = -133.2}}$

KCL @ i/p: $i_{in} = (V_{in} - V_{out})/R_G = V_{in}(1 - A_v)/R_G$

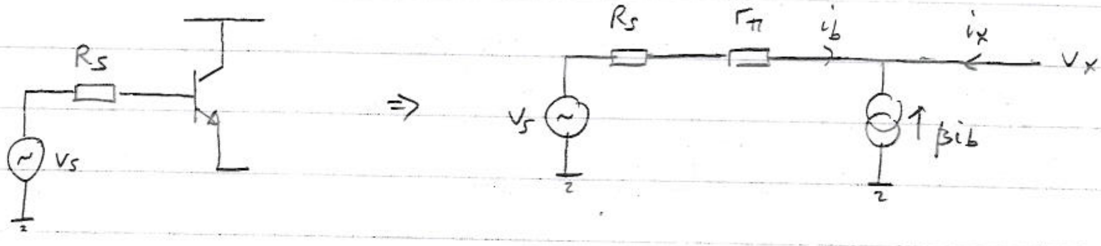
$\Rightarrow$ $V_{in}/i_{in} = R_G/(1 - A_v) = 1\,M\Omega / 134.2 = \underline{\underline{7.45\,k\Omega = R_{in}}}$

[15]

c) Body effect is modulation of channel conductivity due to variations in voltage between source and substrate (body contact). In NMOS body contact is common to all devices and at signal ground. For circuit in Fig 3.1, modulation of Q2's channel due to signal voltage V_{bs} between body (Gnd) and source (V_{out}) significantly reduces effective o/p resistance and hence voltage gain.

[6]

4 a) Emitter follower:



$R_o = V_x / i_x$ when $V_s = 0$

KCL @ o/p $\Rightarrow$ $i_x = -(\beta+1)\, i_b$

Also $V_x = -(R_s + r_\pi)\, i_b$

$$\Rightarrow \frac{V_x}{i_x} = R_o = \frac{R_s + r_\pi}{1+\beta}$$

$$= \frac{R_s}{1+\beta} + r_e \qquad [10]$$

b) o/p resistance of LH transistor (Q1) $= \dfrac{R_s}{1+\beta} + r_{e1}$

$\Rightarrow$ o/p resistance of Q2 $= \dfrac{R_s/(1+\beta) + r_{e1}}{1+\beta} + r_{e2}$

$$R_o = R_s/(1+\beta)^2 + r_{e1}/(1+\beta) + r_{e2}$$

But $I_{E2} = (1+\beta) I_{E1}$ $\Rightarrow$ $r_{e1}/(1+\beta) = r_{e2} = r_e$

$$\Rightarrow \quad R_o = \frac{R_s}{(1+\beta)^2} + 2 r_e \quad \text{as reqd} \qquad [12]$$

c) To get nominal o/p voltage, neglect base current. Then voltage on base of LH transistor is:-

$\dfrac{22}{22+12} \times 10 = 6.47\,V$ and $V_{OUT} \simeq 6.47 - 2 \times 0.7$

$$= \underline{\underline{5.07 \simeq 5V}}$$

At $I_{LOAD} \sim 500\,mA$ $\quad r_e = \dfrac{25\,mV}{500\,mA} \simeq 0.05\,\Omega$

and $\dfrac{R_s}{(1+\beta)^2} = \dfrac{22k \,//\, 12k}{(101)^2} = 0.76\,\Omega$

$\Rightarrow$ Total o/p resistance is $R_o \simeq 0.86\,\Omega$ dominated by source resistance term.

Change of $\Delta I = 50\,mA$ in load current will produce a change of $\underline{\underline{\Delta V = R_o \Delta I \simeq 43\,mV}}$ in the o/p voltage $\qquad$ [8]