

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING  
EXAMINATIONS 2005

EEE/ISE PART I: MEng, BEng and ACGI

Corrected Copy

**ANALOGUE ELECTRONICS 1**

Friday, 3 June 10:00 am

Time allowed: 2:00 hours

**There are FOUR questions on this paper.**

**Q1 is compulsory.**

**Answer Q1 and any two of questions 2-4.**

**Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).**

**Any special instructions for invigilators and information for candidates are on page 1.**

Examiners responsible

First Marker(s) : A.S. Holmes, A.S. Holmes

Second Marker(s) : S. Lucyszyn, S. Lucyszyn

1. **This question is compulsory.** You should attempt all six parts. State clearly any assumptions made in your calculations.

- a) For the BJT in Figure 1.1, choose the values of  $R_B$  and  $R_C$  to give a collector current of 1 mA and a collector voltage of +5 V.

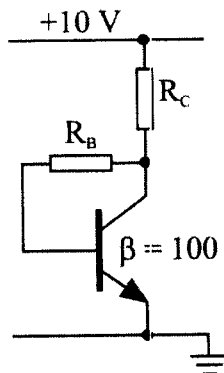


Figure 1.1

[6]

- b) Determine the drain current and drain voltage of the MOSFET in Figure 1.2. What is the minimum supply voltage for which the MOSFET will remain active?

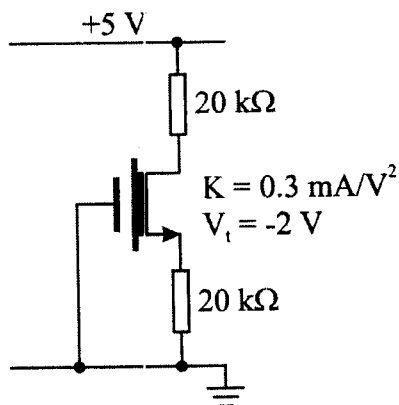


Figure 1.2

[8]

- c) Show that the output current  $I$  of a simple BJT current mirror comprising two matched transistors is related to the input current  $I_{REF}$  by the following equation:

$$I = \frac{I_{REF}}{1 + 2/\beta} \quad [4]$$

- d) Sketch circuits showing a Class B push-pull output stage and one possible configuration for a Class AB push-pull output stage. Explain briefly the advantages of the Class AB configuration. [10]

Question 1 continues on the next page...

**Question 1 continued:**

- e) Figure 1.3 shows an n-channel, depletion mode MOSFET connected as an active load. Sketch the I-V characteristic of this device for  $V \geq 0$ , and annotate your graph to identify clearly the triode and active regions.

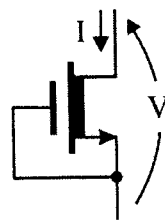


Figure 1.3

[5]

- f) Using the resistance reflection rule, or otherwise, determine the small-signal output resistance of the circuit in Figure 1.4.

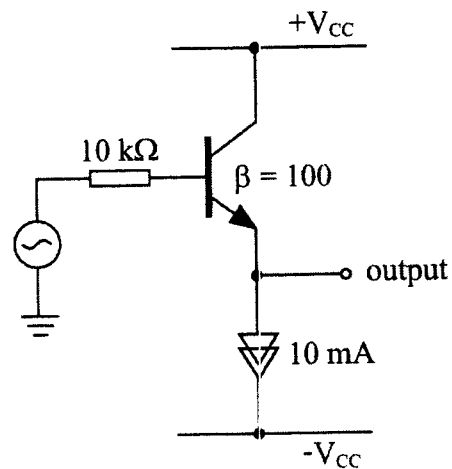


Figure 1.4

[7]

2. The signal  $v_s$  from a high-impedance source is to be amplified using a simple amplifier based on an n-channel enhancement mode MOSFET, as shown in Figure 2.1.

- a) Determine the quiescent values of the drain current and drain voltage, and show that the MOSFET is saturated under quiescent conditions. State clearly any assumptions made in your calculations. [10]
- b) Draw a small-signal equivalent circuit of the amplifier, and calculate its small-signal voltage gain. Also calculate the small-signal input resistance of the amplifier, taking into account the bias resistors, and hence determine the overall in-circuit voltage gain  $v_{out}/v_s$  in the mid-band i.e. at frequencies for which the coupling capacitor  $C$  is effectively short-circuit. [15]
- c) By what ratio would the gain  $v_{out}/v_s$  be increased if the  $10\text{ k}\Omega$  resistor were replaced by a depletion type active load with an Early voltage of  $80\text{ V}$ , assuming the same quiescent current? [5]

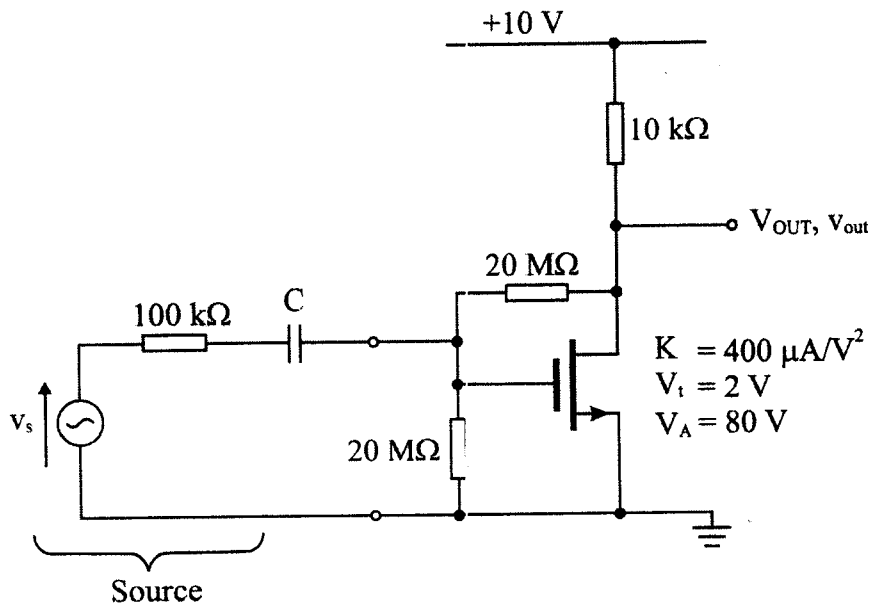


Figure 2.1

3. This question relates to the Wilson current mirror shown in Figure 3.1. You may assume that the three transistors are matched.

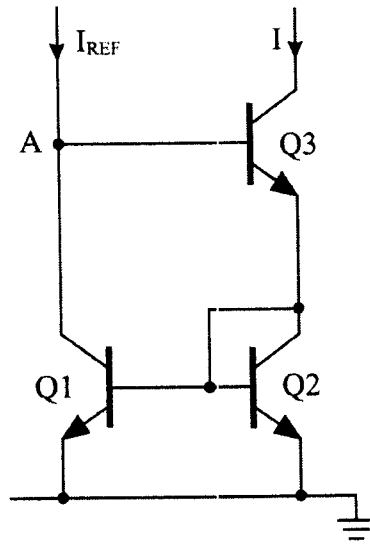
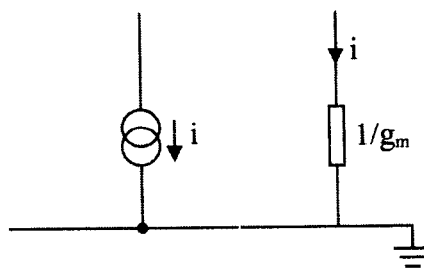


Figure 3.1

- a) By applying Kirchhoff's current law at node A, and making use of the fact that Q1 and Q2 form a simple BJT current mirror, show that the currents I and I<sub>REF</sub> are related as follows:

$$\frac{I_{REF}}{I} = \left( 1 + \frac{2}{\beta(\beta + 2)} \right) \approx 1 + 2/\beta^2 \quad [10]$$

- b) Draw a small-signal equivalent circuit (SSEC) of the simple BJT current mirror formed by Q1 and Q2, and show that, by assuming  $r_{be} \gg 1/g_m$  and neglecting output resistances, it can be reduced to the following approximate form:



[10]

- c) Draw a small-signal equivalent circuit of the complete Wilson current mirror, including the output resistance of Q3, but using the SSEC given in part b) to represent Q1 and Q2. By applying a test signal to the output terminal, or otherwise, show that the small-signal output resistance  $R_o$  of the circuit you have drawn is:

$$R_o = \left[ 1 + \frac{1}{2} \left( \beta + \frac{1}{g_m r_o} \right) \right] r_o \approx \frac{1}{2} \beta r_o \quad [10]$$

4. Figure 4.1 shows a differential amplifier in which all four transistors are matched. You may neglect base currents in any large-signal calculations, and in parts a), b) and c) you may assume that the transistors have infinite output resistance.

a) Choose the value of R to give a tail current of  $I = 0.5 \text{ mA}$ . Assuming this value of R, what is the quiescent output voltage of the circuit when  $V_{IN1} = V_{IN2}$  and all transistors are active? [6]

b) Show that, provided none of the transistors enters saturation, the output voltage  $V_{OUT}$ , for arbitrary  $V_{IN1}$  and  $V_{IN2}$ , may be expressed as:

$$V_{OUT} = \frac{10}{1 + \exp(-40V_D)} \quad [10]$$

where  $V_D = V_{IN1} - V_{IN2}$  is the differential input voltage.

c) By evaluating  $d(V_{OUT})/dV_D$  at  $V_D = 0$ , or otherwise, determine the small-signal differential gain of the amplifier. Also calculate the differential input resistance for small signals if  $\beta = 200$ . [10]

d) What will be the common-mode rejection ratio of the amplifier if the transistors have an Early voltage of 100 V? You may neglect the output resistances of Q1 and Q2 when evaluating the common-mode gain. [4]

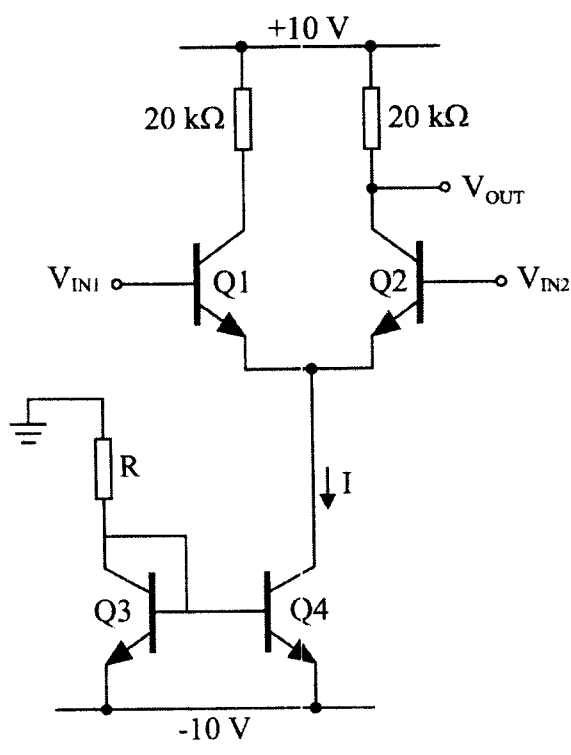


Figure 4.1

## 2005 E1.4 - Analogue Electronics 1 - Solutions.

1 (a) For  $I_c = 1\text{mA}$  require  $I_B = 1\text{mA}/100 = 10\ \mu\text{A}$

$$I_B = \frac{V_C - V_B}{R_B} \Rightarrow R_B = \frac{5 - 0.7}{10^{-5}} = \underline{\underline{430\ \text{k}\Omega}}$$

$$R_c \text{ carries emitter current} \Rightarrow R_c = \frac{10 - 5}{1\text{mA}} \times \frac{100}{101} = \underline{\underline{4.95\ \text{k}\Omega}}$$

Assumed  $V_{ce} = 0.7\ \text{V}$

[6]

(b)  $V_S = I_D R_S \dots \textcircled{1}$  and  $V_D = 5 - I_D R_D \dots \textcircled{2}$

and, assuming FET is active,  $I_D = K(V_{GS} - V_t)^2 = K(2 - V_S)^2 \dots \textcircled{3}$

Eliminating  $I_D$  from  $\textcircled{1}$  &  $\textcircled{3} \Rightarrow V_S = R_S K (2 - V_S)^2$

$$R_S K = 6\ \text{V} \Rightarrow 6V_S^2 - 25V_S + 24 = 0$$

$$\Rightarrow V_S = \frac{25 \pm 7}{12} = \cancel{2.67} \text{ or } 1.5$$

(sub threshold)

From  $\textcircled{1}, \textcircled{2}$   $I_D = V_S / R_S = \underline{\underline{75\ \mu\text{A}}}$  and  $V_D = 5 - 1.5 = \underline{\underline{3.5\ \text{V}}}$

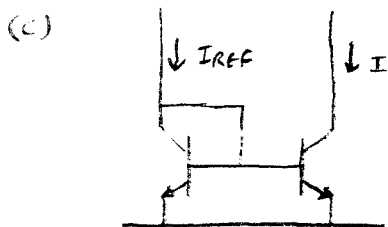
Check mode:  $V_{DS} = 3.5 - 1.5 = 2$ ,  $V_{GS} - V_t = -1.5 - -2 = +0.5$

$\Rightarrow$  ACTIVE assumption was correct.

Min supply voltage is when  $V_{DS} = 0.5\ \text{V}$ , in which case

$$V_{\text{supply}} = V_S + V_{DS} + I_D R_D = 1.5 + 0.5 + 1.5 = \underline{\underline{3.5\ \text{V}}}$$

[8]



$$I_{\text{REF}} = I_c + 2I_B \quad (\text{KCL at LHS})$$

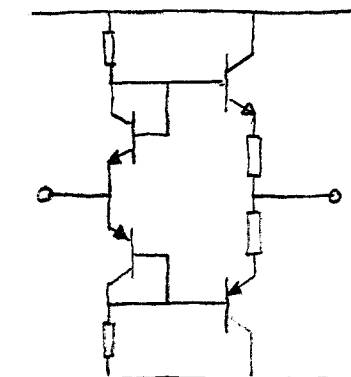
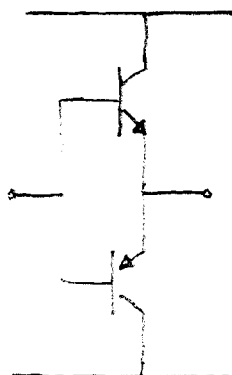
$$= I_c (1 + 2/\beta)$$

$$I = I_c = I_{\text{REF}} / (1 + 2/\beta)$$

[4]

(d) Class B:

Class AB: (one possible soln)

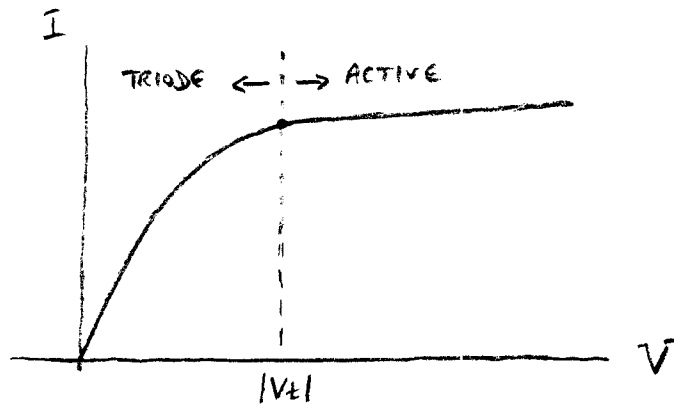


Cont'd...

1 (d) cont'd Main advantage of class AB over class B is that cross-over distortion is much lower because at least one o/p transistor is conducting at all times. Advantage over class A is lower power consumption

[10]

(e)



[5]

(f) using resistance reflection rule :

$$R_o = \frac{R_s + r_{\pi}}{(1+\beta)} = \frac{R_s}{(1+\beta)} + r_e$$

where  $R_s$  = source resistance =  $10 \text{ k}\Omega$

$$r_e = \text{emitter resistance} = \frac{V_T}{I_E} = \frac{25 \text{ mV}}{10 \text{ mA}} = 2.5 \Omega$$

$$\Rightarrow R_o = \frac{10 \text{ k}}{101} + 2.5 = \underline{\underline{101.5 \Omega}}$$

[7]



2 (a)  $I_G = 0 \Rightarrow$  Bias network imposes constraint  $V_G = V_D/2$   
 Know that  $V_G > V_t$  (since, if FET were not conducting,  $V_G$  would be +5V which would not be self-consistent)  
 and  $V_D = 2V_G > V_G - V_t \Rightarrow$  FET is ACTIVE

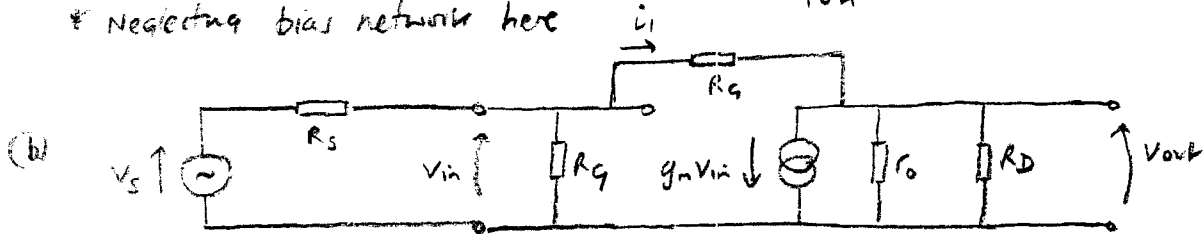
\*  $I_D$  satisfies:  $I_D = \frac{+10 - V_D}{R_D} = K \left( \frac{V_D}{2} - V_t \right)^2$

$K R_D = 4V \Rightarrow V_D^2 - 7V_D + 6 = 0, V_D = 1$  or  $V_D = 6$

$I_D = \frac{10 - 6}{10k} = \underline{\underline{0.4 \text{ mA}}}$

[10]

\* Neglecting bias network here



KCL @ o/p  $\Rightarrow g_m v_{in} + \frac{v_{out}}{r_o} + \frac{v_{out}}{R_D} + \frac{v_{out} - v_{in}}{R_g} = 0$

$\Rightarrow A_v = \frac{v_{out}}{v_{in}} = -\left(g_m - \frac{1}{R_g}\right) \cdot (r_o \parallel R_D \parallel R_g)$

$g_m = 2\sqrt{K I_D} = 0.8 \text{ mA/V}, r_o = \frac{V_A}{I_D} = 200 \text{ k}\Omega$

$R_D = 10 \text{ k}\Omega, R_g = 20 \text{ M}\Omega \Rightarrow A_v = \underline{\underline{-7.61}}$

$i_i = \frac{v_{in} - v_{out}}{R_g} = \frac{v_{in}(1 - A_v)}{R_g} \Rightarrow v_{in}/i_i = R_g / (1 - A_v)$   
 and  $R_{in} = R_g \parallel [R_g / (1 - A_v)] = \underline{\underline{2.08 \text{ M}\Omega}}$

Overall gain:  $\frac{v_{out}}{V_s} = A_v \times \frac{R_{in}}{R_{in} + R_s} = \underline{\underline{-7.26}}$

[15]

(c) With active load  $R_D \rightarrow V_A / I_D = 200 \text{ k}\Omega$

$\Rightarrow A_v \rightarrow -\left(g_m - \frac{1}{R_g}\right) (r_o/2 \parallel R_g) = -79.6$

$R_{in} \rightarrow 248 \text{ k}\Omega$

overall gain  $\frac{v_{out}}{V_s} \rightarrow A_v \times \frac{R_{in}}{R_{in} + R_s} = -56.7$

[5]

Ratio =  $\frac{56.7}{7.26} = 7.8$

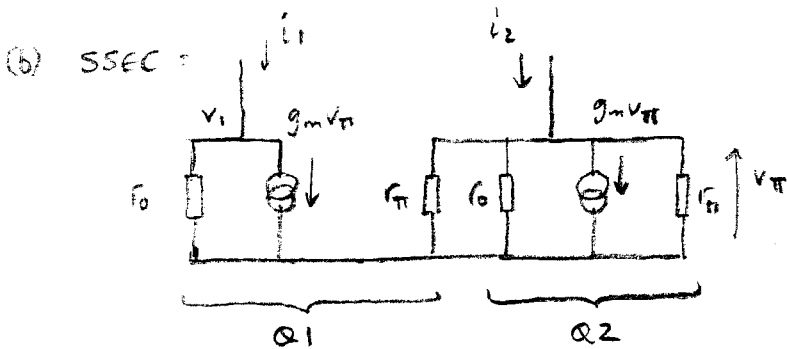
3 (a) KCL at A:  $I_{REF} = I_{B3} + I_{c1} = \frac{I}{\beta} + I_{c1} \dots \textcircled{1}$

Q1, Q2 form CM  $\Rightarrow I_{c1} = \frac{I_{E3}}{1 + 2/\beta} = \frac{I}{\alpha} \cdot \frac{1}{(1 + 2/\beta)} \dots \textcircled{2}$

$\textcircled{1}$  in  $\textcircled{2} \Rightarrow \frac{I_{REF}}{I} = \frac{1}{\beta} + \frac{(\beta+1)}{\beta} \cdot \frac{1}{1 + 2/\beta}$

$$= \frac{(2+\beta) + \beta(\beta+1)}{\beta(2+\beta)} = \frac{\beta^2 + 2\beta + 2}{\beta(2+\beta)}$$

$$= 1 + \frac{2}{\beta(\beta+2)} \approx 1 + 2/\beta^2 \quad \text{since } \beta \gg 1 \quad [10]$$



KCL @ RHS:

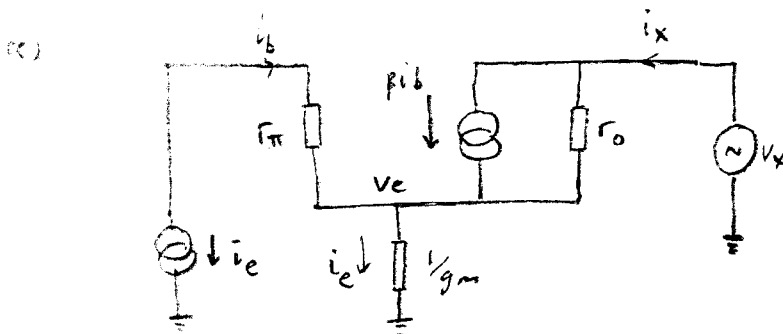
$$i_2 = 2\frac{v_{\pi}}{r_{\pi}} + \frac{v_{\pi}}{r_o} + g_m v_{\pi}$$

$$\frac{v_{\pi}}{i_2} = \left( \frac{r_{\pi}}{2} \parallel r_o \parallel \frac{1}{g_m} \right)$$

if  $\frac{1}{g_m} \ll r_{\pi}$ , and  $r_o$  neglected then  $v_{\pi} = \left(\frac{1}{g_m}\right) i_2$   
and RHS can be approximated as resistor  $1/g_m$

KCL @ LHS:  $i_1 = g_m v_{\pi} + \frac{v_i}{r_o} \approx g_m v_{\pi}$

$$= g_m v_{\pi} \approx g_m \cdot \left(\frac{1}{g_m}\right) i_2 = i_2 \quad [10]$$



KCL for Q3:

$$i_b + i_x = i_e$$

$$\text{and } i_b = -i_e$$

$$\Rightarrow i_x = 2i_e \dots \textcircled{1}$$

KCL @ o/p:  $i_x = \frac{v_x - v_e}{r_o} + \beta i_b = \frac{v_x}{r_o} - \frac{i_e}{g_m r_o} - \beta i_e \dots \textcircled{2}$

$\textcircled{1} \rightarrow \textcircled{2} \Rightarrow i_x \left[ 1 + \frac{1}{2} \left[ \beta + \frac{1}{g_m r_o} \right] \right] = \frac{v_x}{r_o}$

$$= \frac{v_x}{r_o} \cdot r_o = r_o \left[ 1 + \frac{\beta}{2} + \frac{1}{2g_m r_o} \right] \approx \frac{r_o \beta}{2} \quad [10]$$

since  $\beta \gg 1$  and  $g_m r_o \gg 1$

4 (a) Assuming ideal current mirror  $I = (0 - V_{B3})/R$

$V_{B3} \approx -9.3V$ , so for  $I = 0.5mA$  require  $R = \underline{\underline{18.6k\Omega}}$   
 when  $V_{in1} = V_{in2}$ ,  $I_{C1} = I_{C2} = I/2 = 0.25mA$

$$V_{out} = +10 - I_{C2} \times 20k = \underline{\underline{+5V}} \quad [6]$$

(b) Large signal eqns for  $Q1$  &  $Q2$  ( $L \rightarrow R$ ) are:

$$I_{C1} = I_S \exp\left(\frac{V_{in1} - V_E}{V_T}\right) \dots \textcircled{1} \quad I_{C2} = I_S \exp\left(\frac{V_{in2} - V_E}{V_T}\right) \dots \textcircled{2}$$

where  $V_E =$  (common) emitter voltage of  $Q1/Q2$

$$\textcircled{1}/\textcircled{2} \Rightarrow I_{C1}/I_{C2} = \exp(V_D/V_T) \dots \textcircled{3}$$

$$\text{KCL at common emitter: } I_{C1} + I_{C2} = I \dots \textcircled{4}$$

$$\textcircled{3} + \textcircled{4} \Rightarrow I_{C2} [1 + \exp(V_D/V_T)] = I$$

$$V_{out} = V_{CC} - I_{C2} R_C = V_{CC} - \frac{I R_C}{1 + \exp(V_D/V_T)}$$

$$V_{CC} = 10V, I R_C = 10V$$

$$\Rightarrow V_{out} = 10 \left[ 1 - \frac{1}{1 + \exp(V_D/V_T)} \right] = \frac{10}{1 + \exp(-40V_D)}$$

$$\text{since } V_T = \frac{1}{40} V \quad [10]$$

(c) From given equation  $\frac{dV_{out}}{dV_{in}} = \frac{-10}{[1 + \exp(-40V_D)]^2} \cdot -40 \exp(-40V_D)$

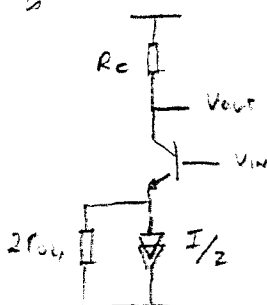
Evaluating at  $V_D = 0 \Rightarrow A_v = \underline{\underline{+100}}$

Differential i/p resistance is  $R_i = 2r_{be} = \frac{2\beta}{g_m} = \frac{2\beta V_T}{I_c}$

where  $I_c = 0.25mA$

$$\Rightarrow R_i = \underline{\underline{40k\Omega}} \quad [10]$$

(d) Common mode gain depends on current mirror v/p resistance  $r_{o4}$  &  $r_{o5}$  for this ckt (C.E. amp  $\bar{R}_E$ )



$$A_{cm} \approx -\frac{R_C}{2r_{o4}} = -\frac{R_C I}{2V_A} = -\frac{R_C I_c}{V_A} = -0.05$$

$$\Rightarrow CMRR = \frac{100}{0.05} = 2000 \quad [4] \\ [= 66dB]$$