IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2003

ANALOGUE ELECTRONICS 1

Corrected Copy

Monday, 2 June 10:00 am

Time allowed: 2:00 hours

There are FIVE questions on this paper.

Answer THREE questions.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : A.S. Holmes
Second Marker(s) : M.K. Gurcan

1. (a) For the amplifier in Figure 1a, choose values of R_B and R_C to give a collector bias current of 0.5 mA and a quiescent output voltage of 5 V. State clearly any assumptions you make. [6]

(b) Draw a small-signal equivalent circuit for the amplifier in Figure 1a, and determine the small-signal macromodel parameters (input resistance, output resistance and voltage gain) assuming the resistor values are as you calculated above. [8]

(c) An amplifier similar to that in Figure 1a, with the resistor values you calculated above, is inserted between a signal source and a load as shown in Figure 1b. Determine the overall voltage gain v_L/v_S for this arrangement in the mid-band, and draw a dimensioned sketch showing the variation of $|v_L/v_S|$ with frequency over the range 10 Hz to 10 kHz. [6]

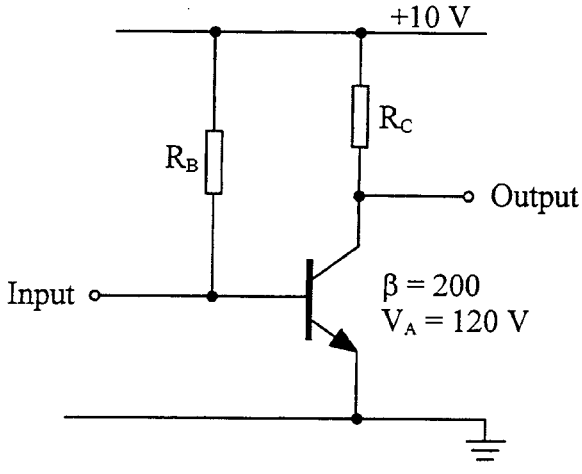

Figure 1a

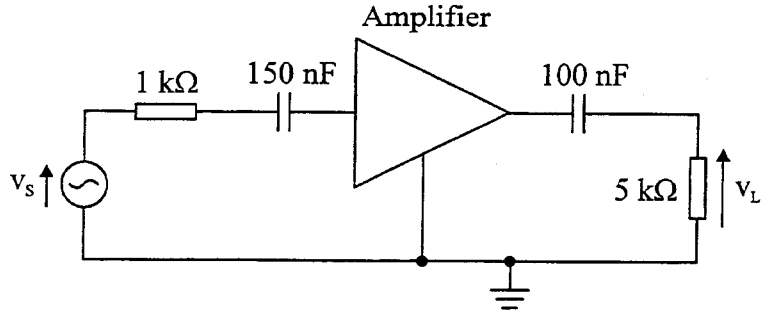

Figure 1b

2. Figure 2 shows an NMOS amplifier employing two enhancement mode MOSFETs.

(a) Neglecting any current in the bias resistors, and assuming both MOSFETs are saturated, show that the output voltage V_{OUT} may be expressed as:

$$V_{OUT} = V_{DD} - V_{t2} - \sqrt{\frac{K_1}{K_2}} \cdot (V_{G1} - V_{t1})$$

where V_{G1} is the gate voltage of Q1. [6]

(b) By considering the constraint imposed on V_{OUT} and V_{G1} by the bias network, calculate the quiescent output voltage and the quiescent drain current in each MOSFET. Also confirm that both MOSFETs are indeed saturated under quiescent conditions. What is the minimum supply voltage at which the amplifier could be operated? [8]

(c) Using the equation in part (a), or otherwise, determine the voltage gain of the amplifier at signal frequencies for which the input capacitor is effectively short-circuit. [6]

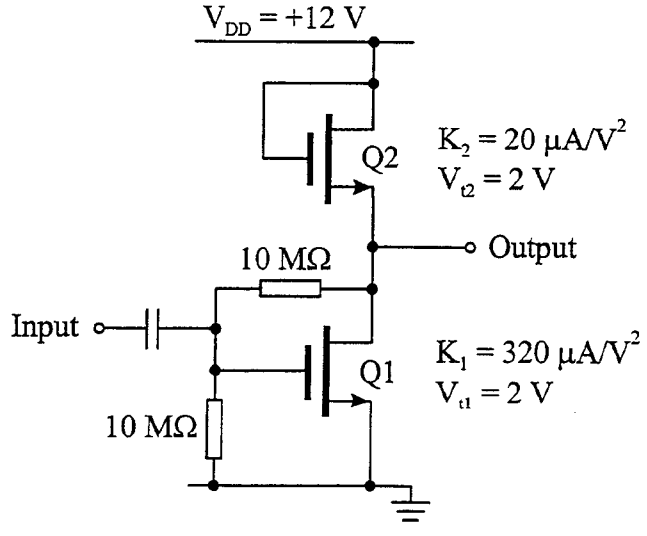

Figure 2

3. This question relates to the Widlar current sink shown in Figure 3.

(a) Assuming the two transistors are matched, and ignoring base currents, show that the currents I_{REF} and I are related as follows:

$$I = I_{REF} \exp\left(\frac{-IR_E}{V_T}\right)$$

where V_T is the thermal voltage. [6]

(b) Assuming that the base of Q2 is effectively held at signal ground by the diode-connected transistor Q1, draw a small-signal equivalent circuit (SSEC) of the right-hand side of the current sink.

By applying a test source to the output of your SSEC, or otherwise, show that the small-signal output resistance of the circuit is:

$$R_o = r_o[1 + g_m R'_E] + R'_E$$

where R'_E is the parallel combination of R_E and r_{be}, and the small-signal parameters g_m, r_{be} and r_o all refer to Q2. [10]

(c) What advantages does the Widlar circuit offer over a simple current mirror? Use the results in parts (a) and (b) to illustrate your answer. [4]

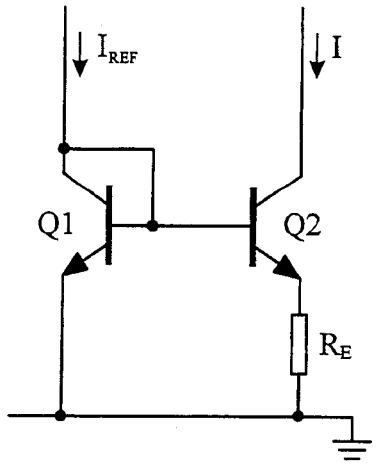

Figure 3

4. (a) Sketch a circuit diagram for a class B push-pull output stage. What are the main drawbacks of this configuration as a voltage follower? [6]

(b) It is proposed that the class AB configuration shown in Figure 4 be used as the output stage of an operational amplifier. The transistors Q1-Q4 are matched, with saturation currents of 3×10^{-14} A and β values of 200.

Explain why all four transistors necessarily have the same collector bias current when Vin = 0, and calculate the value of this current. State any simplifying assumptions you make. [6]

(c) Making use of the large-signal equation $I_C = I_S \exp(V_{BE}/V_T)$, calculate values for the base voltage of Q3 and the input voltage Vin when the class AB output stage is delivering +10 V into a 100 Ω load. In this calculation you should assume that Q4 is carrying negligible load current. By also calculating the base voltage of Q4, show that the above assumption is justified. [8]

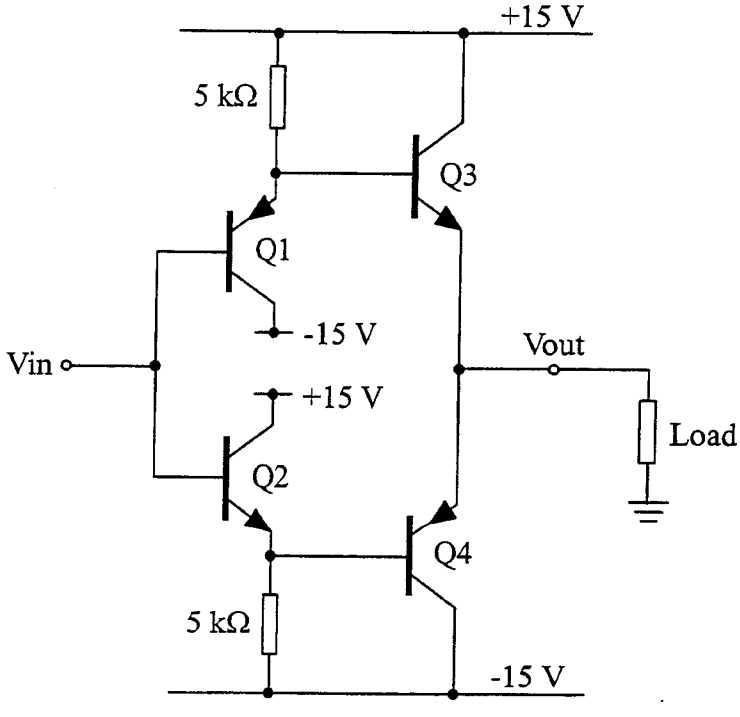

Figure 4

5. Figure 5 shows the circuit of a classic astable multivibrator, modified only by the addition of an ENABLE input to allow oscillations to be started and stopped. The ENABLE input is assumed to be either high (5 V) or low (0 V).

(a) Explain qualitatively the operation of the circuit when the enable input is high. It may help you to include in your answer a sketch showing the time variations of the base and collector voltages of the two transistors. [8]

(b) Assuming R >> 1 kΩ, show that the period T of the free-running oscillations is given approximately by:

$$T = 2\tau \ln\left(\frac{2V_{CC} - V_{BE} - V_{CEsat}}{V_{CC} - V_{BE}}\right)$$

where V_{BE} and V_{CEsat} have their usual meanings, and τ = RC. Hence choose reasonable values for R and C to give an oscillation frequency of 10 kHz, assuming the transistors have $\beta = 100$, [8]

(c) If the ENABLE input makes a low-to-high transition after being low for a long time, roughly how long after ENABLE goes high will the first transition in the outputs occur? [4]

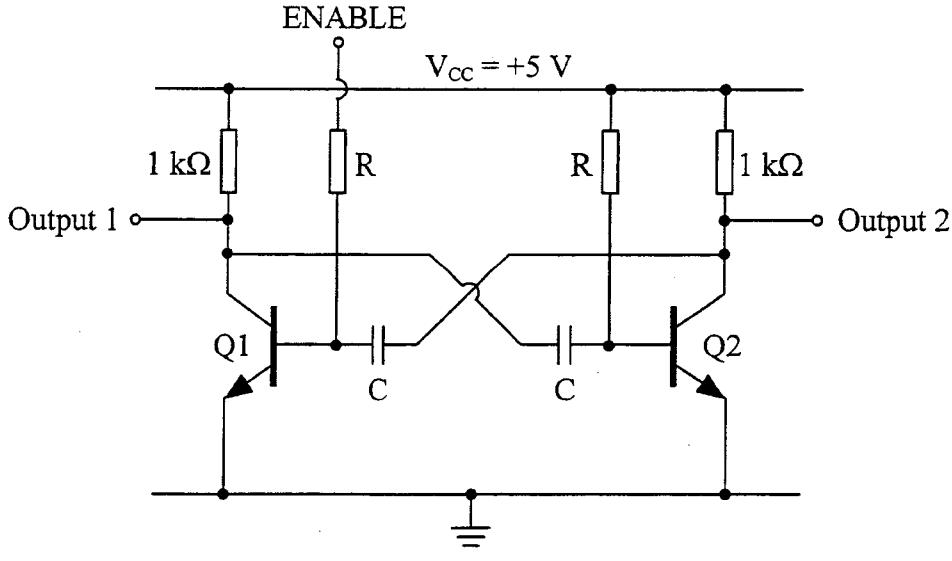

Figure 5

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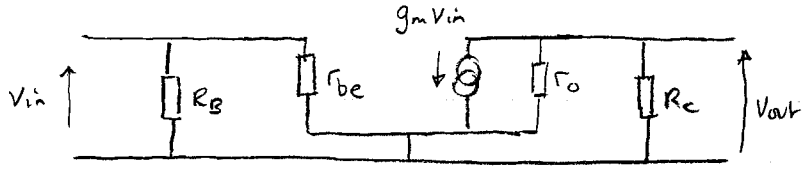
1 (a) $I_C = 0.5\,mA \Rightarrow I_B = \frac{0.5}{200}\,mA = 2.5\,\mu A = \frac{10 - 0.7}{R_B}$

$\Rightarrow \underline{\underline{R_B = 3.72\,M\Omega}}$

$V_{OUT} = 5V = 10 - I_C R_C \Rightarrow \underline{\underline{R_C = 5V/0.5mA = 10k\Omega}}$

Assumed $V_{BE} = 0.7\,V$ [6]

(b) SSEC :



$g_m = \frac{I_c}{V_T} = 0.02\,S$

$r_{be} = \beta/g_m = 10k\Omega$

$r_o = \frac{V_A}{I_c} = 240k\Omega$

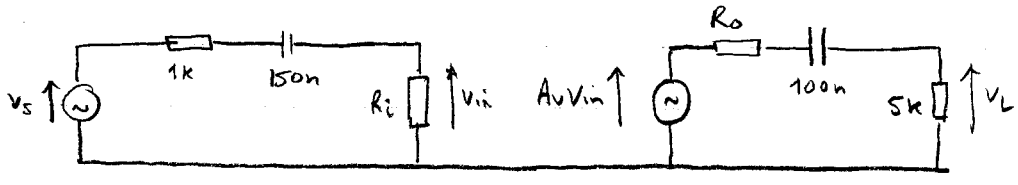
Macromodel parameters :

$R_i = R_B \,||\, r_{be} = 3.72M \,||\, 10k = \underline{\underline{9.97\,k\Omega}}$

$R_o = r_o \,||\, R_c = 240k \,||\, 10k = \underline{\underline{9.6\,k\Omega}}$

$A_v = \frac{V_{out}}{V_{in}} = -g_m R_o = -0.02 \times 9.6k = \underline{\underline{-192}}$ [8]

(c) Using macromodel, overall SSEC is :



Overall gain in mid-band (100n caps short-cct) is :

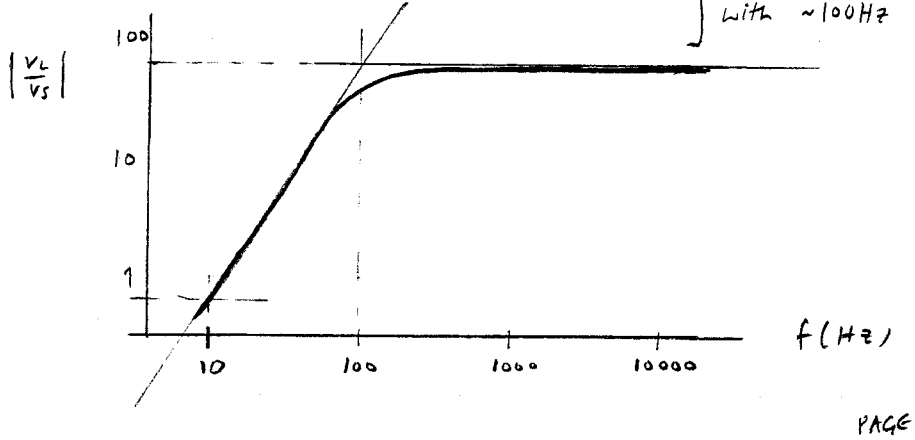
$\frac{V_L}{V_S} = \left(\frac{5k}{5k + 9.6k}\right) \times (-192) \times \left(\frac{9.97k}{9.97k + 1k}\right) = \underline{\underline{-59.8}}$

Cut-off frequencies for I/P and O/P RC networks are :

$f_{ci} = [2\pi \times 10.97k \times 150n]^{-1} = 97\,Hz$

$f_{co} = [2\pi \times 15k \times 100n]^{-1} = 106\,Hz$

} combined effect is 2nd order HP filter with ~100Hz cut-off



[6]

2 (a) For Q1 : $I_{D1} = K_1 (V_{G1} - V_{t1})^2$ ... ①

For Q2 : $I_{D2} = K_2 (V_{DD} - V_{OUT} - V_{t2})^2$ ... ②

Assuming current in bias network is negligible, $I_{D1} = I_{D2}$

$$\therefore \quad K_1 (V_{G1} - V_{t1})^2 = K_2 (V_{DD} - V_{OUT} - V_{t2})^2$$

and taking $\sqrt{\ }$ gives

$$\pm \sqrt{K_1/K_2}\,(V_{G1} - V_{t1}) = V_{DD} - V_{OUT} - V_{t2}$$

Negative root can be neglected, as it would put one of the FETs below threshold

$$\Rightarrow \quad \underline{\underline{V_{OUT} = V_{DD} - V_{t2} - \sqrt{\frac{K_1}{K_2}}\,(V_{G1} - V_{t1})}} \qquad [6]$$

(b) Bias network imposes constraint $V_{OUT} = 2 V_{G1}$ under quiescent conditions. We can use this to eliminate V_{G1} from large sig equation, giving:

$$V_{OUT} = V_{DD} - V_{t2} - \sqrt{\frac{K_1}{K_2}}\left(\frac{V_{OUT}}{2} - V_{t1}\right)$$

$$\text{or} \quad V_{OUT} = \frac{V_{DD} - V_{t2} + \sqrt{\frac{K_1}{K_2}}\,V_{t1}}{1 + \frac{1}{2}\sqrt{K_1/K_2}}$$

$V_{DD} = 12$, $V_{t1} = V_{t2} = 2$, $\sqrt{K_1/K_2} = 4$

$$\Rightarrow \quad V_{OUT} = (12 - 2 + 8)/3 = \underline{\underline{6\,V}}$$

From ②, $I_D = 20\mu \times (12 - 6 - 2)^2 = \underline{\underline{320\,\mu A}}$

Check modes: both conducting with $V_{DS} > V_{GS} - V_t$

$\Rightarrow$ <u>both saturated</u>

Min V_{DD}: provided both FETs remain above threshold, amplifier will work

$V_{GS1} = V_{OUT}/2 \Rightarrow$ require $V_{OUT} > 4\,V$

$V_{GS2} = V_{DD} - V_{OUT} \Rightarrow$ require $V_{DD} > V_{OUT} + 2\,V$

$$\Rightarrow \quad \underline{\underline{V_{DD\,min} = 6\,V}} \qquad [8]$$

(c) Easiest method is simply to differentiate large signal equation:

$$A_v = \frac{\partial V_{OUT}}{\partial V_{G1}} = -\sqrt{\frac{K_1}{K_2}} = \underline{\underline{-4}} \qquad [6]$$

3 (a) For Q1 : $I_{REF} = I_S \exp\left(V_{BE1}/V_T\right)$ ... ①

For Q2 : $I = I_S \exp\left(V_{BE2}/V_T\right)$ ... ②

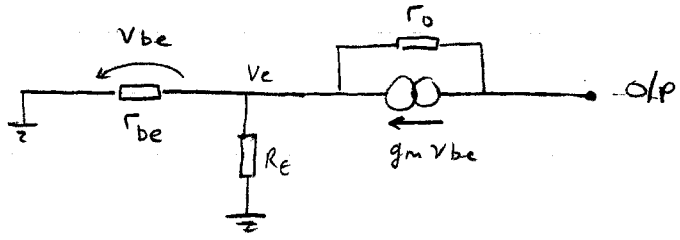
②/① $\Rightarrow$ $I = I_{REF} \exp\left(\frac{V_{BE2} - V_{BE1}}{V_T}\right)$ ... ③

But KVL gives

$V_{BE1} = V_{BE2} + I R_E$ ... ④

④ in ③ $\Rightarrow$ $I = I_{REF} \exp\left(-\frac{I R_E}{V_T}\right)$ ⑤ [6]

(b) With base of Q2 at signal ground, SSEC of RHS is :



Applying a test source V_x to o/p, current i_x into o/p terminal is :

$$i_x = \frac{V_x - V_e}{r_o} + g_m v_{be} \quad ⑥$$

But, we also have $v_{be} = -v_e$ ... ⑦

and $v_e = i_x R'_E$ ... ⑧

⑦, ⑧ into ⑥ gives :

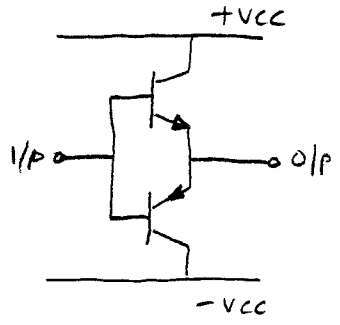
$$i_x \left[1 + \left(g_m + \frac{1}{r_o}\right) R'_E \right] = \frac{V_x}{r_o}$$

and $R_o = \frac{V_x}{i_x} = r_o + (g_m r_o + 1) R_E'$

$= r_o \left[1 + g_m R'_E \right] + R_E'$ ⑨ [10]

(c) Exponential term in ⑤ can be made $\ll 1$, allowing small o/p current to be derived from larger reference current w/o requiring large resistor values. From ⑨, $R_o > r_o$, so Widlar has higher o/p resistance than simple current mirror $\Rightarrow$ better performance as current source. [4]

4 (a) Class B :



Drawbacks : ○ O/p is offset by $\pm V_{BE}$ wrt I/p

○ Transistors both off when $|V_{IN}| \lesssim 0.6\,V$

$\Rightarrow$ cross-over distortion [6]

(b) Because of cct symmetry and transistor matching, we can say that $V_{out} = 0$ when $V_{in} = 0$.

It follows that all four transistors have the same V_{BE}, and hence the same I_C.

Ignoring base currents, I_{C1} is equal to the current in the upper 5kΩ resistor. Assuming $V_{BE1} \sim 0.7\,V$, this gives

$$I_C \sim \frac{15 - 0.7}{5k} = \underline{\underline{2.86\ mA}} \qquad [6]$$

(c) when $V_{out} = +10\,V$ with 100Ω load, $I_{E3} \sim 100\,mA$

$$\Rightarrow I_{B3} = \frac{I_{E3}}{1+\beta} = 0.5\,mA \quad \text{and} \quad V_{BE3} = V_T \ln\left(\frac{I_{C3}}{I_S}\right) = 721\,mV$$

$$\text{So} \quad V_{B3} = 10 + 0.721 = \underline{\underline{10.721\ V}}$$

$$I_{E1} = \frac{15 - 10.721}{5k} - I_{B3} = 0.356\ mA$$

$$\text{and} \quad V_{BE1} = -V_T \ln\left(\frac{I_{C1}}{I_S}\right) = -580\,mV$$

$$\Rightarrow V_{in} = V_{B3} + V_{BE1} = 10.721 - 0.58 = \underline{\underline{10.141\ V}}$$

Ignoring the base current of Q_4, the emitter current of Q_2 is approx $I_{E2} \sim \frac{(10.141 - 0.7) - (-15)}{5k} = 4.89\,mA$

From this, we can get a good estimate of $V_{BE2} \sim V_T \ln\left(\frac{I_{C2}}{I_S}\right) = 645\,mV$

$$\Rightarrow V_{B4} \sim 10.141 - 0.645 = \underline{\underline{9.496\ V}}$$

$$\Rightarrow V_{BE4} = 9.496 - 10 = -504\,mV \Rightarrow I_{C4} \sim 0.02\,mA \text{ (i.e. SMALL)} \qquad [8]$$

5 (a) Start by assuming:

(1) Q1 is being held ON (in saturation) via its base resistor

(2) Q2 is OFF because $V_{B2} < \sim 0.6V$

Under these conditions, V_{B2} will rise as the RH capacitor charges via Q2's base resistor. At some point, V_{B2} will reach $\sim 0.6V$, and Q2 will turn ON. This will cause V_{C2} to fall from V_{CC} to V_{CEsat}. Because the voltage across the LH capacitor cannot change instantaneously, V_{B1} will simultaneously fall to $[V_{CEsat} - (V_{CC} - V_{BE})]$, cutting Q1 OFF. This represents the end of one half-cycle; the next half-cycle is similar but with Q2 ON and Q1 OFF. ⇒ oscillator [8]

(b) Making $R \gg 1k$ ensures that the collector voltage of whichever Q is OFF reaches V_{CC} during the half-cycle. In this case, the initial base voltage on the other Q at the start of next half-cycle will be:

$$V_{Bi} = V_{CEsat} - (V_{CC} - V_{BE})$$

The final (asymptotic) base voltage on this Q in the absence of diode clamping would be $V_{Bf} = V_{CC}$. However, the Q turns on when $V_B \sim V_{BE}$. Standard result for RC transient gives:

$$V_{BE} = V_{CC} + \left[(V_{CEsat} + V_{BE} - V_{CC}) - V_{CC}\right] e^{-T/2\tau}$$

$$\Rightarrow \quad T = 2\tau \ln\left[\frac{2V_{CC} - V_{BE} - V_{CEsat}}{V_{CC} - V_{BE}}\right] \sim 1.5\tau \quad \text{when } V_{CC} = 5V,\ V_{BE} \sim 0.7V,\ V_{CEsat} \sim 0.2V$$

For 10 kHz operation require $T = 100\,\mu sec \Rightarrow \tau \sim 66.7\,\mu sec$

Suitable R to ensure Q's are driven well into saturation would be $R = \beta \times 1k/5 = \underline{\underline{20k\Omega}} \Rightarrow C = \frac{\tau}{R} = \underline{\underline{3.3\,nF}}$ [8]

(c) After a long time with $V_{ENABLE} = 0V$, $V_{B1} \to 0V$ (⇒ Q1 OFF; Q2 ON)

Delay to 1st o/p transition is time for V_{B1} to go from 0V to $\sim V_{BE}$

$$\Rightarrow \quad V_{BE} = V_{CC} + [0 - V_{CC}]e^{-t/\tau} \Rightarrow t = \tau \ln\left[\frac{V_{CC}}{V_{CC} - V_{BE}}\right] \sim \underline{\underline{10\,\mu sec}}$$ [4]