Paper Number(s): **E1.4**
ISE1.9

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2001

EEE/ISE PART I: M.Eng., B.Eng. and ACGI

ANALOGUE ELECTRONICS I

Monday, 11 June 10:00 am

There are FIVE questions on this paper.

Answer THREE questions.

Time allowed: 2:00 hours

CORRECTED

Examiners: Holmes,A.S. and Vickery,J.C.

1. For each of the four circuits in Figure 1 below, determine the operating modes of the transistor(s), and calculate the value of the current I or voltage V. State clearly any assumptions made in your calculations.

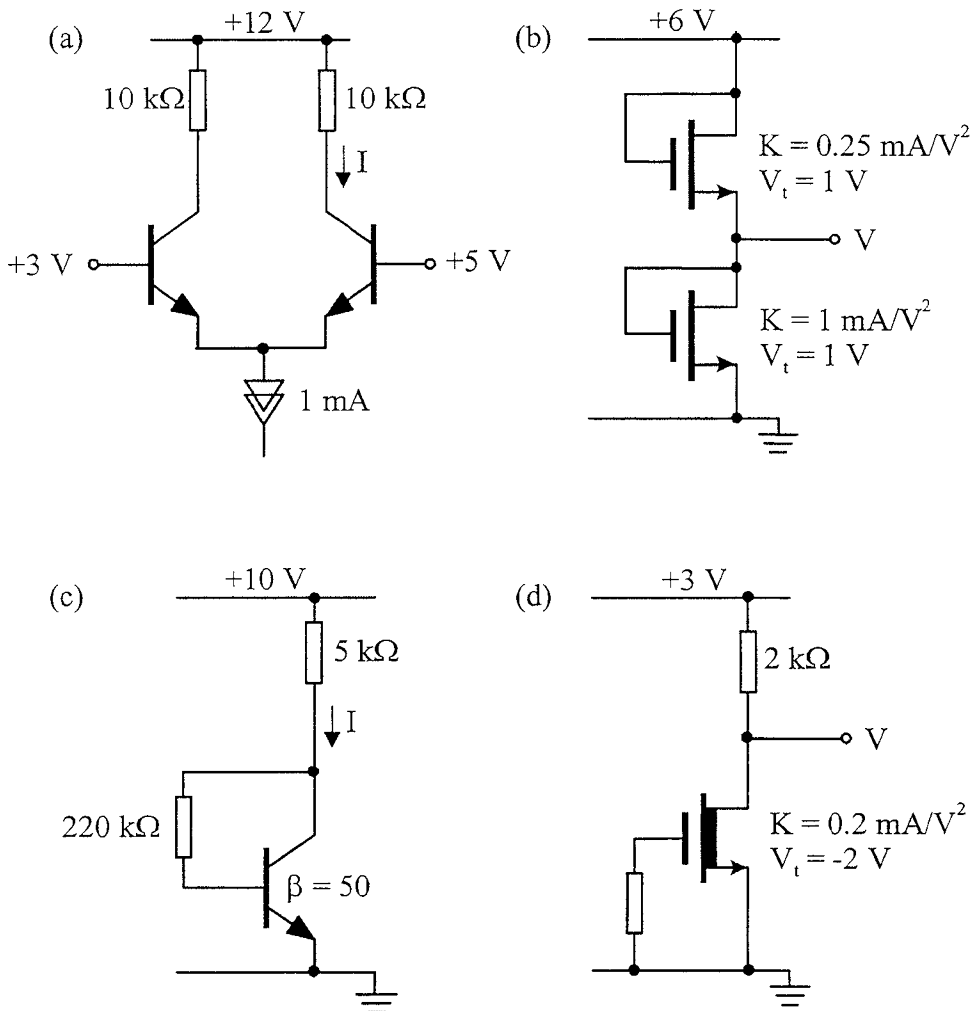


Figure 1

The four parts carry, respectively, 6, 5, 4 and 5 marks.

2. Figure 2a shows a common-emitter amplifier in which the transistor has a β value of 100 and an Early voltage of 120 V.

a) Determine the quiescent output voltage and the collector bias current, stating clearly any assumptions you make. Your calculation should take into account the base current of the transistor. [6]

b) Draw a small-signal equivalent circuit valid in the mid-band region, and determine the small-signal macromodel parameters i.e. input resistance, output resistance and voltage gain. [9]

c) Two amplifiers similar to that in Figure 2a are cascaded and inserted between a signal source and a load, as shown in Figure 2b. Determine the overall voltage gain v_L/v_S for this arrangement at frequencies for which all capacitors are effectively short-circuit. [5]

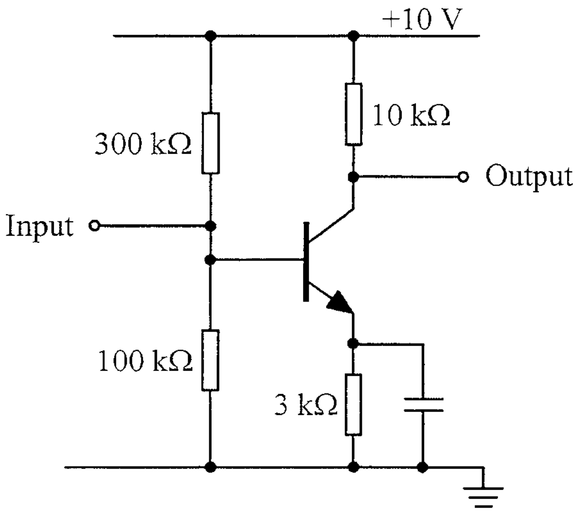


Figure 2a

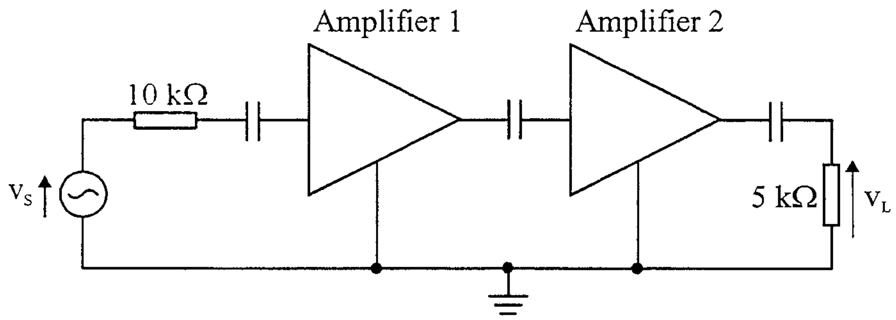


Figure 2b

3. Figure 3 shows an NMOS amplifier employing two enhancement mode MOSFETs.

a) Explain the role of the 10 MΩ resistor, and show that the quiescent output voltage may be expressed as:

$$V_{OUT} = \frac{V_{DD} - V_{t2} + V_{t1} \cdot \sqrt{K_1 / K_2}}{1 + \sqrt{K_1 / K_2}}$$

where the symbols K and V_t denote the usual MOSFET parameters, and the subscripts 1 and 2 refer to Q1 and Q2 respectively.

Evaluate V_{OUT} and determine the quiescent drain current in each MOSFET. [8]

b) Draw a small-signal equivalent circuit of the amplifier, and determine the small-signal voltage gain at frequencies for which the input capacitor is effectively short-circuit. Neglect the 10 MΩ resistor and the small-signal output resistances of the MOSFETs. [8]

c) If a sinusoidal input signal is applied to the amplifier, over what range of input amplitudes will both transistors remain active? Assume that the input capacitor has negligible impedance at the signal frequency. [4]

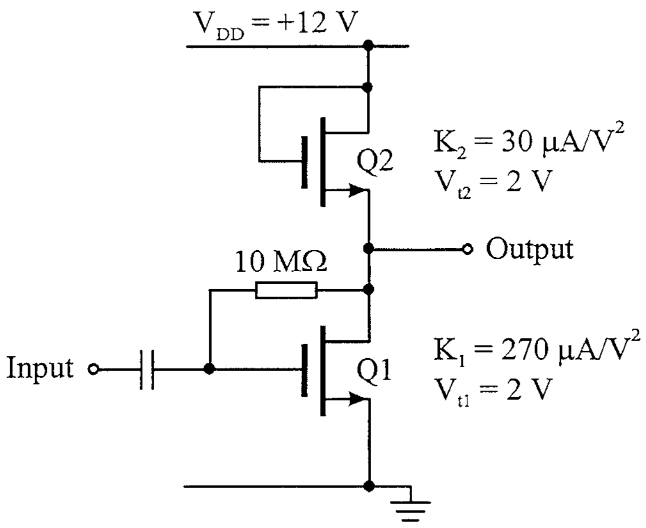


Figure 3

4. Figure 4 shows a variable-gain differential amplifier in which the gain can be adjusted by means of a control voltage V_C. All three transistors are matched and have $\beta = 100$.

a) Assuming all transistors are active, calculate the quiescent tail current I and the output voltage V_{OUT} when $V_C = 0$ and there is zero differential input voltage. Your calculation should include base currents. [6]

b) Draw a small-signal macromodel for the amplifier, expressing any bias-dependent parameters in terms of the tail current. You may neglect the small-signal output resistances of the transistors. [8]

c) Calculate the maximum and minimum values of the differential voltage gain as V_C is varied over the range –5 V to + 5V. Also determine the input common-mode voltage range for the two extreme values of V_C. [6]

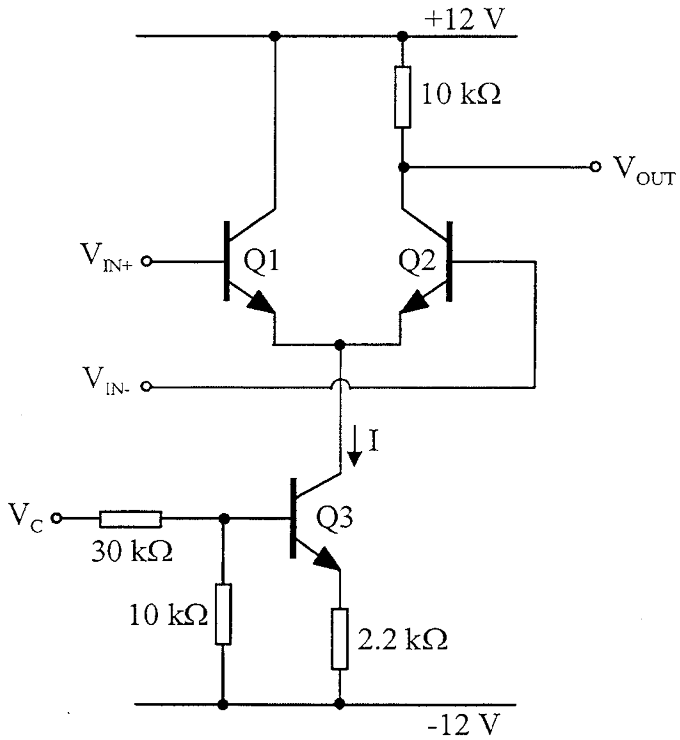


Figure 4

5. a) Show that, if a small-signal voltage source with output resistance R_S is connected to a load via a suitably biased emitter follower, the output resistance R_o of the source/follower combination is:

$$R_o = \frac{R_S + r_{be}}{1+\beta}$$

where β and r_{be} are the usual small-signal BJT parameters. [6]

b) The circuit in Figure 5 is to be used to derive a stable +5 V supply voltage from an unregulated supply of +15 V. The Zener diode has a small-signal resistance of 5 Ω when operated in its reverse breakdown region.

By evaluating the output resistance of the supply, calculate the change in output voltage when the load current I increases from 50 mA to 55 mA. [5]

If the unregulated +15 V supply has a ripple of 100 mV pk-pk amplitude, what is the amplitude of the corresponding ripple on the output voltage when the supply is driving a 100 Ω resistive load? [5]

Over what range of load currents can the supply be expected to maintain a stable output voltage? [4]

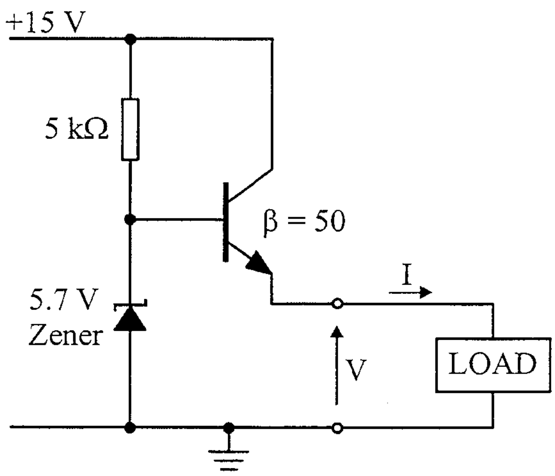


Figure 5

1 a) Large differential input voltage ⇒ one Q cut-off, other conducting

Emitter voltage $V_E \sim MAX(V_{IN1}, V_{IN2}) - 0.7 = 4.3V$

So, $V_{BE1} = -1.3V$ and <u>Q1 (LEFT) is CUT-OFF</u>

⇒ Q2 (RIGHT) carries all of tail current.

If Q2 active, then $V_{C2} = 12 - 1mA \times 10k = 2V < V_{B2}$

⇒ <u>Q2 is SATURATED</u> with $V_{C2} \sim V_E + 0.2 = 4.5V$

and $\underline{I = (12 - 4.5)/10k = 0.75\ mA}$

[6]

b) Both (enh. mode) MOSFETs have $V_{DS} = V_{GS}$, and $V_{DD} > V_{t1} + V_{t2}$

⇒ <u>BOTH MOSFETS are ACTIVE</u>

For Q1 (lower) have $I_D = K_1(V - V_{t1})^2$

For Q2 (upper) $I_D = K_2(V_{DD} - V - V_{t2})^2$

Equating drain currents ⇒ $K_1(V - V_{t1})^2 = K_2(V_{DD} - V - V_{t2})^2$

$\sqrt{\ }$ and rearrange to give $V = \dfrac{(V_{DD} - V_{t2})\sqrt{k_2/k_1} + V_{t1}}{1 + \sqrt{k_2/k_1}}$

[5]

$= \dfrac{5 \cdot \frac{1}{2} + 1}{1 + \frac{1}{2}} = 7/3$ $\quad \underline{V = 2.\dot{3}\ V}$

c) <u>Transistor is ACTIVE</u> ($V_c \leq 10V \Rightarrow I \geq 0 \Rightarrow I_B = \frac{I}{1+\beta} \geq 0 \Rightarrow V_c \geq V_B$)

$I_B = \dfrac{V_c - V_{BE}}{220k\Omega} = \dfrac{I}{(1+\beta)}$ --- ①, $\quad I = \dfrac{10 - V_c}{5k\Omega}$ --- ②

① into ② ⇒ $I = \dfrac{10 - \frac{220}{51}I - V_{BE}}{5}$ $\quad I = \dfrac{10 - 0.7}{5 + \frac{220}{51}} = \underline{1\ mA}$

[4]

d) $V_{GS} = 0$ $(I_G = 0)$ ⇒ if MOSFET active $I_D = K(V_t)^2 = 0.8mA$

But this would give $V_{DS} = 3 - 2 \times 0.8 = 1.4V < |V_{GS} - V_t| = 2V$

⇒ <u>MOSFET is in TRIODE region</u>

So, need to solve $I_D = K[2|V_t|V - V^2] = \dfrac{3 - V}{R}$

$RK = 0.4\ V^{-1}$, $|V_t| = 2$

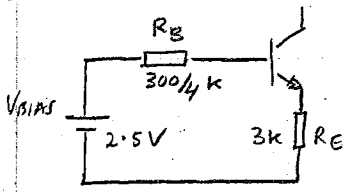
$$4V - V^2 = 5/2(3 - V)$$

$$V^2 - \frac{13V}{2} + \frac{15}{2} = 0$$

$$V = \frac{13 \pm 7}{4} = \cancel{5V} \text{ or } 1.5V$$

$> V_{DD}$ ⇒ $\underline{V = 1.5\ V}$ [5

2 a) Bias cct



KVL : $I_E R_E + V_{BE} + I_B R_B = V_{BIAS}$

$$\Rightarrow \quad I_E = \frac{V_{BIAS} - V_{BE}}{R_E + R_B/_{1+\beta}}$$

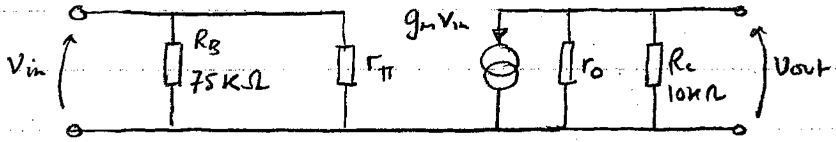
Assuming $V_{BE} \sim 0{\cdot}7\ V$ $\Rightarrow$ $I_E = \dfrac{2{\cdot}5 - 0{\cdot}7}{\left(3 + \frac{300}{4 \times 101}\right)k} = 481\ \mu A$

$I_c = \alpha I_E = \underline{\underline{476\ \mu A}}$ $\qquad V_{OUT} = 10 - 10 \times 0{\cdot}476 = \underline{\underline{5{\cdot}24V}}$

[6]

b) In mid-band, by-pass capacitor is s/c

$\Rightarrow$ SSEC :



$g_m = \dfrac{I_c}{V_T} = 19\ mS$

$r_\pi = \beta/g_m = 5{\cdot}25\ k\Omega$

$r_o = V_A/I_c = 252\ k\Omega$

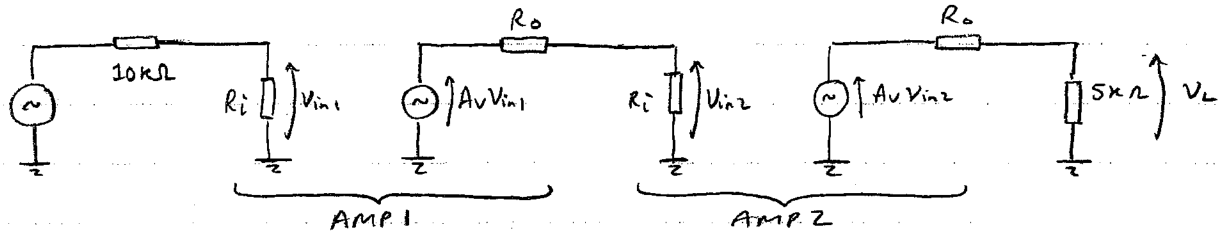
By inspection : $R_i = R_B \| r_\pi = 75k \| 5{\cdot}25k = \underline{\underline{4{\cdot}91\ k\Omega}}$

$R_o = R_c \| r_o = 10k \| 252k = \underline{\underline{9{\cdot}62\ k\Omega}}$

$A_V = -g_m R_o = -0{\cdot}019 \times 9{\cdot}62k = \underline{\underline{-183}}$

[9]

c) Using macromodels, overall SSEC in mid-band is :



Working R → L :

$$V_L = \frac{5k}{5k + R_o} \cdot A_V V_{in2} = \frac{5}{5+R_o} \cdot A_V \cdot \frac{R_i}{R_i + R_o} \cdot A_V V_{in1}$$

$$= \frac{5}{5+R_o} \cdot A_V \cdot \frac{R_i}{R_i + R_o} \cdot A_V \cdot \frac{R_i}{R_i + 10} \cdot V_s$$

$\Rightarrow$ overall gain is $\dfrac{V_L}{V_s} = \dfrac{5}{5+9{\cdot}62} \times (-183)^2 \times \dfrac{4{\cdot}91}{4{\cdot}91 + 9{\cdot}62} \times \dfrac{4{\cdot}91}{4{\cdot}91 + 10}$

$= 0{\cdot}342 \times 33489 \times 0{\cdot}338 \times 0{\cdot}329$

$= \underline{\underline{+1274}}$

[5]

3 a) Resistor sets operating point by holding Gate + Drain of Q1 at same potential ($I_G = 0$).

Both MOSFETs have $V_{DS} = V_{GS}$, and $V_{DD} > V_{t1} + V_{t2}$

$\Rightarrow$ Both are active

So, $I_D = K_1 (V_{OUT} - V_{t1})^2 = K_2 (V_{DD} - V_{OUT} - V_{t2})^2$

$\sqrt{\ }$ and rearrange:

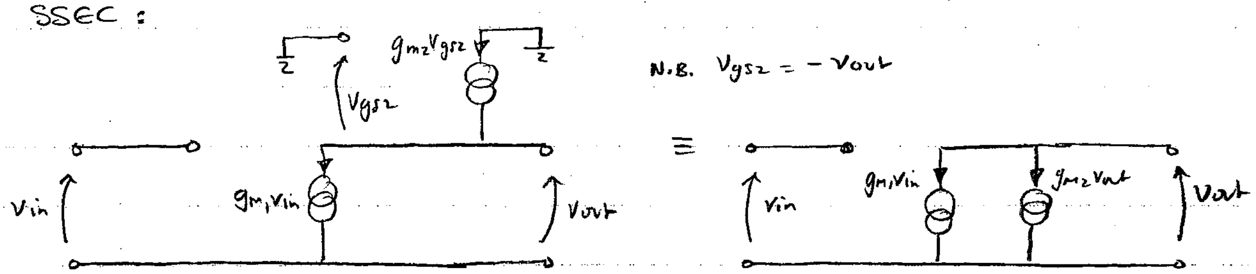
$$V_{OUT} = \frac{V_{DD} - V_{t2} \pm V_{t1}\sqrt{K_1/K_2}}{1 \pm \sqrt{K_1/K_2}}$$

Taking +ve root (−ve root gives $V_{OUT} < 0$) gives req'd result,

Putting $V_{DD} = 12\,V$, $V_{t2} = V_{t1} = 2V$, $K_1/K_2 = 9$ $\Rightarrow$ $\underline{\underline{V_{OUT} = 4V}}$

using $I_D = K_1 (V_{OUT} - V_{t1})^2$ $\Rightarrow$ $\underline{\underline{I_D = 1.08\ mA}}$ [8]

b) SSEC:



N.B. $V_{gs2} = -V_{out}$

KCL @ o/p gives $g_{m1} V_{in} + g_{m2} V_{out} = 0$ $\Rightarrow$ $A_v = -\dfrac{g_{m1}}{g_{m2}}$

But $g_m = 2\sqrt{K I_D}$ $\Rightarrow$ $A_v = -\sqrt{\dfrac{K_1}{K_2}} = \underline{\underline{-3}}$ [8]

c) if V_{in} is applied signal, then total o/p voltage (ie bias + signal) is:

$$V_{OUT} = 4 - 3V_{in}$$

For Q2 to remain in conduction, require $V_{OUT} \leq 10V$

Corresponding condition on V_{in} is $4 - 3V_{in} \leq 10V$ $\quad V_{in} \geq -2V$

For Q1, require $V_{DS} = V_{OUT} \geq V_{GS} - V_t$

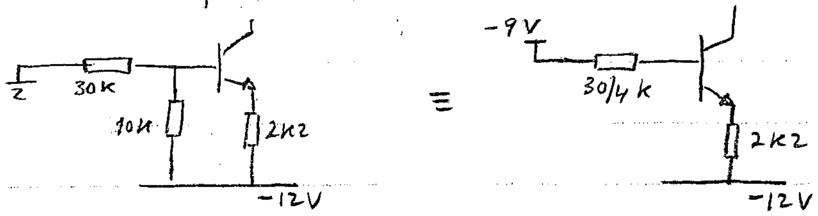
But $V_{GS\,total} = 4 + V_{in}$

$\Rightarrow$ condition on V_{in} is $4 - 3V_{in} \geq 4 + V_{in} - 2$

$V_{in} \leq 0.5$

So, if applied signal is sinusoidal with amplitude A, allowed range of A is $0 \leq A \leq 0.5$ [4]

4 a) With $V_c = 0$, tail current source is:



KVL : $I_{B3}\left(\frac{30}{4}k\right) + V_{BE} + I_{E3}\,2k2 = 3V$

Putting $I_{B3} = I_{E3}/101$ and $V_{BE} \simeq 0.7$ $\Rightarrow$ $I_{E3} = 1.01\ mA$

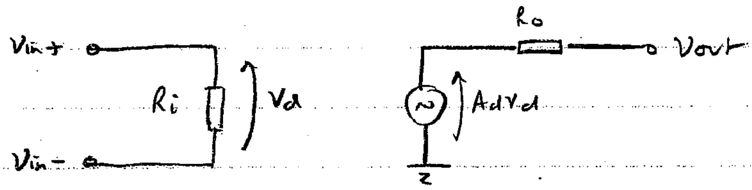
$I = \alpha I_{E3}$ $\Rightarrow$ $\underline{\underline{I = 1.0\ mA}}$

when $V_{IN+} = V_{IN-}$, $I_{E1} = I_{E2} = I/2$

$\Rightarrow I_{C2} = \frac{\alpha I}{2} = 495\ \mu A$

and $\underline{\underline{V_{OUT} = 12 - 0.495 \times 10 = 7.05\ V}}$ [6]

b) Macromodel :



with :

$R_i = 2r_\pi = \frac{2\beta}{g_m}$ where $g_m = \frac{I_{C1,2}}{V_T} = \frac{\alpha I}{2V_T}$

$\Rightarrow$ $\underline{\underline{R_i = \frac{4V_T(\beta+1)}{I}}}$

$\underline{\underline{R_o = 10\,k\Omega}}$

$\underline{\underline{A_d = \frac{g_m R_o}{2} = \frac{\alpha I R_o}{2V_T}}}$ [8]

c) Neglecting I_{B3} :

$V_c = -5V \Rightarrow V_{B3} = -12 + \frac{7}{4} = -10.25$, $V_{E3} = -10.95$, $I = 0.477\ mA$

$\Rightarrow$ $\underline{\underline{A_v = 94 = A_{v\,MIN}}}$

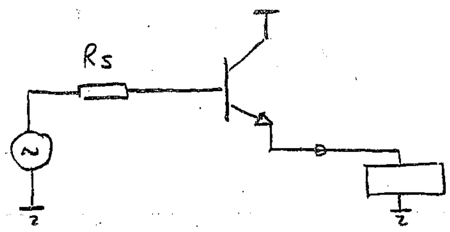
$V_c = +5V$ $\Rightarrow V_{B3} = -12 + \frac{17}{4} = -7.75$, $V_{E3} = -8.45$, $I = 1.614\ mA$

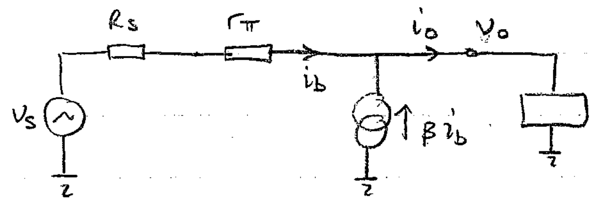
$\Rightarrow$ $\underline{\underline{A_v = 318 = A_{v\,MAX}}}$

CMVR : Q2 saturates when $V_{IN} \simeq V_{OUT} + 0.5$ (MAX V_{IN})
($V_{IN+} = V_{IN-} = V_{IN}$) Q3 saturates when $V_{IN} \simeq V_{B3} - 0.5 + 0.7$ (MIN V_{IN})
$\simeq V_{B3} + 0.2$

$V_c = -5V$: $V_{B3} = -10.25$ and $V_{OUT} = 12 - \frac{10 \times 0.477}{2} = 9.62$ $\Rightarrow$ $-10 \lesssim V_{IN} \lesssim 10$

$V_c = +5V$: $V_{B3} = -7.75$ and $V_{OUT} = 12 - \frac{10 \times 1.614}{2} = 3.93$ $\Rightarrow$ $-7.5 \lesssim V_{IN} \lesssim 4.4$ [6]

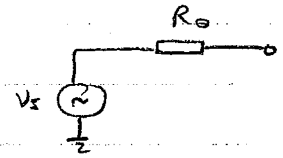
5 a) 

SSEC: 

NB: biasing not shown.

From SSEC: $i_b = \dfrac{V_s - V_o}{R_s + r_\pi}$ and $i_o = (1+\beta)\, i_b$

$\Rightarrow i_o = \dfrac{V_s - V_o}{R_o}$ where $R_o = \dfrac{R_s + r_\pi}{1+\beta}$

and source / follower combination is equiv. to  [6]

b) $R_s = 5k\Omega \,//\, r_d$ where r_d = zener dynamic res = 5Ω

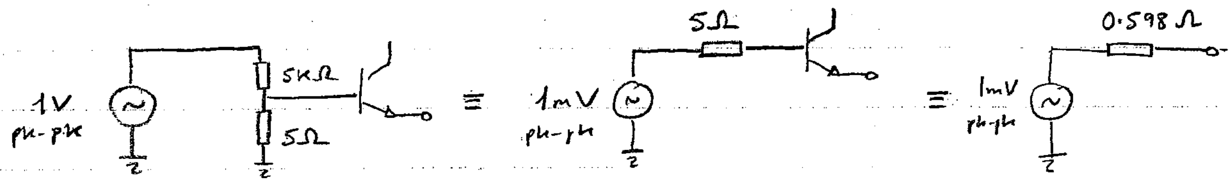
At $I = 50$ mA, $\dfrac{r_\pi}{1+\beta} = \dfrac{V_T}{I_E} = \dfrac{25mV}{50mA} = 0.5\ \Omega$

$\Rightarrow R_o = \dfrac{5}{51} + 0.5 = 0.598\ \Omega$

change ΔV in V for change ΔI in I is just $\Delta V = -R_o \Delta I$

Putting $\Delta I = 5mA$, $\underline{\underline{\Delta V = -0.598 \times 5 = -3\ mV}}$ [5]

Ripple:



pk-pk ripple at o/p $= \dfrac{100}{100 + 0.598} \times 1mV \sim \underline{\underline{1mV\ pk\text{-}pk}}$ [5]

Max I:

Current in 5k is shared by zener and transistor base

$I_{5k} \sim \dfrac{15 - 5.7}{5k\Omega} = 1.86\ mA$

Zener regulation lost when $I_{zener} \to 0$

This occurs when $I_B = 1.86$ mA or $I = 51 \times 1.86 \simeq 95$ mA

$\Rightarrow$ Range is $\underline{\underline{0 \leq I \lesssim 95\ mA}}$ [4]

E1.4