IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2007

EEE/ISE PART I: MEng, BEng and ACGI

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DIGITAL ELECTRONICS 1

Monday, 21 May 10:00 am

Time allowed: 2:00 hours

There are FOUR questions on this paper.

Q1 is compulsory.
Answer Q1 and any two of questions 2-4.
Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P.Y.K. Cheung, P.Y.K. Cheung
Second Marker(s) : Z. Durrani, Z. Durrani

Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least significant bit of a bus signal is labelled as bit 0, and the most significant bit with the highest integer number. Therefore the signal X[7:0] is an eight bit bus with X7 being the MSB and X0 the LSB.

In questions involving circuit design, you may use any standard digital circuits that are not explicitly forbidden by the question provided that you fully specify their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

[Question 1 is compulsory]

1. a) Figure 1.1 shows the truth table of a three-input, two-output logic module. Using Karnaugh maps, derive minimal sum-of product expressions for F and G.

inputs			outputs	
A	B	C	F	G
0	0	0	0	1
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	1
1	1	0	1	1
1	1	1	1	1

Figure 1.1

[4]

b) The waveforms for signals P and Q shown in Figure 1.2 are applied to the circuit shown in Figure 1.3. Copy the timing diagram and add waveforms for S, T, U and V. Assume that initially U=0 and V=1.

[6]

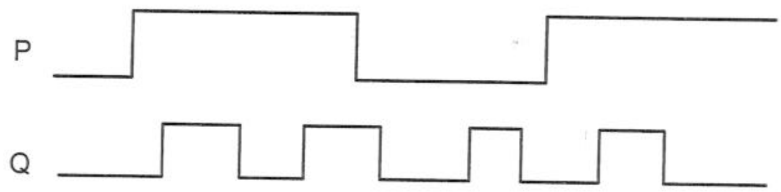


Figure 1.2

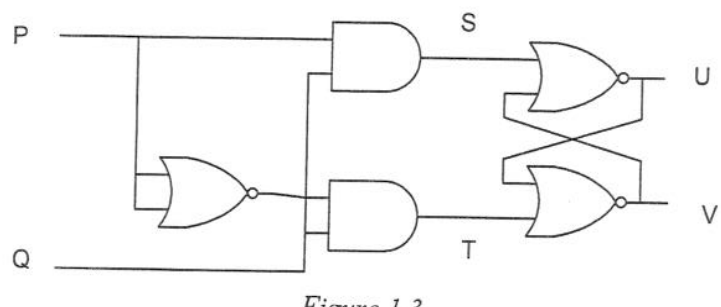


Figure 1.3

c) Assuming that all numbers are represented using 16 bits, and that ASCII characters are stored as consecutive bytes, complete the missing entries which are not shaded in the following table. An ASCII table is provided at the end of this paper. Signed numbers are represented in 2's complement form.

(No marks will be awarded for this question unless you show how the solutions are derived.)

Unsigned Decimal	Signed Decimal	Hexadecimal	Binary	ASCII
?		?	0100 1000 0110 1001	?
?	-2049	?		

[10]

d) Given that $F = \overline{X}\,Y\,\overline{Z} + \overline{X}\,\overline{Y}\,Z$, find $\overline{F}$ in product-of-sum form.

[4]

e) Simplify the Boolean expression $A\,B + \overline{A}\,C + B\,C$ using Boolean algebra so that the expression is sum of two products, each product having only two variables.

[6]

f) For the circuit shown in Figure 1.4, draw a truth table showing the output Q for all combinations of inputs A, B and C.

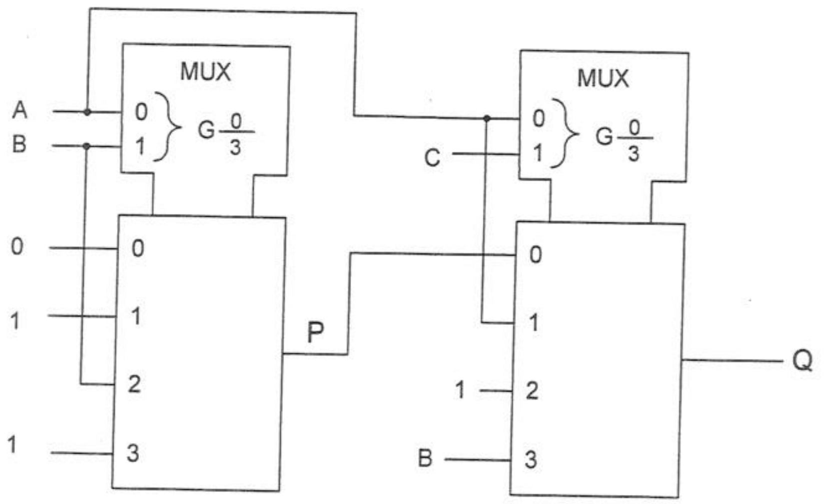


Figure 1.4

[6]

e) Draw the state transition table for the finite state machine (FSM) shown in Figure 1.5.

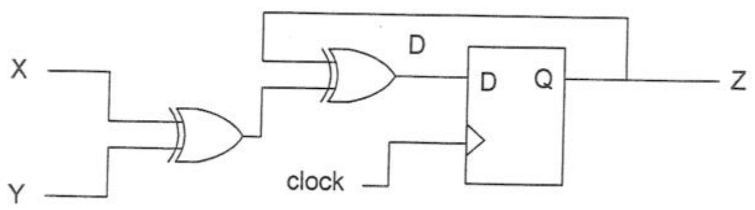


Figure 1.5

[4]

2. a) With the aid of a diagram, show how the following logic function can be implemented on a PAL device.

$$f = (\overline{X} + Y + \overline{Z})\,(X + \overline{Y})$$

[10]

b) Figure 2.1 shows a finite state machine (FSM) implemented with a ROM that contains eight 4-bit numbers and three D flip-flops. The ROM address signals are A[2:0] and the ROM data signals are D[3:0]. D[2:0] are connected to the D inputs of three flip-flops as shown in Figure 2.1. The most significant data bit D3 from the ROM provides the output signal Z. The outputs of the flip-flops Q2, Q1 and Q0 are connected to the address signals A2, A1 and A0 of the ROM respectively. The contents of the ROM are shown in Figure 2.2. The registers are initially set to all ones (i.e. Q0 = Q1= Q2= '1').

(i) Draw a Moore state diagram showing the state transitions and the output values of the FSM.

[10]

(ii) Sketch the waveforms for the signals Q[2:0] and Z for at least 6 cycles of the clock.

[10]

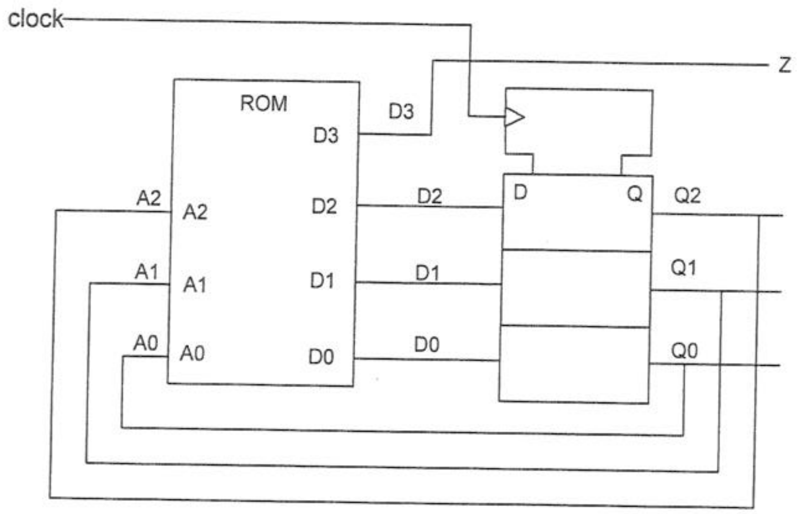


Figure 2.1

Address A[2:0]	ROM Data D[3:0]
0	0001
1	1101
2	0000
3	1000
4	0000
5	0110
6	1011
7	0000

Figure 2.2

3. a) Figure 3.1 shows a combinational circuit with six inputs (D3, D2, D1, D0, S1, S0) and one output Y. Derive a Boolean equation for Y. Hence, or otherwise, draw a functional truth table for this circuit.

[10]

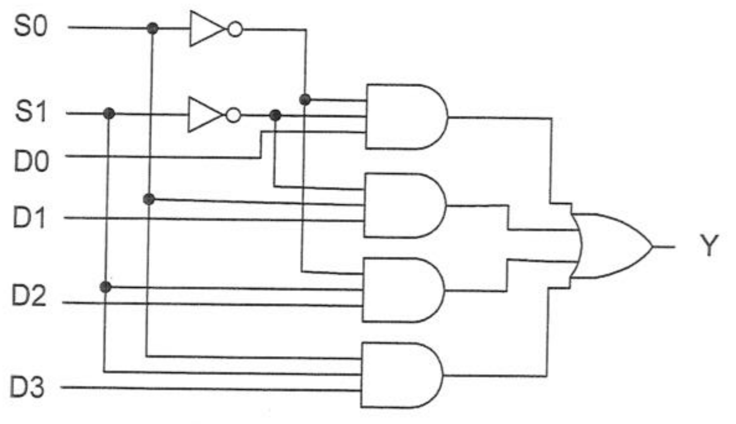


Figure 3.1

b) Figure 3.2 shows the truth-table of a priority encoder circuit with 4 inputs (D3, D2, D1 and D0), and two outputs (A1, A0). Use Karnaugh maps to find the minimized Boolean equations for A1 and A0. Hence design a gate level implementation for this circuit. You may use any basic gate types.

[10]

Inputs				**Outputs**	
D3	**D2**	**D1**	**D0**	**A1**	**A0**
0	0	0	0	X	X
0	0	0	1	0	0
0	0	1	X	0	1
0	1	X	X	1	0
1	X	X	X	1	1

Figure 3.2

c) Modify the circuits in a) and b) above so that only NAND gates are used. You may use NAND gates with any number of inputs above 2.

[10]

4. a) Design a half adder circuit using only 2-input NOR gates.

[8]

b) Using half adders and 2-input NOR gates, design a 4-bit binary adder circuit that adds two 4-bit numbers A[3:0] and B[3:0] to produce a 4-bit sum S[3:0].

[10]

c) Figure 4.1 shows a 4-bit adder-subtractor circuit. When the input SUB is low, the circuit performs a 4-bit addition A+B. When the input SUB is high, the circuit performs a 4-bit subtraction A-B. By adding extra components to the design in b), or otherwise, design the adder-subtractor circuit.

[8]

d) The circuit in c) is used to add and subtract 4-bit signed numbers in 2's complement form. State with examples the conditions under which this circuit would produce wrong answers.

[4]

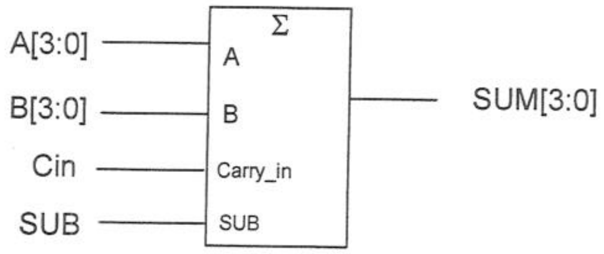


Figure 4.1

ASCII Table for Question 1

Ctrl	Dec	Hex	Char	Code	Dec	Hex	Char	Dec	Hex	Char	Dec	Hex	Char
^@	0	00		NUL	32	20	sp	64	40	@	96	60	`
^A	1	01	☺	SOH	33	21	!	65	41	A	97	61	a
^B	2	02	☻	STX	34	22	"	66	42	B	98	62	b
^C	3	03	♥	ETX	35	23	#	67	43	C	99	63	c
^D	4	04	♦	EOT	36	24	$	68	44	D	100	64	d
^E	5	05	♣	ENQ	37	25	%	69	45	E	101	65	e
^F	6	06	♠	ACK	38	26	&	70	46	F	102	66	f
^G	7	07	•	BEL	39	27	'	71	47	G	103	67	g
^H	8	08	◘	BS	40	28	(	72	48	H	104	68	h
^I	9	09	○	HT	41	29	)	73	49	I	105	69	i
^J	10	0A	◙	LF	42	2A	*	74	4A	J	106	6A	j
^K	11	0B	♂	VT	43	2B	+	75	4B	K	107	6B	k
^L	12	0C	♀	FF	44	2C	,	76	4C	L	108	6C	l
^M	13	0D	♪	CR	45	2D	—	77	4D	M	109	6D	m
^N	14	0E	♫	SO	46	2E	.	78	4E	N	110	6E	n
^O	15	0F	☼	SI	47	2F	/	79	4F	O	111	6F	o
^P	16	10	►	SLE	48	30	0	80	50	P	112	70	p
^Q	17	11	◄	CS1	49	31	1	81	51	Q	113	71	q
^R	18	12	↕	DC2	50	32	2	82	52	R	114	72	r
^S	19	13	‼	DC3	51	33	3	83	53	S	115	73	s
^T	20	14	¶	DC4	52	34	4	84	54	T	116	74	t
^U	21	15	§	NAK	53	35	5	85	55	U	117	75	u
^V	22	16	▬	SYN	54	36	6	86	56	V	118	76	v
^W	23	17	↨	ETB	55	37	7	87	57	W	119	77	w
^X	24	18	↑	CAN	56	38	8	88	58	X	120	78	x
^Y	25	19	↓	EM	57	39	9	89	59	Y	121	79	y
^Z	26	1A	→	SIB	58	3A	:	90	5A	Z	122	7A	z
^[	27	1B	←	ESC	59	3B	;	91	5B	[	123	7B	{
^\	28	1C	∟	FS	60	3C	<	92	5C	\	124	7C	|
^]	29	1D	↔	GS	61	3D	=	93	5D	]	125	7D	}
^^	30	1E	▲	RS	62	3E	>	94	5E	^	126	7E	~
^_	31	1F	▼	US	63	3F	?	95	5F	_	127	7F	⌂[†]

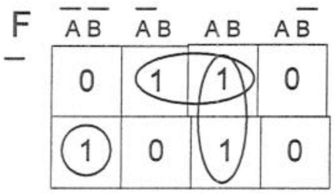
[THE END]

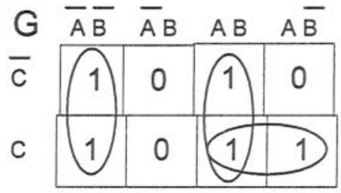
E1.2 Digital Electronics 1
Solutions 2007

All questions are unseen.

Question 1 is compulsory.

1. a) SOLUTION:



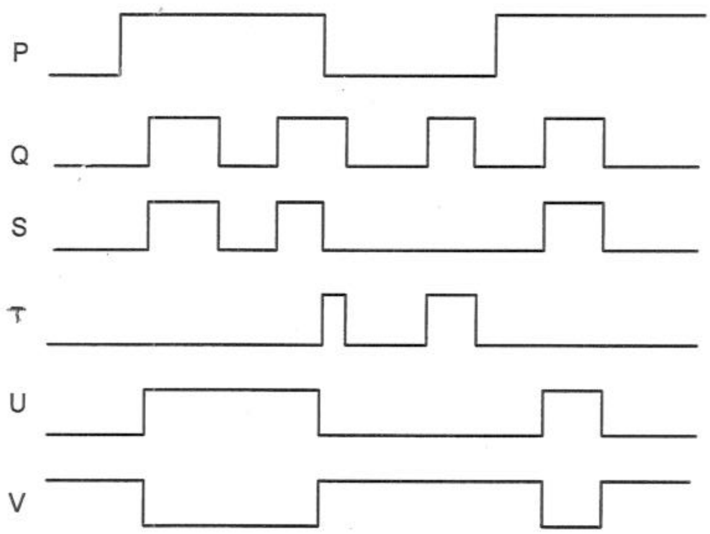


$F = B\overline{C} + AB + \overline{A}\,\overline{B}C$

$G = \overline{A}\,\overline{B} + AB + A\ C$

[4]

b) SOLUTION:



[6]

c)

SOLUTION:

Unsigned Decimal	Signed Decimal	Hexadecimal	Binary	ASCII
18537		**4869**	0100 1000 0110 1001	**"Hi"**
65022	-2049	**FDFE**		

[10]

d) SOLUTION:

$$\overline{F} = (X + \overline{Y} + Z)\,(X + Y + \overline{Z})$$

[4]

e) SOLUTION:

$$\begin{aligned} & AB + \overline{A}C + BC \\ &= AB + BC(A + \overline{A}) + \overline{A}C \\ &= AB + ABC + \overline{A}BC + \overline{A}C \\ &= AB(C+1) + \overline{A}C(B+1) \\ &= AB + \overline{A}C \end{aligned}$$

[6]

f) SOLUTION:

C	B	A	P	Q
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

[6]

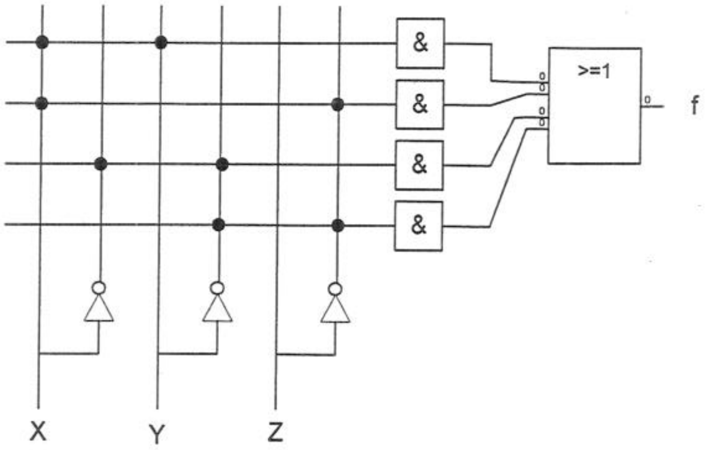
g) SOLUTION:

Z	X	Y	D = next Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

[4]

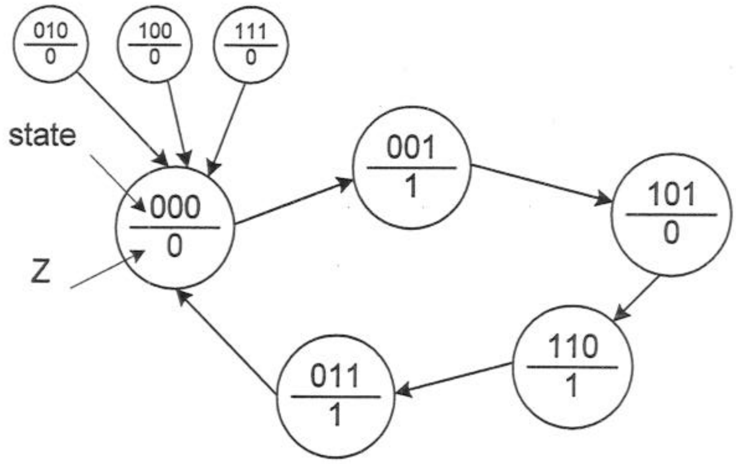
2. SOLUTION

a)



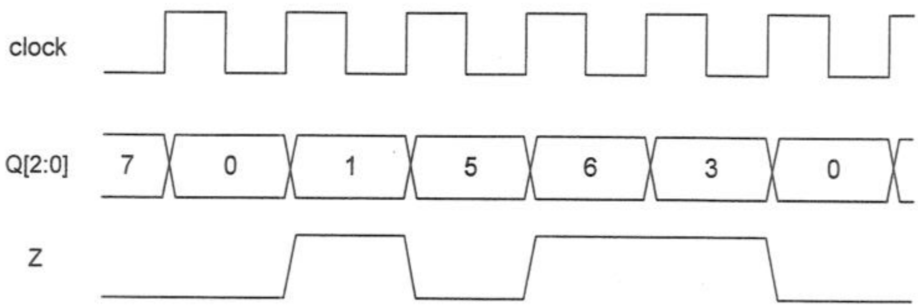
[10]

b) (i)



[10]

(ii)



[10]

3. SOLUTION:

a)

$$Y = \overline{S1}\,\overline{S0}\,D0 + \overline{S1}\,S0\,D1 + S1\,\overline{S0}\,D2 + S1\,S0\,D3$$

S1	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

[10]

b)

A1

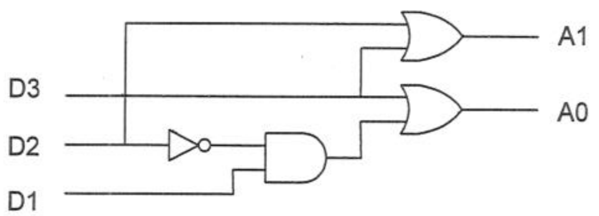
D3 D2 \ D1 D0	00	01	11	10
00	X	0	0	0
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

A1 = D2 + D3

A0

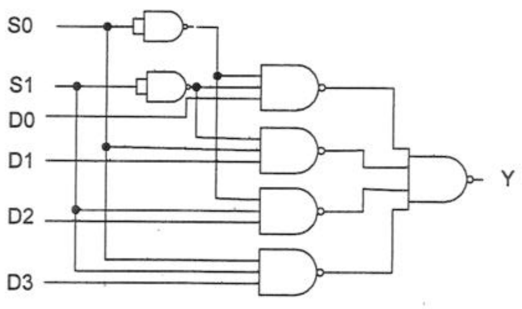
D3 D2 \ D1 D0	00	01	11	10
00	X	0	1	1
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

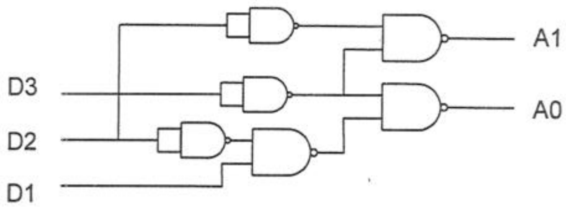
$A0 = D3 + D1\,\overline{D2}$



[10]

c)

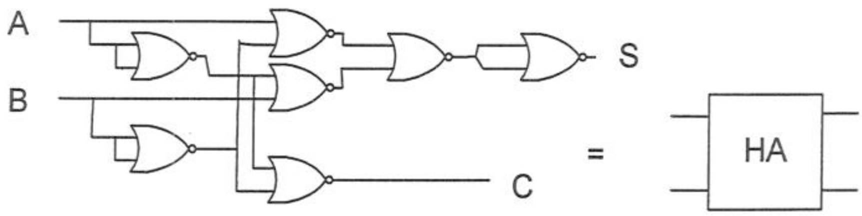




[10]

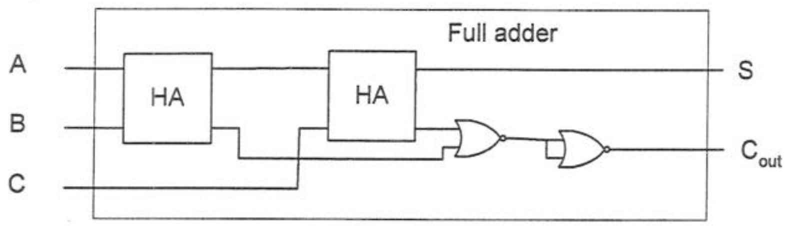
4. SOLUTION:

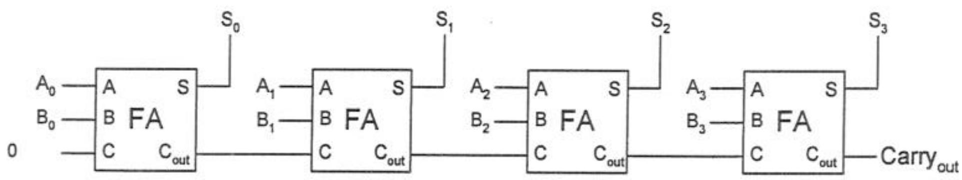
a)



[8]

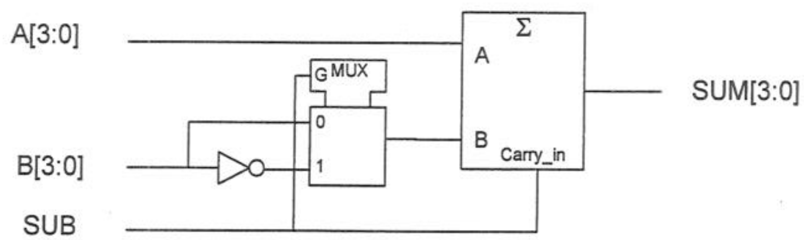
b)





[10]

c)



[8]

d)

When the sum or difference of the two numbers falls outside the range of value -8 to +7. For example, 7+3 will give a sum -6 and not +10. Similar -7-3 gives 6, not -10.

[4]