IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2003

**DIGITAL ELECTRONICS 1**

Tuesday, 27 May 10:00 am

Time allowed: 2:00 hours

**There are FIVE questions on this paper.**

**Question 1 is compulsory.**

**Answer THREE questions, including Question 1.**

**Corrected Copy**
10:00 Fig 1.3

**Any special instructions for invigilators and information for candidates are on page 1.**

Examiners responsible First Marker(s) : P.Y.K. Cheung
Second Marker(s) : P.A. Naylor

**[Question 1 is compulsory]**

1. a) For the circuit shown in figure 1.1, draw a truth table showing the output Q for all combinations of inputs A, B and C.

[4]

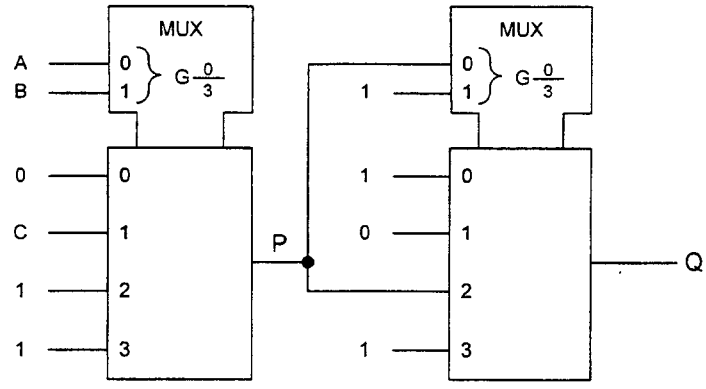



*Figure 1.1*

b) Minimize the following Boolean functions:

$$f = \overline{(A + \overline{B})\,(\overline{A} + B)}$$

$$g = \overline{\overline{A}\,\overline{B}\,C\,D}$$

[4]

c) Assuming that all numbers are 16 bits wide, complete the missing entries which are not shaded in the following table. (No marks will be awarded for this question unless you show your working.)

| Decimal | Hexadecimal | Binary | BCD |
|---|---|---|---|
| 7245 | ? | | |
| | | 1001011101010010 | ? |
| ? | 37FD | | |
| -2317 | ? | | |

[4]

d) Simplify the following expression using a Karnaugh map.

$$y = \overline{(C + D)} + \overline{A}\,C\,\overline{D} + A\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C\,D + A\,C\,\overline{D}$$

[4]

e) The timing diagram of figure 1.2 shows the waveforms that are applied to the circuit shown in figure 1.3. Copy the timing diagram and add waveforms for S,R and Q. Assume that initially Q=0.

[4]

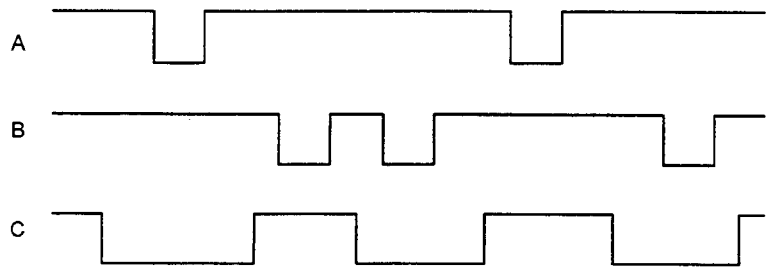
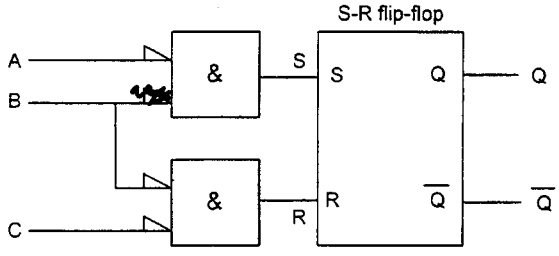



*Figure 1.2*




10·00a m

No inversion on line B

*Figure 1.3*

2. a) Figure 2.1 shows a 4-bit parallel counter circuit implemented with J-K flip-flops. Analyse its function and determine its counting sequence. You should assume that all flip-flops are initially in the reset state.

[8]

b) Redesign the circuit in a) using D flip-flops instead of J-K flip-flops. Your solution should be in the form of Boolean equations.

State whether your D flip-flop implementation has any advantages or disadvantages over the JK implementation shown in figure 2.1.

[12]

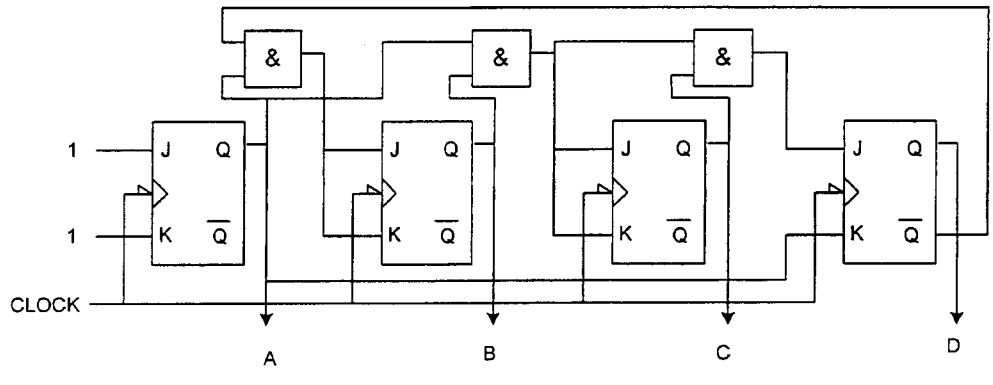



*Figure 2.1*

3. a) With the aid of a diagram, show how the following logic function can be implemented on a PAL device.

$$f = (A + \overline{B} + C)(\overline{A} + C)$$

[6]

b) Figure 3.1 shows a finite state machine (FSM) implemented with a ROM that contains four 4-bit numbers. The ROM address signals are A[1:0] and the ROM data signals are D[3:0]. D[1:0] are connected to the D inputs of two registers as shown in Figure 3.1. The upper two data bits from the ROM D[3:2] are providing the output signals F and G respectively. The outputs of the registers Q1 and Q0 are connected to the address signals A1 and A0 of the ROM respectively. The content of the ROM is shown in Figure 3.2. The registers are initially in a reset state (i.e. Q0 = Q1 = '0').

(i) Draw a diagram showing the state transition and the output values for the FSM. [6]

(ii) Write down the important difference(s) between the two types of FSM and to say to which type the FSM of figure 3.1 corresponds. [4]

(iii) Sketch the waveforms for the output signals F and G for at least 4 cycles of the clock. [4]

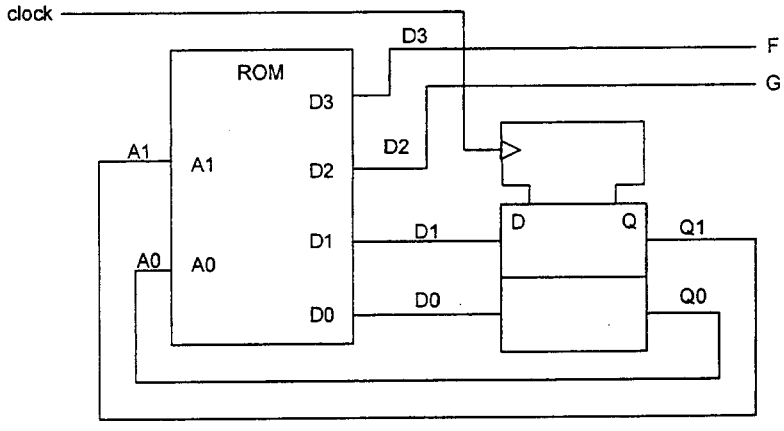



*Figure 3.1*

| Address A[1:0] | ROM Data D[3:0] |
|---|---|
| 0 | 1111 |
| 1 | 0100 |
| 2 | 1001 |
| 3 | 0110 |

*Figure 3.2*

4. a) Design a half adder circuit using only 2-input NAND gates.

[5]

b) Using half adders and 2-input NOR gates, design a 4-bit binary adder circuit that adds two 4-bit numbers A[3:0] and B[3:0] to produce a 4-bit sum S[3:0].

[5]

c) By adding extra components to the design in b), or otherwise, design a 4-bit binary adder/subtractor circuit with an additional input signal SUB such that:

```
IF (SUB = 0)
   S[3:0] = A[3:0] + B[3:0];
ELSE
   S[3:0] = A[3:0] – B[3:0];
```

[5]

d) The circuit in c) is used to add and subtract 4-bit signed numbers in 2's complement form. State with examples the conditions under which this circuit would produce wrong answers.

[5]

5. Figure 5.1 shows the IEEE/ANSI symbol for a 74290 counter integrated circuit.

a) What is the function performed by the inputs $MR_1$ and $MR_2$?

[3]

b) What is the function performed by the inputs $MS_1$ and $MS_2$?

[3]

c) If the circuit is connected as shown in Figure 5.2 with a periodic clock signal applied to the input $\overline{CP_0}$, list the sequence that is observed at the outputs $Q_3$, $Q_2$, $Q_1$ and $Q_0$.

[7]

d) Figure 5.3 shows another way that the counter can be connected. The periodic clock signal is now applied to the input $\overline{CP_1}$. Described with reasons the signal expected at the output $Q_0$.

[7]

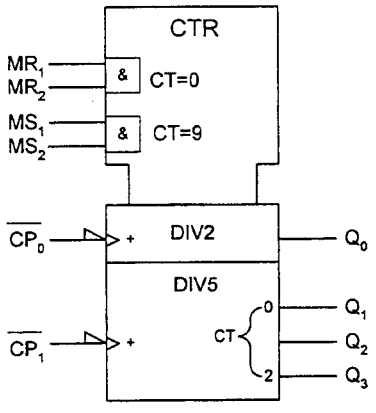



*Figure 5.1*

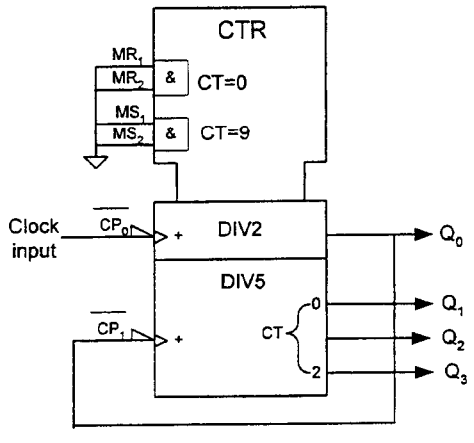



*Figure 5.2*

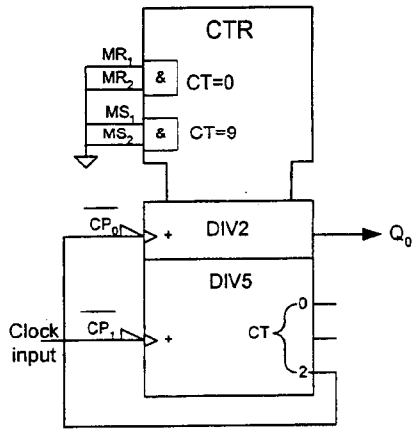



*Figure 5.3*

**E1.2 Digital Electronics 1**
**Solutions 2003**

**Question 1 is compulsory.**

1. a)

| A | B | C | P | Q |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |

[4]

b)

$$f = \overline{A}\,B + A\,\overline{B}$$

$$g = \overline{\overline{A\,B}\,C + \overline{D}}$$
$$= (\overline{A} + \overline{B})\,C + \overline{D}$$

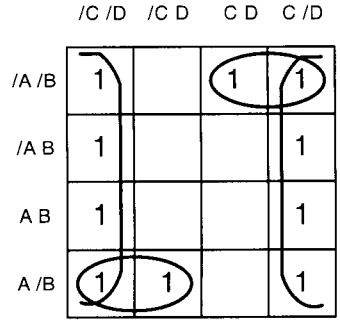
[4]

c)

| Decimal | Hexadecimal | Binary | BCD |
|---|---|---|---|
| 7245 | **1C4D** | | |
| | | 1001011101010010 | **9752** |
| **14333** | 37FD | | |
| -2317 | **F6F3** | | |

[4]

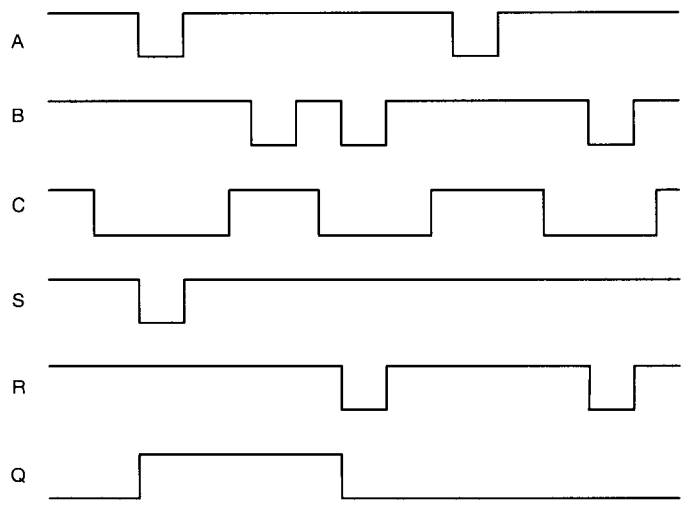
d)




$$y = \overline{D} + \overline{A}\,\overline{B}\,C + A\,\overline{B}\,\overline{C}$$

[4]

e)




[4]

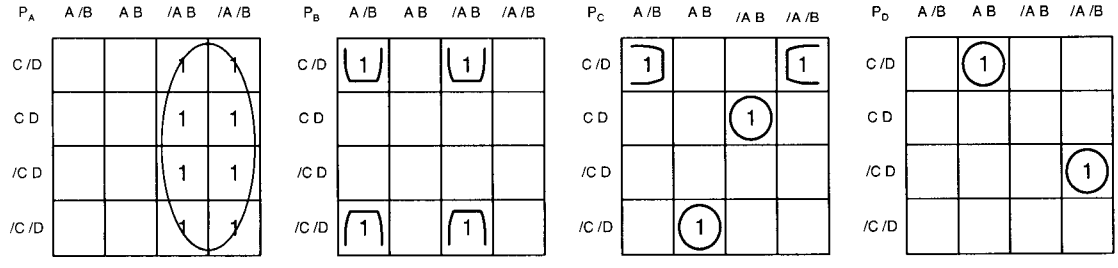
2. a)

| D | C | B | A |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 |

Counter reset to zero after 9.

[8]

b) Inputs to D flip-flops are $P_D$:$P_C$:$P_B$:$P_A$ and outputs are D:C:B:A.




$$P_A = \overline{A}$$

$$P_B = A\overline{B}\,\overline{D} + \overline{A}B\overline{D}$$

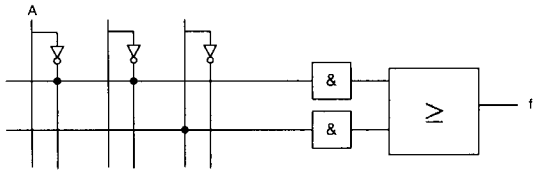
$$P_C = \overline{B}C\overline{D} + \overline{A}BCD + AB\overline{C}\,\overline{D}$$

$$P_D = ABC\overline{D} + \overline{A}\,\overline{B}\,\overline{C}D$$

[12]

3. a)

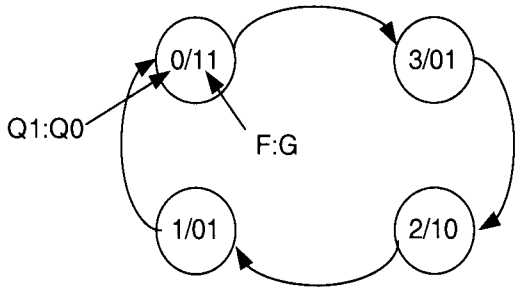
$$f = (A + \overline{B} + C)(\overline{A} + C)$$
$$= \overline{A}B\overline{C} + A\overline{C}$$




[6]

b)

(i)

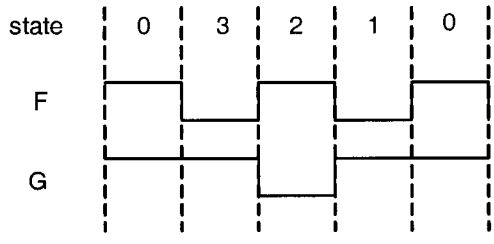



[6]

(ii) This is a Moore machine where outputs are only dependent on states. The other type is Mealey machine where output are dependent on both states and inputs.

[3]

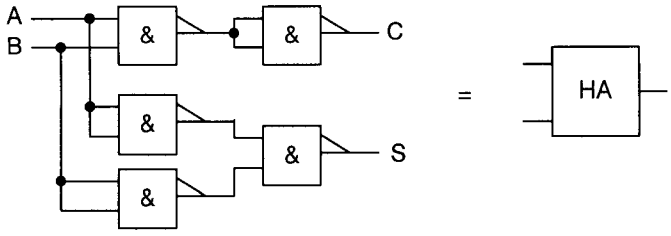
(iii)




[5]

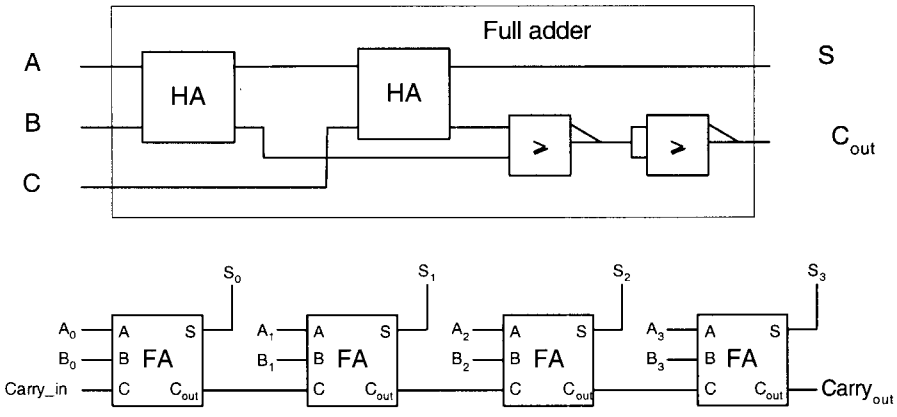
4. a)

| A | B | S | C |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |



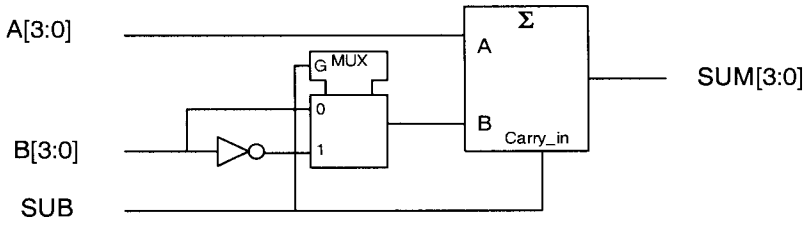

[5]

b)




[5]

c)




[5]

d)

When the sum or difference of the two numbers falls outside the range of value -8 to +7. For example, 7+3 will give a sum -6 and not +10. Similar -7-3 gives 6, not -10.

[5]

5. a)

MR1 & MR2 are just to reset all counter output to zero when both MR1 and MR2 are high.

[3]

b)

MS1 & MS2 are just to set the counter output to the value 9 when both signals are high.

[3]

c) The counter counts the sequence 0, 1, 2, 3, ....9, then 0 again. It is working as a BCD counter

[7]

d) The counter divides the input clock signal by 10 and produces a symmetric square wave at the output Q0. Q3:Q2:Q1 counts the sequence 000, 001, 010, 011, 100, 000 .....

Therefore Q3 changes once for every 5 clock cycles. DIV 2 output Q0 therefore gives a symmetric output at half the frequency of Q3.

[7]