Paper Number(s): **E1.2**
ISE1.2

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2001

EEE/ISE PART I: M.Eng., B.Eng. and ACGI

DIGITAL ELECTRONICS I

Wednesday, 13 June 10:00 am

There are FIVE questions on this paper.

Question 1 is compulsory.

Answer THREE questions, including Question 1.

Time allowed: 2:00 hours

CORRECTED COPY

Examiners: Naylor,P.A. and Coonick,A.H.

[Question 1 is compulsory]

1. a) State De Morgan's Theorem and hence miminise the function [4]

$$f = A.\overline{B}.C + B.C + A.\overline{C}\ .$$

b) Which one of the following statements best describes the expression 'setup time'? [4]

(i) The amount of time a clock signal must wait before making a transition,

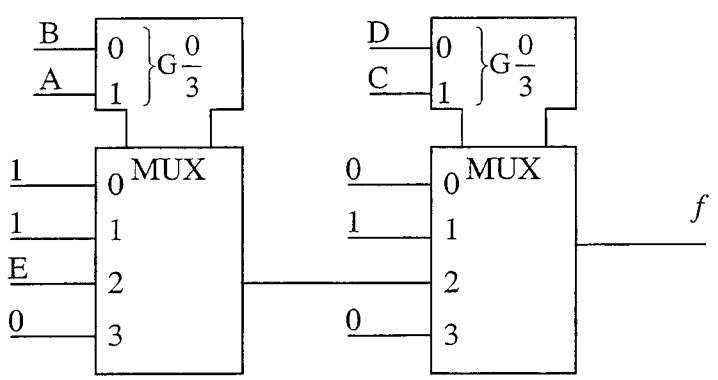
(ii) The period of time before a clock transition during which the input data can't change,

(iii) The interval of time prior to a clock transition during which a change in data could cause metastability,

(iv) The time taken for a device to arrive in a stable state,

(v) The duration of time taken by a device for its output to respond to changes in its input.

c) Determine the Boolean function f. [4]



d) An 8-bit microprocessor register contents is displayed as $A1 where $ indicates hexadecimal. What is the corresponding decimal value assuming 2's complement binary format? [4]

Convert the decimal number 3.14 into BCD.

Convert the decimal number 3.25 into single precision binary floating-point format.

e) Draw the Karnaugh map of the following function: [4]

$$f = A.\overline{B} + C(\overline{D} \oplus (A \oplus B)) + A.\overline{C}.D$$

State the number of gates required to implement this function, not counting inverters.

2. a) Describe the architecture of PALs with the aid of one or more illustrative diagrams. [4]

Indicate clearly how a PAL device would be programmed to implement a full adder. [4]

b) A 64x1-bit ROM is programmed as indicated in the table below. Deduce a minimal Boolean expression for the output in terms of the inputs. [7]

	Col 0 Cells 0-7	Col 1 Cells 8-15	Col 2 Cells 16-23	Col 3 Cells 24-31	Col 4 Cells 32-39	Col 5 Cells 40-47	Col 6 Cells 48-55	Col 7 Cells 56-63
Row 0	1	1	0	0	0	0	0	0
Row 1	1	0	0	0	0	0	0	0
Row 2	0	0	0	0	0	0	0	0
Row 3	0	0	0	0	0	0	0	0
Row 4	1	0	0	0	0	0	0	0
Row 5	1	0	0	0	0	0	0	0
Row 6	0	0	0	0	0	0	0	0
Row 7	0	1	0	0	0	0	0	0

c) Show how a multiplexer with two data inputs can be used to implement a 2-input OR gate. [5]

3. A warning indicator is to be designed using four red LEDs arranged in a line, spaced by 1.5 cm. To alert the user to danger, the LEDs are to light in the following repeating pattern.

Time Instant	LED3	LED2	LED1	LED0
1	◎	◎	○	○
2	○	◎	◎	○
3	○	○	◎	◎
4	○	◎	◎	○
5	◎	◎	○	○
6	○	◎	◎	○
Etc.				

The symbol ○ indicates the LED is off; ◎ indicates the LED is on.

Design a synchronous state machine to control the LEDs. Show the details of the design and sketch a circuit diagram of your state machine. [17]

State how you would connect the LEDs to the state machine outputs. [3]

4. Consider the number X as a 4-bit signed 2's complement binary number formed from the bits X3, X2, X1 and X0. Design a circuit to compute the square of X, giving the result also in signed 2's complement binary. Show in your design relevant truth tables and all other working. [20]

Sketch the resulting circuit diagram of your circuit.

5. Derive the Boolean equations of a single bit comparator with input bits A, B, > and < and outputs A>B and A<B, where the inputs > and < are override inputs. Sketch the corresponding circuit diagram. [7]

Show how your comparator can be used to compare two 4-bit signed 2's complement numbers. [7]

Determine the best-case and worst-case time to make a 4-bit comparison if each gate (including inverters) has a propagation delay of T seconds. Give examples of bit patterns for the two 4-bit numbers which correspond to the best-case and worst-case timing. [6]

Digital Electronics I 2001 Solutions

1.a) $\overline{X \cdot Y} \equiv \bar{X} + \bar{Y}$, $\overline{X+Y} \equiv \bar{X} \cdot \bar{Y}$

$f = A\bar{B}C + BC + A\bar{C} = A(\bar{B} + \bar{C}) + BC$

$= A(\overline{BC}) + BC = A + BC$

b) iii

c) $f = \bar{C}D + C\bar{D}P$, $P = \bar{A}\bar{B} + \bar{A}B + A\bar{B}E$

d) \$A1 ≡ 1010 0001 = -127 + 32 + 1 = -94

3.14 ≡ 0011, 0001 0100 (BCD)

3.25 = 0 1000 0000 101 00... (23 bits)

e)

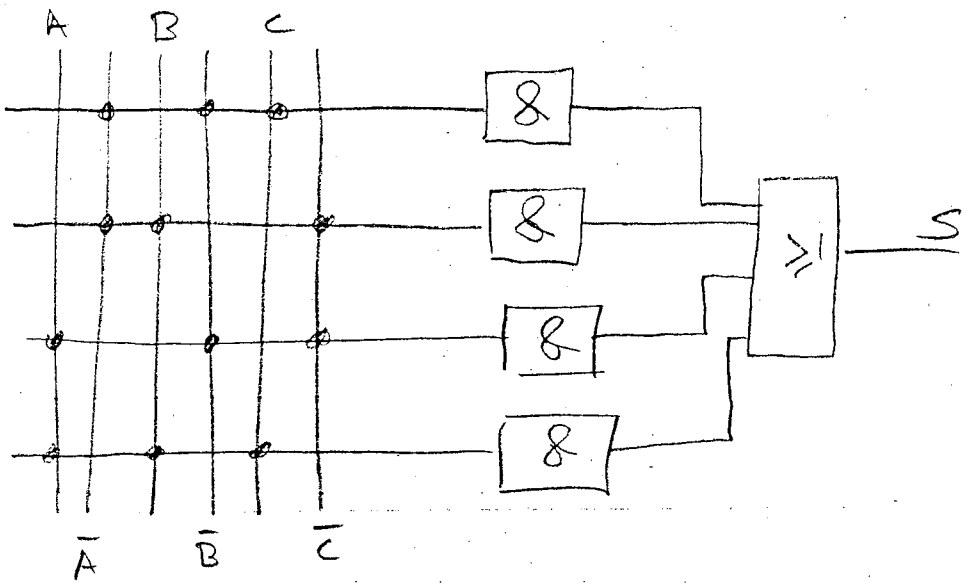
f	AB: 00	01	11	10
CD: 00	0	0	0	1
01	0	0	1	1
11	0	1	0	1
10	1	0	1	1

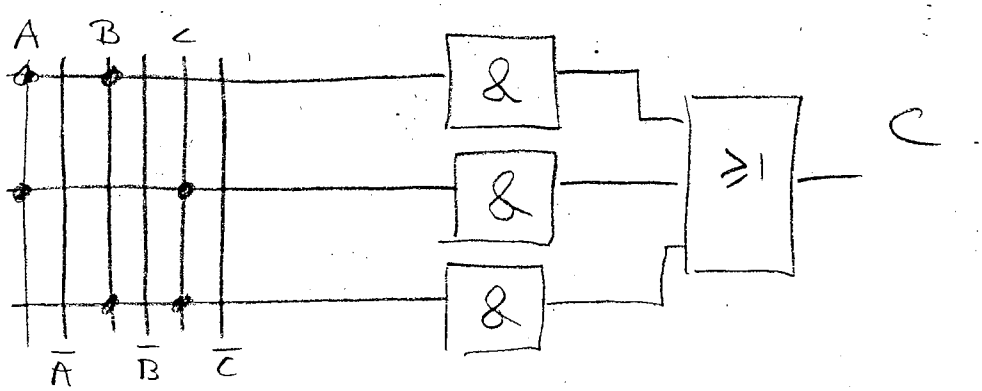
6 gates

2 a) PAL architecture - bookwork.

Full adder $S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$C = AB + C(A+B)$





b) 3 bits for Row, 1 bit for column.

B, C, D

A

f	AB 00	01	11	10
CD 00	1	1	0	1
01	1	1	0	0
11	0	0	1	0
10	0	0	0	0

$f = \bar{A}\bar{C} + \bar{B}\bar{C}\bar{D} + AB\bar{C}D$

c)

A	B	S	Output
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Let B = 0 then
Output = A + S

3) 4 states required ⇒ 2 state variables
Q_1, Q_0

Transition table

Q_1	Q_0	Q_1^+	Q_0^+	L3	L2	L1	L0
0	0	0	1	1	1	0	0
0	1	1	0	0	1	1	0
1	0	1	1	0	0	1	1
1	1	0	0	0	1	1	0

Next-state logic

Q_0^+	Q_0 = 0	Q_0 = 1
Q_1 = 0	1	0
Q_1 = 1	1	0

$Q_0^+ = \overline{Q_0}$

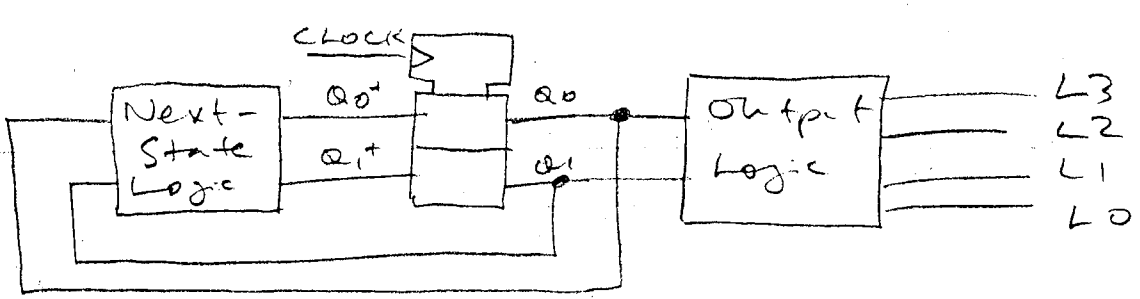
Q_1^+	Q_0 = 0	Q_0 = 1
Q_1 = 0	0	1
Q_1 = 1	1	0

$Q_1^+ = Q_0 \oplus Q_1$

Output Logic

$L3 = \overline{Q_1} \cdot \overline{Q_0}$, $L2 = \overline{Q_1} + Q_0$

$L1 = Q_1 + Q_0$, $L0 = Q_1 \cdot \overline{Q_0}$



The LEDs will require a current of the order of a milliamp. Connect using appropriate driver.

4.

X3	X2	X1	X0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	1	0	0	1
0	1	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	1	1	0	0	1
0	1	1	0	0	0	1	0	0	1	0	0
0	1	1	1	0	0	1	1	0	0	0	1
1	0	0	0	0	1	0	0	0	0	0	0
1	0	0	1	0	0	1	1	0	0	0	1
1	0	1	0	0	0	1	0	0	1	0	0
1	0	1	1	0	0	0	1	1	0	0	1
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	0	0	1	0	0	1
1	1	1	0	0	0	0	0	0	1	0	0
1	1	1	1	0	0	0	0	0	0	0	1

$Q7 = Q1 = 0$, $Q6 = X3 \cdot \bar{X2} \bar{X1} \cdot \bar{X0}$, $Q0 = X0$

Q5 \ X3X2 \ X1X0	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	0	0	0	0
10	0	1	0	1

Q4 \ X3X2 \ X1X0	00	01	11	10
00	0	0	0	0
01	1	1	1	0
11	1	0	0	0
10	0	1	1	0

$Q5 = \bar{X5} \cdot X2 \cdot X1 + X3 \cdot \bar{X2} (\bar{X1} \cdot X0 + X1 \cdot \bar{X0})$

$Q4 = \bar{X3} \cdot X2 \cdot X0 + X2 \bar{X1} \cdot \bar{X0} + X3 \cdot \bar{X2} \cdot X0$

		X1 X0			
	Q3	00	01	11	10
X3 X2	00	0	0	1	0
	01	0	1	0	0
	11	0	1	0	0
	10	0	0	1	0

		X1 X0			
	Q2	00	01	11	10
X3 X2	00	0	0	0	1
	01	0	0	0	1
	11	0	0	0	1
	10	0	0	0	1

$Q3 = X2 . \bar{X1} . X0 + \bar{X2} . X1 . X0$

$Q2 = X1 . \bar{X0}$

Circuit diagrams follow directly from these equations

5.

A	B	>	<	A > B	A < B
x	X	0	1	0	1
x	X	1	0	1	0
x	X	1	1	0	0
0	0	0	0	0	0
0	1	0	0	0	1
1	0	0	0	1	0
1	1	0	0	0	0

A, B

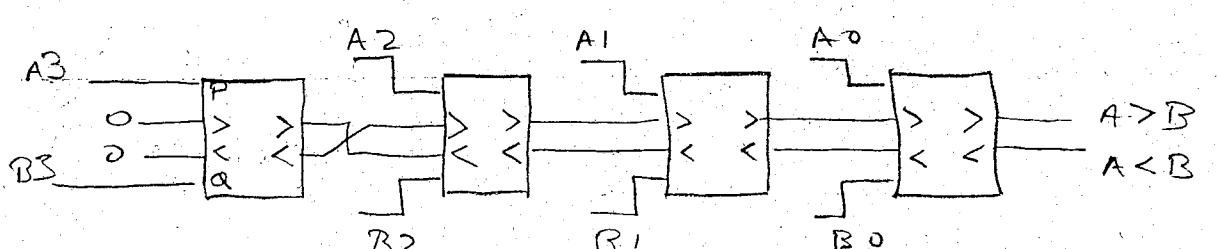
A>B	00	01	11	10
00	0	0	0	1
01	0	0	0	0
11	0	0	0	0
10	1	1	1	1

>, <

A, B

A<B	00	01	11	10
00	0	1	0	0
01	1	1	1	1
11	0	0	0	0
10	0	0	0	0

$A > B = > . \overline{<} + A . \overline{B} . \overline{<}$ $\quad A < B = \overline{>} . < + \overline{A} B . \overline{>}$



If A3 > B3 → A is negative, b positive ∴ A < B
If A3 < B3 → A is positive, b negative ∴ A > B
If A3 = B3 → result depends on unsigned comparison of A[2..0] with B[2..0].

Implemented using 3-layer logic, each comparator requires 3T seconds. Best case is A0/B0 comparison only, eg 0000/0001, corresponding to 3T seconds. Worst case is 4 × 3T seconds eg 1000/0000