IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2006

EEE/ISE PART I: MEng, BEng and ACGI

ANALYSIS OF CIRCUITS

Corrected Copy

Wednesday, 7 June 10:00 am

Time allowed: 2:00 hours

There are FOUR questions on this paper.

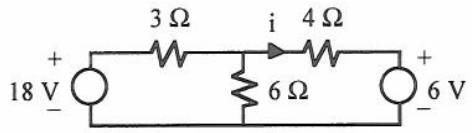
Q1 is compulsory.
Answer Q1 and any two of questions 2-4.
Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : D.G. Haigh,
Second Marker(s) : G. Weiss,

1 a) Use source transformations to determine the current i in the circuit in Figure 1(a):

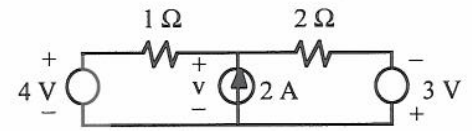
Figure 1(a)



[4]

b) Use the principle of superposition to find the voltage v in the circuit in Figure 1(b):

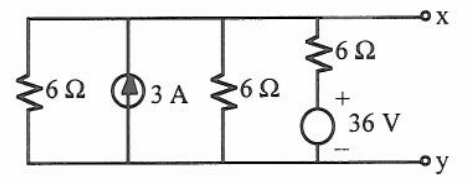
Figure 1(b)



[4]

c) For the sub-circuit in Figure 1(c), determine the Norton and Thevenin equivalent circuits; an approach based on determining short-circuit current and Thevenin resistance is suggested.

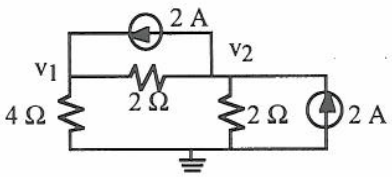
Figure 1(c)



[4]

d) Use nodal analysis to determine the nodal voltages v_1 and v_2 in the circuit in Figure 1(d):

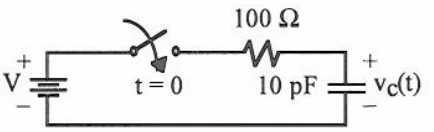
Figure 1(d)



[4]

e) The model in Figure 1(e) can be used to calculate delay introduced when two logic gates are interconnected. Assuming that the capacitor is initially uncharged, determine the capacitor voltage at a time 2 ns (i.e. 2×10^{-9} s) after the switch closes.

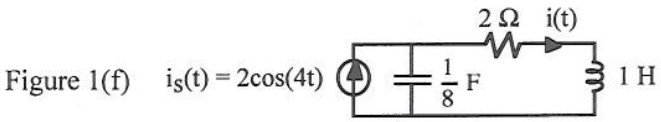
Figure 1(e)



[4]

f) Write the current $i(t) = 2\cos(4t)$ in phasor form. Write the impedances for a 1/8 F capacitor and a 1 H inductor at a frequency of 4 rad/s. Hence use the phasor method to determine the current $i(t)$ in the circuit in Figure 1(f):

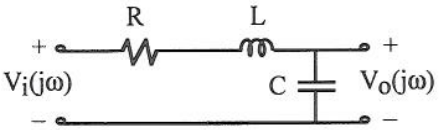
Figure 1(f)



[4]

g) For the filter circuit shown in Figure 1(g), determine the frequency response function $H(j\omega) = V_o(j\omega)/V_i(j\omega)$. By considering the behaviour of $H(j\omega)$ at zero frequency and for $\omega \to \infty$, determine the type of filter response.

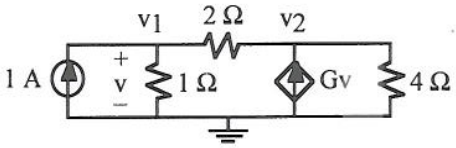
Figure 1(g)



[4]

h) The circuit shown in Figure 1(h) contains a voltage-controlled current source, $i_c = Gv$, where $G = 1$ S and v is defined in the figure. Write the nodal equations and determine the voltages v_1 and v_2. (Hint: Tape the dependent source, perform by-inspection nodal analysis of the circuit and un-tape the dependent source.)

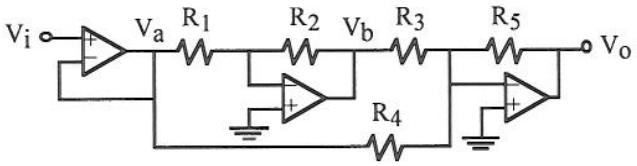
Figure 1(h)



[4]

i) In the circuit in Figure 1(i), determine the voltage V_o as a function of the voltage V_i and the five resistor values; it is suggested to use an informal method and first determine V_a and V_b:

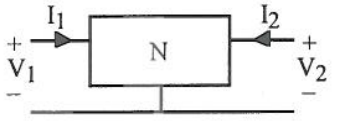
Figure 1(i)



[4]

j) A linear 2-port circuit with its 2-port admittance description is given in Figure 1(j). Determine, in terms of the Y-parameters y_{11}, y_{12}, y_{21} and y_{22}, expressions for (i) the voltage gain V_2/V_1 when port 2 is terminated in an open-circuit and (ii) the current gain I_2/I_1 when port 2 is terminated in a short-circuit.

Figure 1(j)



$$I_1 = y_{11}V_1 + y_{12}V_2$$
$$I_2 = y_{21}V_1 + y_{22}V_2$$

[4]

2 a) Write an expression relating the voltage $v_L(t)$ and current $i_L(t)$ for an inductor and an expression relating the voltage $v_C(t)$ and current $i_C(t)$ for a capacitor.

In the circuit in Figure 2.1(a), the current source $i_s(t)$ has the waveform shown in Figure 2.1(b). Plot the inductor voltage $v_L(t)$ showing its maximum and minimum values.

In the circuit in Figure 2.1(c), the capacitor voltage $v_C(t)$ has the waveform shown in Figure 2.1(d). Plot the source current $i_s(t)$ which causes this capacitor voltage, showing its maximum and minimum values.

State circuit models for the inductor and for the capacitor that can be used for DC analysis of a circuit containing these elements.

[9]

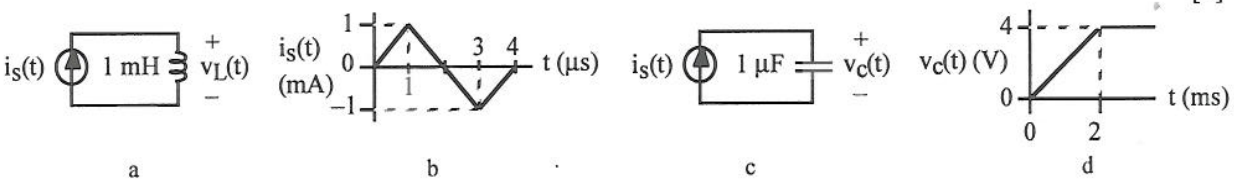


Figure 2.1 Circuits and signal waveforms for Question 2(a)

b) Consider the circuit in Figure 2.2. The switch spends a long time in position 1, allowing all voltages to settle. At time $t = 0$, the switch moves to position 2. Determine the following for $t \geq 0$:

i) The time constant that governs the capacitor voltage $v(t)$

ii) The initial value of $v(t)$ for $t \to 0$ and the final value of $v(t)$ for $t \to \infty$

iii) An expression for $v(t)$ as a function of t

iv) The value of $v(t)$ for $t = 2$ s.

[13]

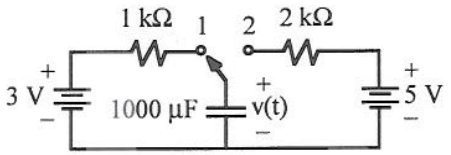


Figure 2.2 Circuit for Question 2(b)

c) Figure 2.3 shows a digital circuit fed by a 5 V DC power supply. The 2.5 μH inductor represents the total inductance in the power supply feed. During a switching transient that lasts for 1 ns, the supply current $i_s(t)$ increases by 1 mA changing at a constant rate. Determine the effective supply voltage $v_s(t)$ during the transient.

How could the change in effective supply voltage be reduced?

[8]

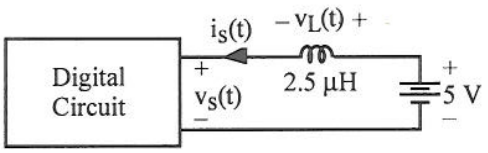


Figure 2.3 Circuit for Question 2(c)

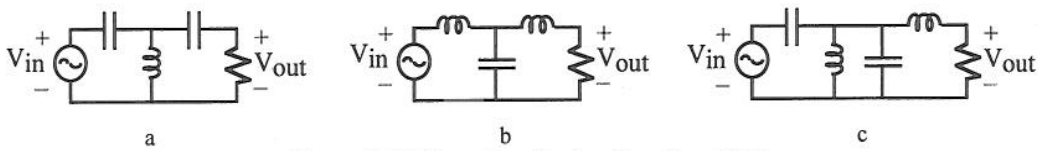
3. a) State expressions for the impedance of an inductor of value L and for the impedance of a capacitor of value C at a frequency ω.

Hence derive models for both the inductor and for the capacitor that may be used for the analysis of a circuit containing them at DC, i.e. when the frequency is zero.

Derive models for both the inductor and for the capacitor that may be used for analysis of a circuit containing them at very high frequencies, i.e. for $\omega \to \infty$.

Determine the frequency response function $V_{out}(j\omega)/V_{in}(j\omega)$ of the circuits in Figure 3.1 for $\omega = 0$ and for $\omega \to \infty$ and hence determine the type of response, such as lowpass.

[12]



a b c

Figure 3.1 Filter circuits for Question 3(a)

b) Select appropriate elements with values from the menu in Figure 3.2 and create simple 2-port circuits with the following frequency response functions V_{out}/V_{in} (the elements in Figure 3.2 may be assumed to be ideal):

i) 1st order RC lowpass filter with a cut-off frequency of 10 rad/sec

ii) 1st order CR highpass filter with a cut-off frequency of 10 krad/sec

iii) 2nd order RLC bandpass filter with a mid-band frequency of 10 Mrad/sec and a Q-factor of 10.

[9]

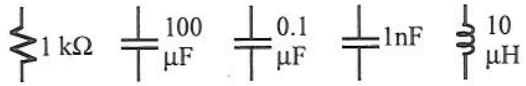


Figure 3.2 Circuit elements for Question 3(b)

c) Define the Q-factor for a reactive element (inductor or capacitor) in terms of energies for sinusoidal excitation.

Figure 3.3 shows a model for a practical inductor with the resistance r_s representing series losses and the resistance r_p representing parallel losses. Carry out the following:

i) Assuming that parallel loss is negligible, i.e. $r_p \to \infty$, state an expression for the Q-factor of the inductor and sketch it as a function of frequency.

ii) Assuming that series loss is negligible, i.e. $r_s = 0$, state an expression for the Q-factor of the inductor and sketch it as a function of frequency.

iii) Assuming that $Q(\omega)$ is very high, derive an approximate expression for the Q-factor of the inductor including series and parallel loss and sketch it as a function of frequency.

[9]

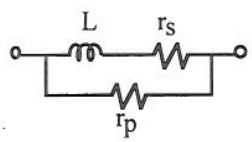


Figure 3.3 Inductor model for Questions 3(c)

4. a) Using elements from the menu of three circuit elements in Figure 4.1, show circuit diagrams with element values for circuits that implement the following circuit functions:

i) An inverting voltage amplifier with voltage gain –2 and input resistance 3 kΩ.

ii) A non-inverting voltage amplifier with voltage gain +3 and very high input resistance.

iii) A unity-gain voltage amplifier with input resistance 9 kΩ.

iv) A current-controlled voltage source with transresistance $R_T = -2$ kΩ, i.e. an input current 1 mA causes the output voltage to be –2 V.

[12]

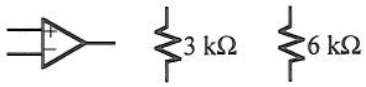


Figure 4.1 Circuit elements for Question 4(a)

b) i) State a simple stability criterion for circuits containing an operational amplifier (op-amp) and resistors in terms of the relative magnitude of the positive and negative feedback factors.

ii) The circuit in Figure 4.2 has a current source excitation. Determine whether the circuit is stable or unstable showing your calculations.

iii) If in the circuit of Figure 4.2 the current source excitation is replaced by a voltage source V_s, the circuit is unstable. Determine the minimum value of source resistance that needs to be inserted in series with V_s in order that the circuit is stable.

[9]

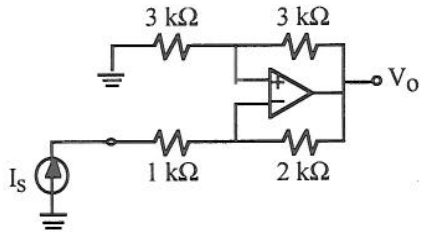


Figure 4.2 Circuit for Question 4(b)

c) i) Sketch a typical amplitude and phase response versus frequency for an op-amp's open-loop frequency response function $V_{out}/(V_+ - V_-)$.

ii) State the constant gain-bandwidth property for standard amplifier circuits that use an op-amp.

iii) Op-amps with the following gain-bandwidth product (GBP) are available:

Type	A	B	C
GBP (MHz)	1	10	100

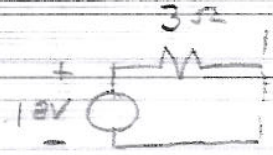
State which (if any) of these op-amp types are suitable for the following requirements (V_{out} and V_{in} refer to the amplifier circuit containing the op-amp):

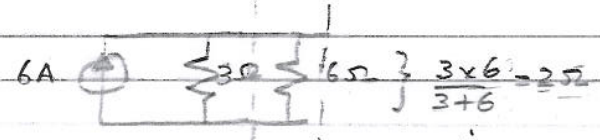
Specification	Gain $\lvert V_{out}/V_{in}\rvert$	Bandwidth
1	100	3 kHz
2	75	20 kHz
3	20	1 MHz
4	10	100 MHz

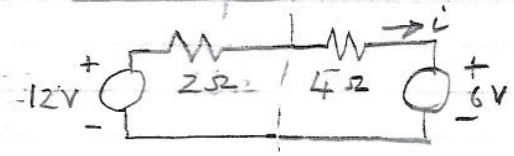
[9]

KEY
A Application
B Bookwork
T Theory

1(a) [A]

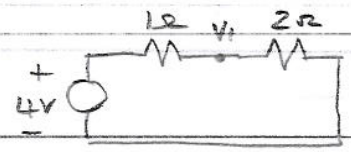




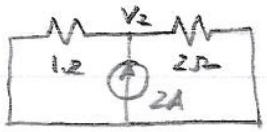


$i = \frac{12-6}{2+4} = 1\,A$

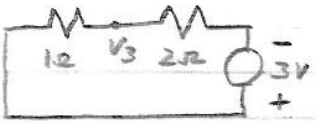
(b) [A]



$V_1 = 4 \times \frac{2}{1+2} = \frac{8}{3}\,V$



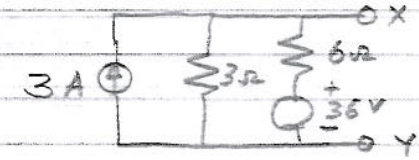
$V_2 = 2 \times \frac{1.2}{1+2} = \frac{4}{3}\,V$



$V_3 = -3 \times \frac{1}{1+2} = -1\,V$

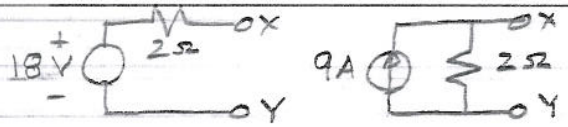
$V = V_1 + V_2 + V_3 = 3\,V$

(c) [A]



$i_{SC} = 3 + \frac{36}{6} = 9\,A$

$R_{th} = \frac{3\times6}{3+6} = 2\Omega \qquad V_{OC} = 12 \times 2 = 24\,V$



(d) [A]

$\frac{1}{4}V_1 + \frac{1}{2}(V_1 - V_2) = 2 \qquad \frac{3}{4}V_1 - \frac{1}{2}V_2 = 2$

$\frac{1}{2}V_2 + \frac{1}{2}(V_2 - V_1) = 0 \qquad -\frac{1}{2}V_1 + V_2 = 0$

$V_1 = 4\,V \qquad V_2 = 2\,V$

(e) [A]

$V_c(t) = V_{c0} + (V_{c\infty} - V_{c0})(1 - e^{-t/\tau})$

$= 0 + (5 - 0)(1 - e^{-t/\tau})$

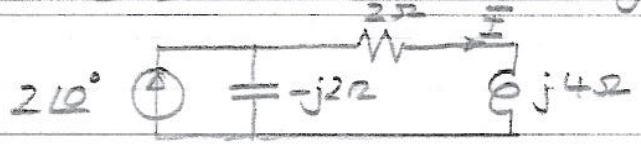
$= 5(1 - e^{-t/\tau})$

$\tau = 100 \times 10^{-11} = 10^{-9}\,s$

$V_c(t) = 5(1 - e^{-2})$

$= 4.323\,V$

1(f) $\bar{I} = 2\angle 0^\circ \quad Z_C = -j2\,\Omega \quad Z_L = j4\,\Omega$



[A] By current division: $\bar{I} = \frac{-j2}{2+j4-j2} \times 2\angle 0^\circ = \frac{-j2}{2+j2} \times 2$

$= \frac{2}{-1+j} = \frac{2}{\sqrt{2}\angle 135^\circ} = \sqrt{2}\angle -135^\circ$

$= -1-j$

$i(t) = \sqrt{2}\cos(4t - 3\pi/4)$

(g) Using voltage division:

$$\frac{V_o}{V_i} = \frac{1/(j\omega C)}{R + j\omega L + 1/j\omega C} = \frac{1}{1 + j\omega CR - \omega^2 LC} = H(j\omega).$$

[A] $H(j0) = 1$; $H(j\omega)|_{\omega \to \infty} = 0$

$\therefore$ the type of filter response is lowpass.

(h) Nodal equations with dependent source taped:

$$\begin{bmatrix} 1+1/2 & -1/2 \\ -1/2 & 1/2 + 1/4 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 1 \\ v \end{bmatrix}$$

[A] Untape source and rearrange, $v = V_1$:

$$\begin{bmatrix} 3/2 & -1/2 \\ -3/2 & 3/4 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

Add equations: $V_2(-1/2 + 3/4) = 1$; $V_2 = 4V$, $V_1 = 2V$

(i) $V_a = V_i$

$V_b = -\frac{R_2}{R_1} V_i$

[A] $V_o = -R_5\left(\frac{V_i}{R_4} - \frac{R_2}{R_1}\cdot\frac{1}{R_3}V_i\right) = -V_i R_5\left(\frac{1}{R_4} - \frac{R_2}{R_1 R_3}\right)$

(j) $I_1 = y_{11}V_1 + y_{12}V_2$

$I_2 = y_{21}V_1 + y_{22}V_2$

[T] (i) Open-circuit: $I_2 = 0$

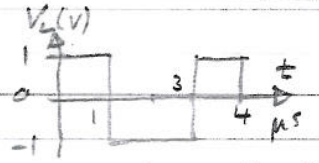
$0 = y_{21}V_1 + y_{22}V_2$; $\frac{V_2}{V_1} = -\frac{y_{21}}{y_{22}}$

(ii) Short-circuit $V_2 = 0$

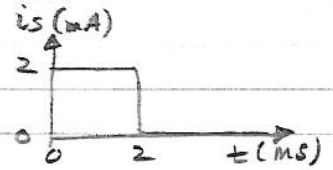
$\frac{I_2}{I_1} = \frac{y_{21}V_1}{y_{11}V_1} = \frac{y_{21}}{y_{11}}$

2(a) $v_L(t) = L\frac{di_L(t)}{dt}$ $\quad i_C(t) = C\frac{dv_C(t)}{dt}$

B + A



$v = L\frac{di}{dt} = 10^{-3}\cdot\frac{10^{-3}}{10^{-6}} = 1V$



$i = C\frac{dv}{dt} = 10^{-6}\cdot\frac{4}{2\cdot10^{-3}} = 2mA$

(9) DC models: Inductor $v_L = 0$ – short-circuit
Capacitor $i_C = 0$ – open-circuit

(b) i $\quad \tau = RC = 2.10^3 \times 10^{-3} = 2s$

ii $\quad V_C(0) = 3V$
$V_C(\infty) = 5V$

A

iii $\quad V(t) = V_{C\infty} + (V_{C\infty} - V_{C0})(1 - e^{-t/\tau})$
$= 3 + (5 - 3)(1 - e^{-t/\tau})$
$= 5 - 2e^{-t/\tau}$

iv $\quad V(2) = 5 - 2e^{-1}$
$= 4.264\ V$

(13)

(c) $\quad V_L(t) = L\frac{di_L(t)}{dt}$

A

$= 2.5.10^{-6} \times \frac{10^{-3}}{10^{-9}} = 2.5V$

$V_S(t) = 5 - V_L(t) = 2.5V$

(8) The reduction in supply voltage can be reduced by connecting a decoupling capacitor across the power supply to the digital circuit.

3(a) $Z_L = j\omega L$ $\quad Z_C = 1/(j\omega C)$

$\omega = 0$: $Z_L = 0$ s/c $\quad Z_C \to \infty$ o/c

B

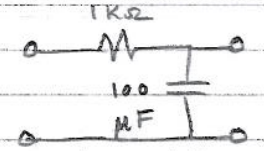
$\omega \to \infty$: $Z_L \to \infty$ o/c $\quad Z_C = 0$ s/c

+

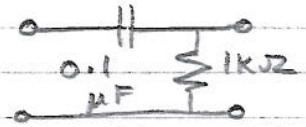
Circuit	$V_{out}/V_{in}(\omega=0)$	$V_{out}/V_{in}(\omega\to\infty)$	Type
a	0	1	HP
b	1	0	LP
c	0	0	BP

A

(12)

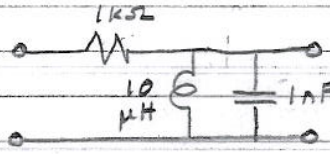
(b) (i) 

$\omega_1 = 1/RC = 1/0.1 = 10$ rad/sec

(ii) 

$\omega_2 = 1/RC = 1/10^{-4} = 10^4$ rad/sec

A

(iii) 

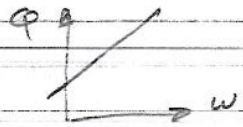
$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{10^{-5}\cdot 10^{-9}}} = 10^7$ rad/sec

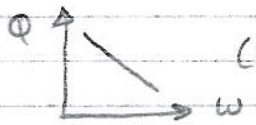
$\omega_0 L = 100\,\Omega \quad \therefore \quad Q = 10$

(9)

B + A

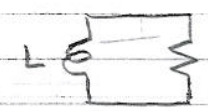
(c) $Q = 2\pi \times \frac{\text{peak stored energy}}{\text{energy dissipated per cycle}}$

(i) $Q_s = \frac{\omega L}{r_s}$ 

(ii) $Q_p = \frac{r_p}{\omega L}$ 

(log scales)

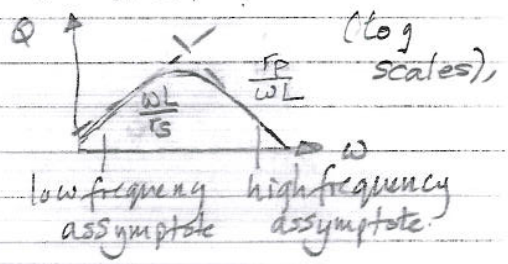
(iii) Convert series loss to parallel loss:



$r_s Q_s^2 = r_s \frac{\omega^2 L^2}{r_s^2} = \frac{\omega^2 L^2}{r_s}$

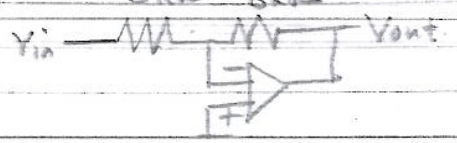
Total parallel resistance $r_{p(tot)} = \left(\frac{1}{r_p} + \frac{r_s}{\omega^2 L^2}\right)^{-1}$

Q factor $= \frac{r_{p(tot)}}{\omega L} = \frac{1}{\frac{\omega L}{r_p} + \frac{r_s}{\omega L}}$

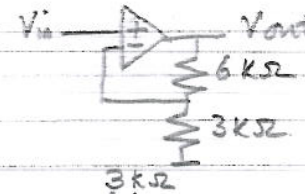


(9)

4 (a) i)

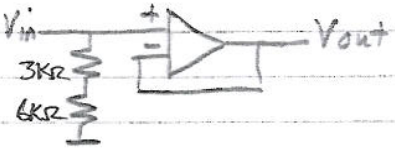


ii).

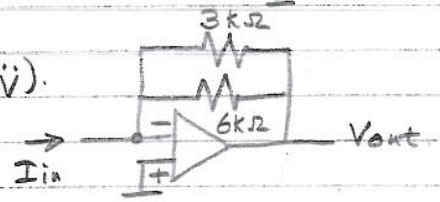


A

iii)



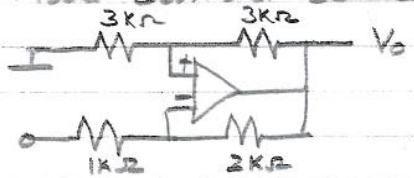
iv).



(12)

B b). i) For stability, magnitude of negative feedback should exceed positive feedback.

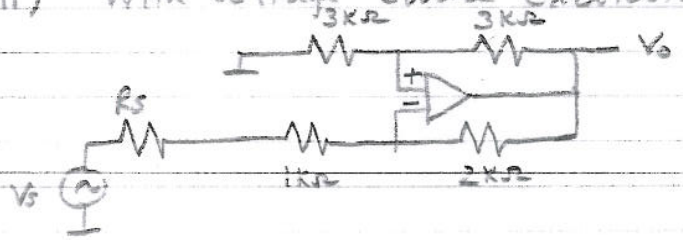
ii). Deactivate current source



\+

A $F_+ = \frac{1}{2}$ $F_- = 1$ $F_- > F_+$ ∴ Circuit is stable

iii) With voltage source excitation and R_S.



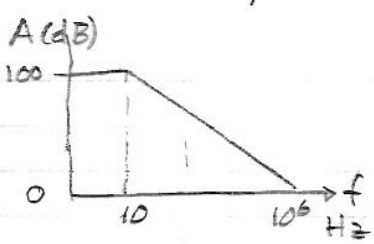
Deactivate voltage source.
Then

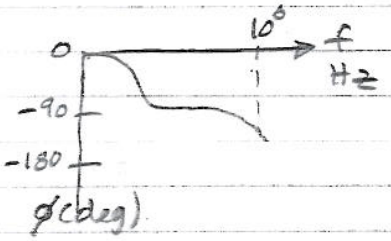
$$F_- = \frac{R_S + 1}{R_S + 1 + 2}, \quad R_S \text{ in K}\Omega.$$

For $F_- = F_+ = \frac{1}{2}$, $R_S = 1\text{K}\Omega$

(9) ∴ $R_S(\text{min}) = 1\text{K}\Omega$.

B c) i)





\+

A

ii) Product of closed-loop gain and bandwidth constant for op-amp amplifier circuits e.g. Figs 4(a) i, ii

iii)

specification	GBP	Suitable OA types
1	300 KHz	A, B, C
2	1.5 MHz	B, C
3	20 MHz	C
4	1 GHz	None

(9)