2010 Electronic and Electrical Fundamentals

Intermediate 2

Finalised Marking Instructions

Marks

Section A

Attempt all the questions in this section (50 marks)

1. Convert the following numbers.

(*a*) $1F_{16}$ Hexadecimal to Decimal

(*b*) 126_{10} Decimal to Binary

(*c*) 10011110_2 Binary to Hexadecimal

Answers

(*a*) 31_{10} **1**

(*b*) 01111110_2 **1**

(*c*) $9E_{16}$ **1**

(3)

2. With reference to Figures Q2*(a)*, *(b)* and *(c)*, identify the components shown and state one application for each.

(*a*)

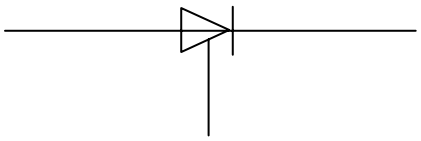


Figure Q2*(a)*

(*b*)

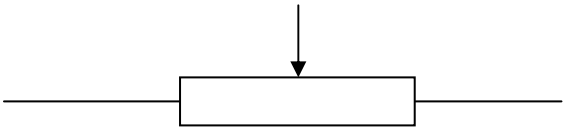


Figure Q2*(b)*

(*c*)

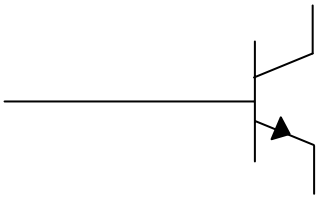


Figure Q2*(c)*

Answers

(*a*) Thyristor (power control (dc), rectification) **2**

(*b*) Resistor (moving contact), (control circuits, power control) **2**

(*c*) Bipolar transistor or npn transistor (amplifying, switching applications) **2**

(6)

Marks

3. In the diagram Figure Q3*(a)*, shown below, an iron ring has been placed in a magnetic field and the field pattern has been plotted.

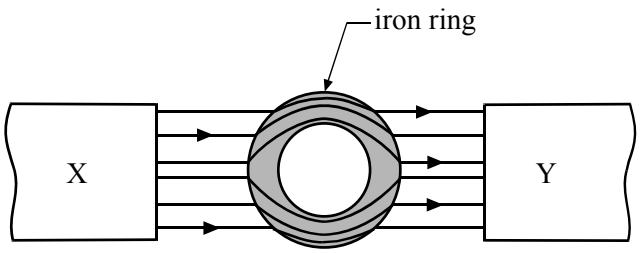


Figure Q3(*a*)

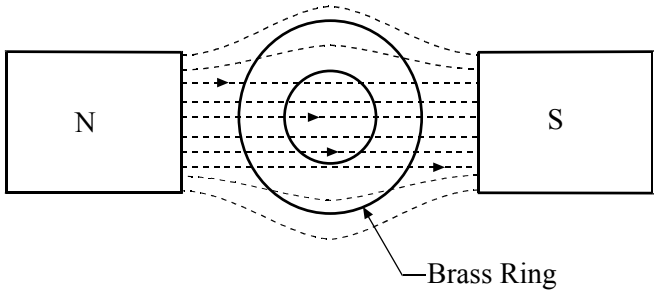
(*a*) Identify the magnetic pole **X**.

(*b*) Draw the field pattern obtained when the iron ring is replaced by a brass ring.

Answers

(*a*) North pole **1**

(*b*)



2

(3)

Marks

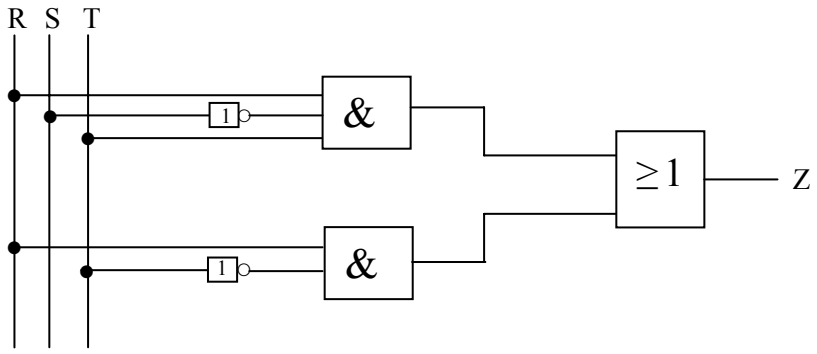
4. Draw, using BS symbols, the logic diagrams for the following expressions.

(*a*) $Z = R.\overline{S}.T + R.\overline{T}$

(*b*) $Z = \overline{A + \overline{B} + C} \ . \ \overline{\overline{A} + \overline{B} + C}$

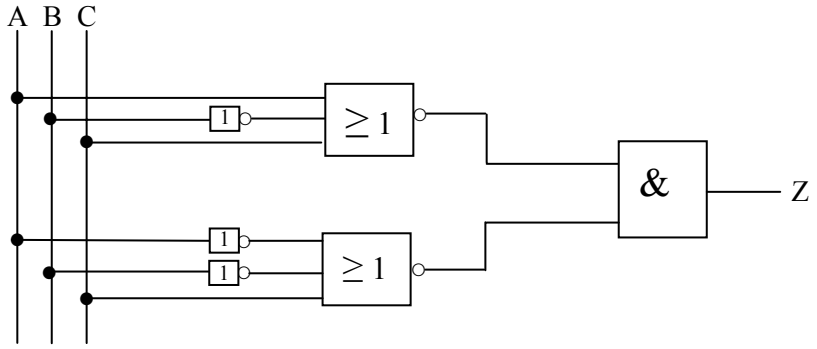
Answers

(*a*)



3

(*b*)



3

(6)

Marks

5. With reference to Figure Q5 and the data sheets provided, determine:

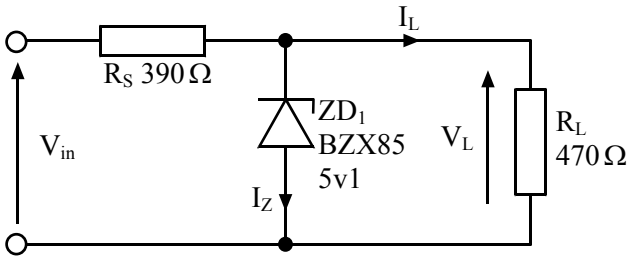


Figure Q5

(*a*) the maximum power the Diode, ZD_1 can handle;

(*b*) the maximum current in the Diode ZD_1;

(*c*) the load current I_L when $V_L = 5{\cdot}1$ V;

(*d*) the maximum permitted value of supply voltage.

Answers

(*a*) Maximum power = 1·3 W **1**

(*b*) $I_{Zmax} = \dfrac{P}{V} = \dfrac{1300}{5{\cdot}1} = 255$ mA **2**

(*c*) $I_L = V_L/R_L = 5{\cdot}1/470 = 10{\cdot}9$ mA **2**

(*d*) $V_{max} = ((I_{Zmax} + I_L) \times R_S) + V_L$
$= ((255\text{ mA} + 10{\cdot}9\text{ mA}) \times 390) + 5{\cdot}1$
$= 103{\cdot}7 + 5{\cdot}1 = 108{\cdot}8$ V **3**

(8)

Marks

6. (*a*) State the formula for determining the force on a current carrying conductor.

(*b*) A current carrying conductor is placed between the poles of a magnet. The length of the conductor in the magnetic field is 500 mm and the magnetic flux density is 0·5 Tesla.

If the force on the conductor is 5 Newtons calculate the current in the conductor.

(*c*) The formula for determining the voltage generated when a current carrying conductor is moved in a magnetic field is E = BLV.

Determine the voltage generated if the velocity of the conductor is 4 m s^{-1}, the field strength is 0·5 T and the length of the conductor is 5 m.

Answers

(*a*) F = BLI **1**

(*b*) I = F/BL
I = 5/0·5 × 0·5
I = 5/0·25
I = 20 A **2**

(*c*) E = BLV
E = 0·5 × 5 × 4
E = 10 V **2**

(5)

Marks

7.

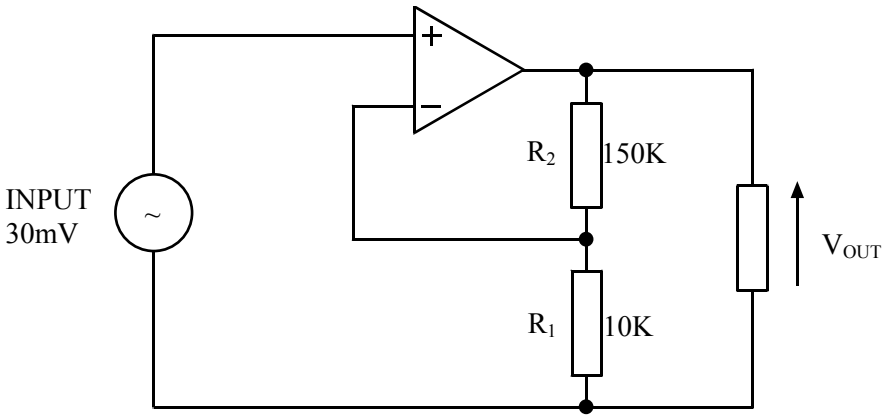


Figure Q7

The circuit shown in Figure Q7 is an operational amplifier with the ± 15 V supplies omitted for clarity.

(*a*) Name the circuit configuration shown in Figure Q7.

(*b*) Calculate the gain of the circuit.

(*c*) Calculate the output voltage.

Answers

(*a*) Non inverting (Amplifier) **1**

(*b*) Gain = $1 + (R_2/R_1) = 1 + 150/10 = 16$ **2**

(*c*) $V_{out} = V_{in} \times \text{Gain} = 30 \text{ mV} \times 16 = 480 \text{ mV}$ **2**

(5)

Marks

8.

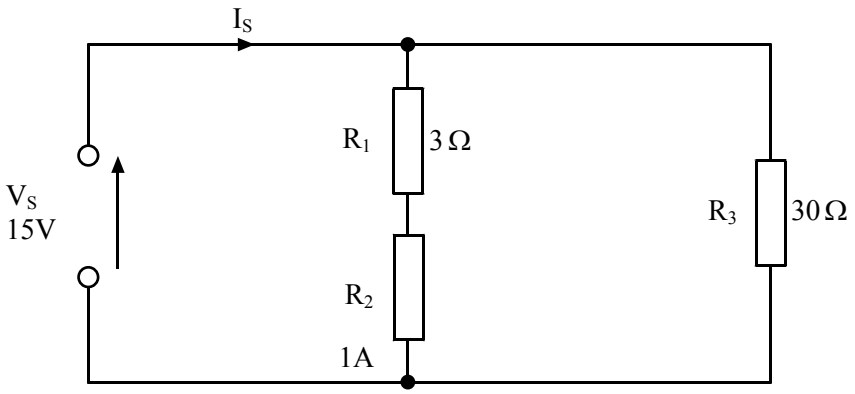


Figure Q8

For the circuit shown in Figure Q8 determine:

(*a*) the current in the resistor R_3;

(*b*) the supply current I_S;

(*c*) the voltage across the resistor R_1;

(*d*) the value of the resistor R_2;

(*e*) the total circuit resistance.

Answers

(*a*) $I = V/R = 15/30 = 0{\cdot}5$ A **2**

(*b*) $I_S = I_{R_3} + I_{R_1}$
$I_{R3} + I_{R1} = 0{\cdot}5 + 1 = 1{\cdot}5$ A **1**

(*c*) $V = I \times R = 1 \times 3 = 3$ V **1**

(*d*) $R_2 = V_{R_2}/I = (V_S - V_{R_1})/I = (15 - 3)/1 = 12\ \Omega$ **2**

(*e*) $R_T = (R_1 + R_2)//R_3 = (3 + 12)//30 = 15//30 = (15 \times 30)/15 + 30 = 450/45 = 10\ \Omega$ **2**

(8)

9. A high pressure gas test can only be carried out when the following conditions are met and there is a logic "1" at the output of the control circuit.

- The explosion proof door (A) is closed and locked (logic 1)
- The warning beacon (B) has been activated (logic 1)
- The emergency stop (C) has not been pressed (logic 0)

(*a*) Determine the logic expression for the control circuit.

(*b*) Draw the truth table for the expression.

(*c*) Draw the logic diagram for the control circuit.

Answers

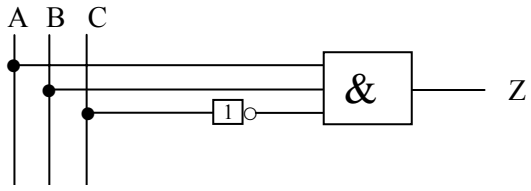
(*a*) $Z = A.B.\overline{C}$ **2**

(*b*)

A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

2

(*c*)



2

ASCI symbols also acceptable **(6)**

Section B

Attempt any TWO questions in this section (50 marks)
Each question is worth 25 marks

10. (*a*) Add the following binary numbers.

$1010_2 + 1110_2$

Answer

(*a*) $1010_2 + 1110_2 = 11000_2$ **2**

Marks

(*b*) Using Worksheet Q10(*b*) and the supplied datasheet for the circuit shown in Figure Q10(*b*) below, draw the logic circuit diagram on the worksheet and label all gate inputs and outputs with the appropriate pin connections.

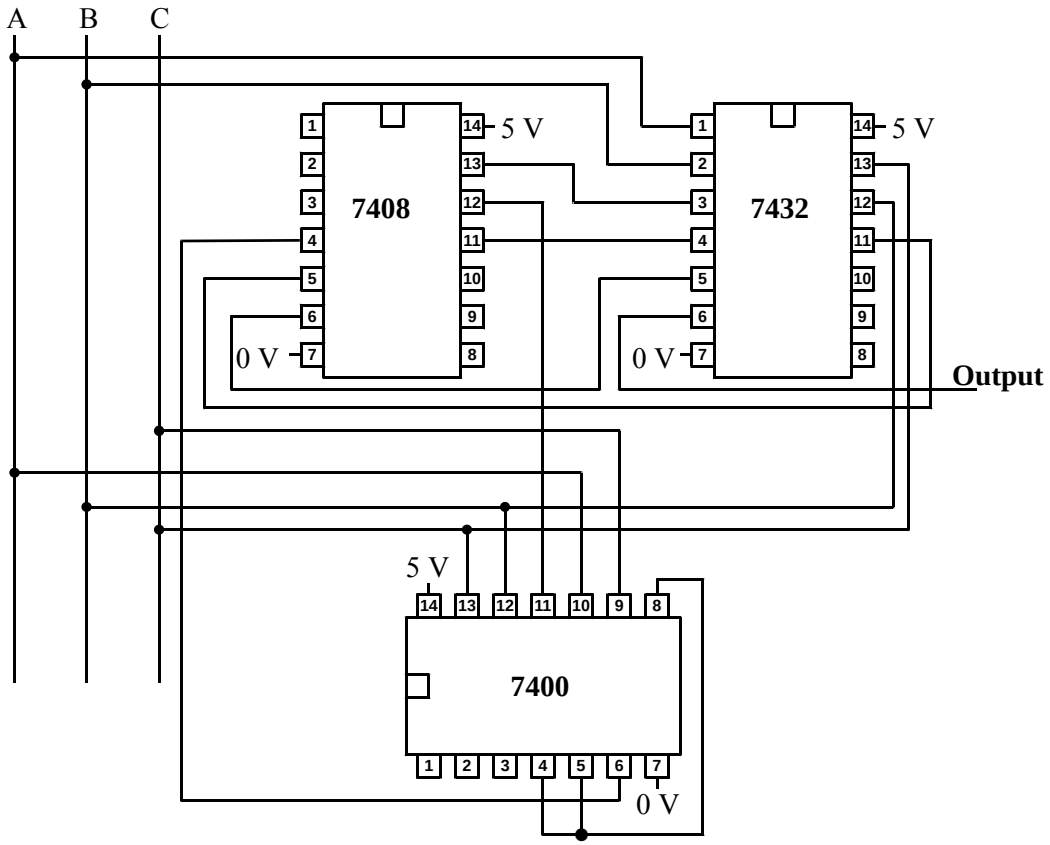
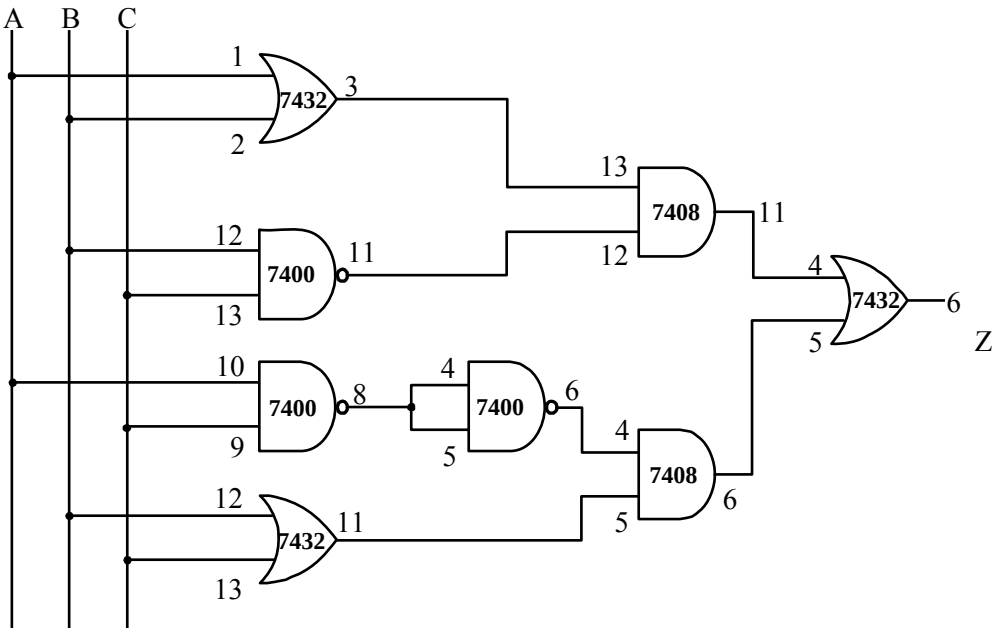


Figure Q10(*b*)

Answer

(*b*)



8

(*c*) Using Worksheet Q10(*c*) for the circuit shown in Figure Q10(*c*) below:

(i) determine the circuit Boolean expression;

(ii) complete the circuit truth table on the Worksheet.

(iii) A fault condition causes pin 11 on the 7400 to be permanently low. State what type of gate could replace the complete circuit under this fault condition. You must explain your answer.

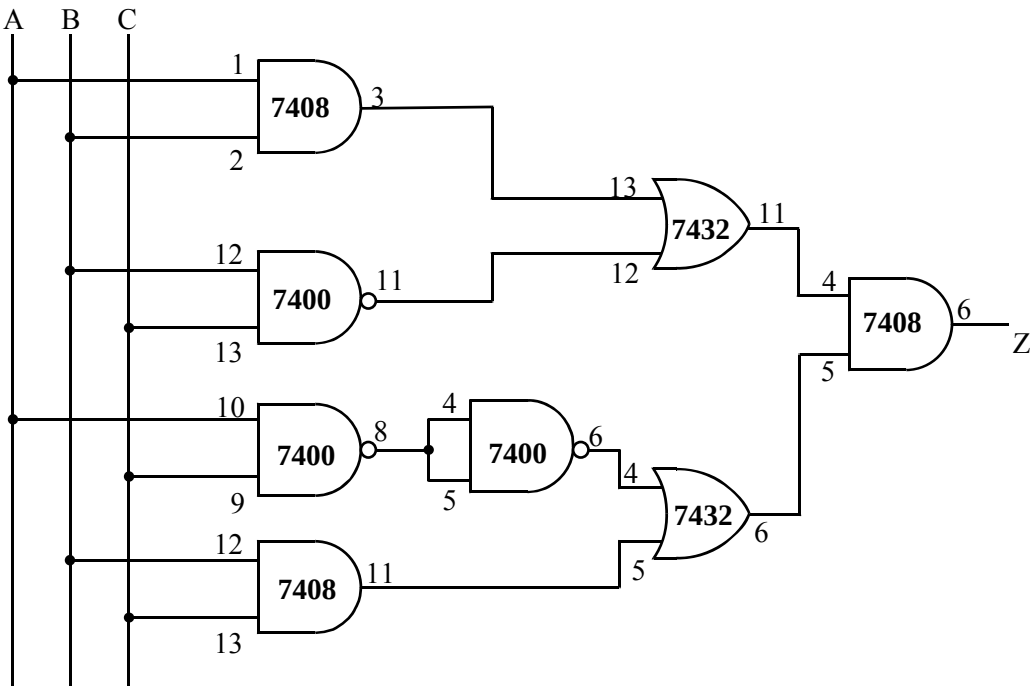


Figure Q10(*c*)

Answers

(*c*) (i) $Z = (A.B + \overline{B.C}).(A.C + B.C)$ **3**

(ii)

INPUTS			GATE OUTPUTS								
A	B	C	7408 Pin 3	7400 Pin 11	7400 Pin 8	7408 Pin 11	7400 Pin 6	7432 Pin 11	7432 Pin 6	7408 Pin 6	Fault condition
0	0	0	0	1	1	0	0	1	0	0	0
0	0	1	0	1	1	0	0	1	0	0	0
0	1	0	0	1	1	0	0	1	0	0	0
0	1	1	0	0	1	1	0	0	1	0	0
1	0	0	0	1	1	0	0	1	0	0	0
1	0	1	0	1	0	0	1	1	1	1	0
1	1	0	1	1	1	0	0	1	0	0	0
1	1	1	1	0	0	1	1	1	1	1	1

8

(iii) When Pin 11 is low on 7400 this means pin 4 on the 7408 can only be high when A.B is high. This in turn causes Z to be low when the input is 101. This leaves the truth table as per the 'Fault' column in (iii) and this is a 3-input AND gate. **4**

(25)

Marks

11. (*a*) For the diagram shown in Figure Q11(*a*) below, determine:

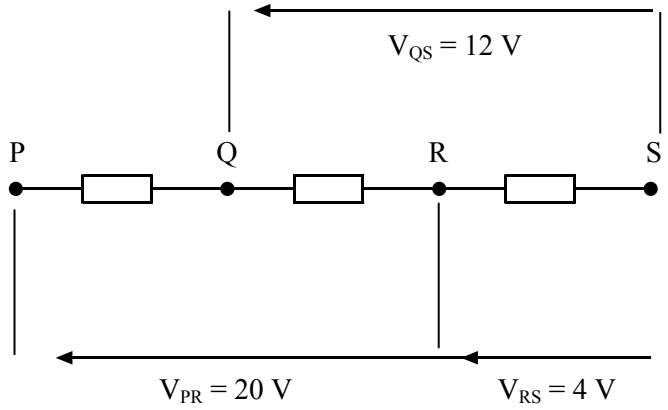


Figure Q11(*a*)

(i) the voltage V_{QR};

(ii) the voltage V_{PQ}.

(*b*) For the circuits shown in Figure Q11(*b*) below, determine:

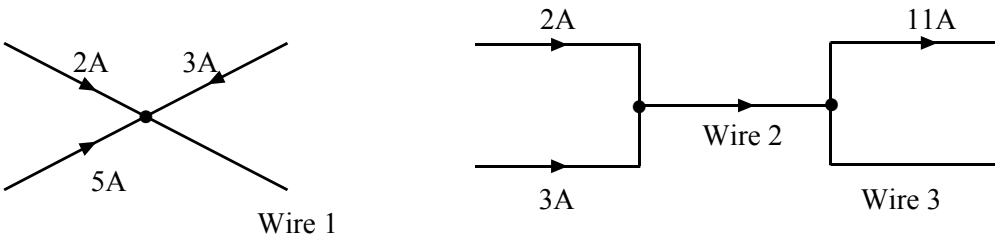


Figure Q11(*b*)

(i) the size and the direction of the current in wire 1;

(ii) the size of the current in wire 2 and wire 3.

Answers

(*a*) (i) V_{QR} = 8V **2**

(ii) V_{PQ} = 12V **2**

(*b*) (i) Wire 1 has 10A flowing away from the junction **2**

(ii) Wire 2 has 5A and Wire 3 has 6A **2**

Marks

(*c*) For the circuit shown in Figure Q11(*c*) below, the variable resistor can be varied between 5 Ω and 15 Ω. It is initially set at 10 Ω.

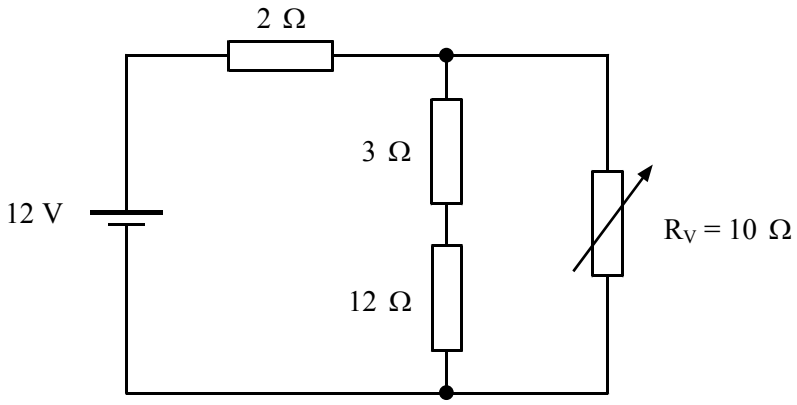


Figure Q11(*c*)

(i) Show that the total circuit resistance is 8 Ω.

Determine:

(ii) the supply current;

(iii) the voltage across the 2 Ω resistor;

(iv) the voltage across the 10 Ω resistor (R_V);

(v) the current through the 10 Ω resistor (R_V);

(vi) the power dissipated by the circuit;

(vii) the energy consumed in five minutes;

(viii) the value that R_V should be set to for minimum circuit current;

(ix) the value that R_V should be set to for maximum circuit power.

Answers

(*c*) (i) $R_t = 2 + 15//10 = 8\ \Omega$ **2**

(ii) $I_S = \frac{V_S}{R_t} = \frac{12}{8} = 1{\cdot}5\text{A}$ **1**

(iii) $V_{2\Omega} = 1{\cdot}5 \times 2 = 3\text{V}$ **1**

(iv) $V_{10\Omega} = V_{15\Omega} // V_{10\Omega} = 1{\cdot}5 \times 6 = 9\text{V}$ **3**

(v) $I_{10\Omega} = V_{10\Omega}/R = 9/10 = 0{\cdot}9\text{A}$ **2**

(vi) $\text{Power} = I_S^2 R_t = 1{\cdot}5^2 \times 8 = 18\text{W}$ **2**

(vii) $\text{Energy} = Pt = 18 \times 5 \times 60 = 5400\text{J}$ **2**

Marks

(viii) Minimum I_S occurs when R_t is a maximum.

Hence R_V should be set to 15 Ω **2**

(ix) Maximum power occurs when I_S is a maximum. This occurs when R_t is a minimum.

Hence R_V should be set to 5 Ω **2**

(25)

12. For the circuit shown in Figure Q12(*a*) below, the variable resistor (R_V) can be varied between 1 kΩ and 100 kΩ.

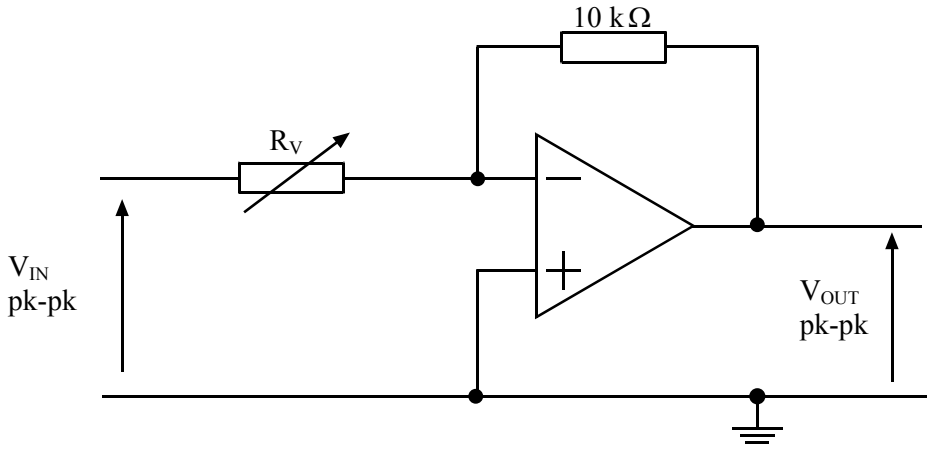


Figure Q12(*a*)

(*a*) Determine the value of R_V required to obtain the following.

(i) Maximum V_{OUT}

(ii) Minimum V_{OUT}

(iii) V_{OUT} (pk-pk) = V_{IN} (pk-pk).

(*b*) When the output voltage is 3·4 V pk-pk and the input voltage is 1·36 V pk-pk determine:

(i) the value of R_V to obtain this output voltage;

(ii) the rms value of V_{OUT}.

Answers

(*a*) (i) Maximum V_{OUT} when R_V = 1 kΩ **2**

(ii) Minimum V_{OUT} when R_V = 100 kΩ **2**

(iii) V_{OUT} (pk-pk) = V_{IN} (pk-pk) when R_V = 10 kΩ **2**

(*b*) (i) Required gain is 3·4/1·36 = 2·5

Hence R_V = 10/2·5 = 4 kΩ **2**

(ii) V_{rms} = 0·707Vpk = 0·707 × 1·7 = 1·2 V **2**

Marks

(*c*) For the circuit shown in Figure Q12(*c*) below;

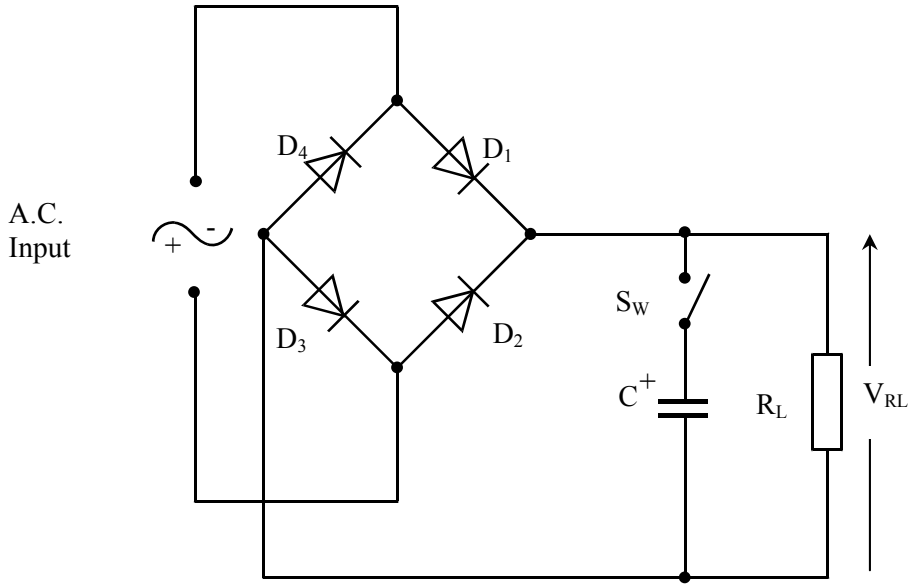


Figure Q12(*c*)

(i) explain the purpose of the diode arrangement in terms of load current;

(ii) explain why the polarity of V_{RL} is always the same.

Sketch the waveform for the voltage across V_{RL} (neglecting diode voltdrops) when the switch is:

(iii) open;

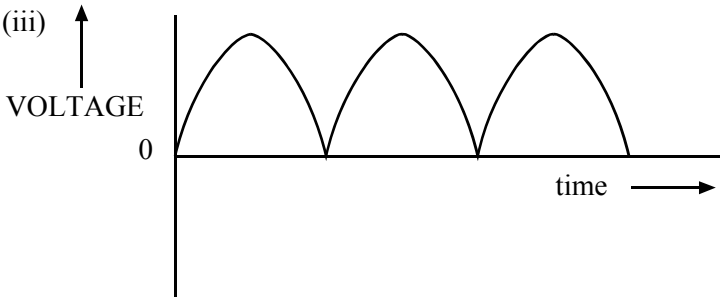
(iv) closed.

Answers

(*c*) (i) The purpose of the diode arrangement is to provide V_{RL} with the same current direction for both +ve and –ve input cycles. **2**

(ii) Polarity is the same because current direction is the same. **2**

(iii)



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(iv)

2

(*d*) For the circuit shown in Figure Q12(*d*) below:

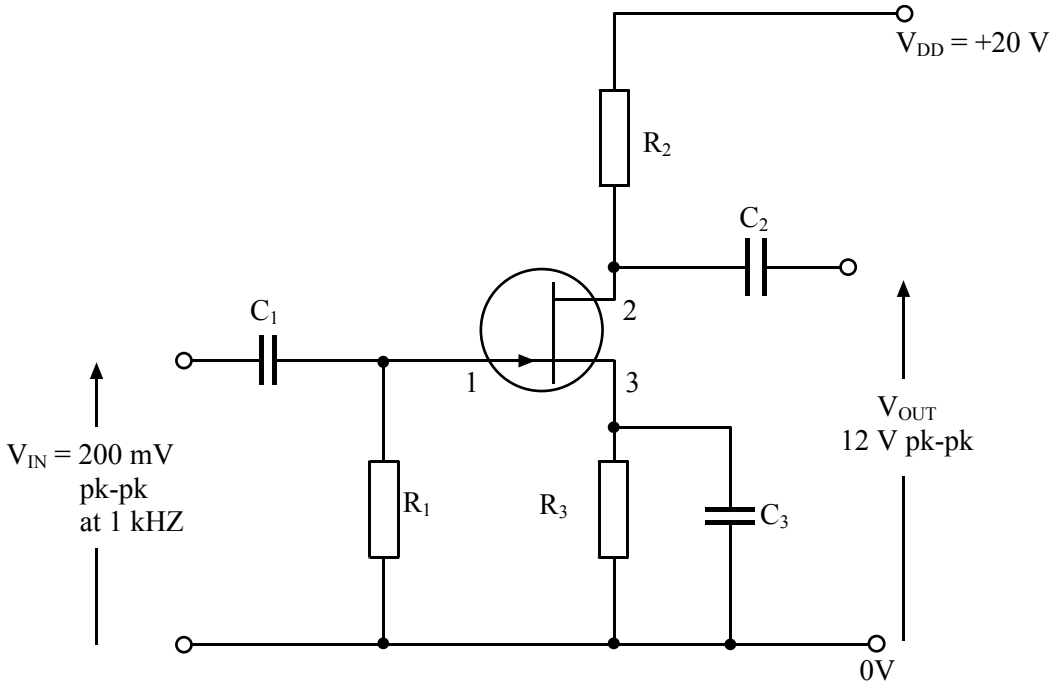

Figure Q12(*d*)

(i) identify the circuit configuration;

(ii) identify the transistor terminals 1, 2 and 3;

(iii) determine the circuit gain;

(iv) state the purpose of capacitor C_1.

Answers

(*d*) (i) FET amplifier **2**

(ii) 1 = Gate, 2 = Drain, 3 = Source **3**

(iii) Gain = 12/0·2 = 60 **1**

(iv) Coupling capacitor **1**

(25)

[END OF MARKING INSTRUCTIONS]