Detailed Solutions A- 09 JUNE 2003

Q1. a. C The pole locations are mirror image symmetric to location of the zeros. Therefore it is an all-pass filter.

b. C The outputs of the first level NAND gates are $\overline{AB}$ and $\overline{BC}$.
The output of the first OR gate is $\overline{AB} + \overline{BC}$.
Thus, the output $Y = \overline{A} + \overline{AB} + \overline{BC} + \overline{C}$.

c. B FFFF is a negative 2's complement number. To obtain its magnitude, complement it and add 1 to obtain hexadecimal 0001 which is equal to decimal 1.

d. A The output of the counter stabilizes after the effect of an input pulse has rippled through all 10 flipflops of the counter, which requires a time equal to 10τ, where τ is propagation delay time of one flipflop. Now, $10\tau < 10^{-6}$, and therefore $\tau < 10^{-7}$s.

e. A By virtual ground the voltage at the –ve terminals of the two Op Amps are 1V and 2V respectively. Let the output voltage of the first Op Amp be V_a. Then, KCL at the –ve terminal of first OpAmp gives

$$\frac{0-1}{2K} + \frac{V_a - 1}{2K} + \frac{2-1}{2K} = 0, \text{ or } V_a = 0V.$$

Also, KCL at the –ve terminal of second Op Amp gives

$$\frac{0-2}{2K} + \frac{1-2}{1K} + \frac{V_o - 2}{1K} = 0, \text{ or } V_o = 8V.$$

f. C

g. C Refer to p.360 [2].

h. D Refer Section 7.15 [2]

PART I

Q2. a. By virtual ground the voltage at the –ve terminals of the two OpAmps are $\frac{V_o}{8}$ and 1V respectively. Assume that V_a is the voltage at output of the first OpAmp Then, KCL at the –ve terminal of first OpAmp gives

$$\frac{1 - \frac{V_o}{8}}{1K} + \frac{V_a - \frac{V_o}{8}}{2K} = 0, \text{ or } V_a = \frac{3V_o}{8} - 1.$$

KCL at the –ve terminal of second OpAmp gives

$$\frac{V_o - 1}{8K} + \frac{V_a - 1}{4K} = 0, \text{ or } V_a = \frac{3 - V_o}{2}.$$

Eliminating V_a from the two equations, $V_o = \frac{20}{7}$ volts.

b. For compensation, refer Section 14.8 [2].
c. For Sawtooth generation, refer Section 15.13 [2].

Q3. Refer Sections16.2, 16.13, 16.14 [2].

Q4.a. By virtual ground the –ve terminal of the OpAmp is at virtual ground. Therefore, the current drawn by the T-network composed of R, 2C, R (call it T1) is

$$I_a = \left[\frac{V_a}{R}\right] \Big/ \left[1 + \frac{1}{1 + 2sCR}\right] = \frac{V_a(1 + 2sCR)}{2 + 2sCR}.$$

The current going out of T1 towards –ve terminal of the OpAmp is

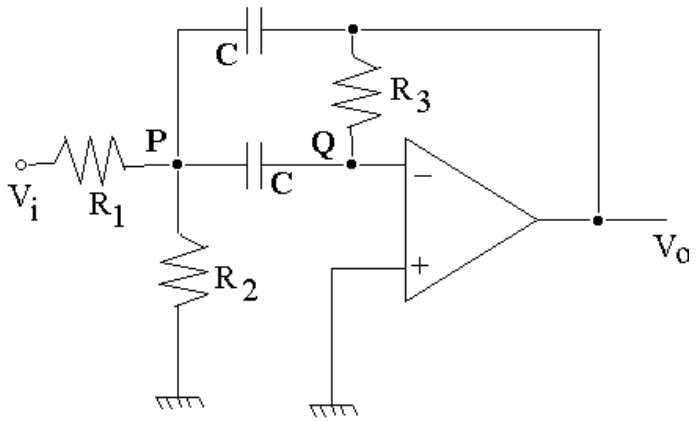
$$I_1 = I_a / [1 + 2sCR] = \frac{V_a}{2 + 2sCR}.$$

Similarly, the current going towards –ve terminal of the OpAmp from the second T-network can be written as

$$I_2 = \frac{Rs^2C^2V_a}{2 + 2sCR}.$$

Applying KCL at –ve terminal of the OpAmp gives $I_1 + I_2 = 0$. Simplifying this identity gives the desired result.

b. The node equations at nodes P and Q in the figure shown will be



$$\frac{V_i - V_p}{R_1} = \frac{V_p}{R_2} + (V_p - V_o)sC + V_p sC \qquad \text{and} \qquad V_p sC = \frac{-V_o}{R_3}$$

Eliminating V_p and letting $R' = R_1 \| R_2$, gives the transfer function as

$$\frac{V_o}{V_a} = \frac{(1/R_1C)s}{s^2 + (2/R_3C)s + (1/R'R_3C^2)} \qquad (4b.1)$$

A standard bandpass filter transfer function can be written as

$$\frac{V_o}{V_a} = \frac{A_0(\omega_0/Q)s}{s^2 + (\omega_0/Q)s + \omega_0^2}, \qquad (4b.2)$$

where A_0 is the midband gain. Equating the corresponding coefficients gives

$$R_1 = \frac{Q}{-A_0\omega_0 C}, \qquad R_3 = \frac{2Q}{\omega_0 C}, \qquad R' = \frac{1}{\omega_0^2 R_3 C^2}$$

From the data given, $\omega_0 = 4000\pi$, $A_0 = 20$, $Q = \frac{40}{3}$. Choosing C=10^{-7}F, gives

$$R_1 = \frac{10^4}{6\pi}, \qquad R_3 = \frac{10^6}{15\pi}, \qquad R_2 = \frac{R_1R'}{R_1 - R'} = \frac{1}{0.3994\pi}$$

Q5.a. For Dual-slope converters, refer to Section 16.5 [2].

b. Resolution = $\frac{12}{2^{12}} = \frac{12}{4096}$ volts, Weightage of MSB = 2^{11}, and

Input voltage corresponding to all 1's at the output = $12(1 - 2^{-12}) \approx 11.997$ volts.

Q6.a. The gain of the RC network of the given oscillator circuit can be obtained as

$$Gain(s) = \frac{R}{3R + \left(\frac{1}{sC} + R^2 sC\right)}.$$

Thus, the loop gain of the oscillator is

$$LG(s) = \left(1 + \frac{R'}{R}\right) Gain(s) = \frac{R\left(1 + \frac{R'}{R}\right)}{3R + \left(\frac{1}{sC} + R^2 sC\right)}$$

At the frequency of oscillation ω_0 , $LG(j\omega_0) = 1\angle 0^\circ$, which gives

$$\omega_0 = \frac{1}{RC} \quad and \quad \frac{R\left(1 + \frac{R'}{R}\right)}{3R} = 1 \quad or \quad R' = 2R$$

b. Refer to Section 8.8 [3] for derivation of the propagation delay time given by

$$t_{PHL} = \frac{C_{load}}{k_N}\left[\frac{V_{DD} - V_{GS} + V_T}{(V_{GS} + V_T)^2} + \frac{1.15}{(V_{GS} + V_T)}\right]$$

Substituting the values from given data gives $t_{PHL} = 0.175\mu s$.

PART II

Q7.a. From the description of the problem

$$F(A,B,C,D) = \sum 0,2,5,6,13,14 + \sum_{\phi} 8,9$$

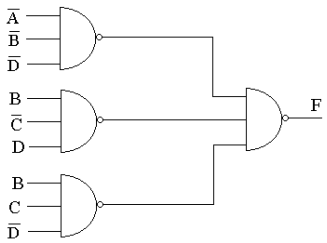
The K-map for $F(A,B,C,D)$ can be written as

CD \ AB	00	01	11	10
00	1	0	0	X
01	0	1	1	X
11	0	0	0	0
10	1	1	1	0

Combining the terms gives the minimized function as

$$F(A,B,C,D) = \overline{A}\,\overline{B}\,\overline{D} + B\,\overline{C}\,D + B\,C\,\overline{D}$$

which can be realized using four 3- input NAND gates as



b. From the figure of the counter, the required table can be written as

PS			NS								
Q_0	Q_1	Q_2	Q_0	Q_1	Q_2	J_0	K_0	J_1	K_1	J_2	K_2
0	0	0	1	0	0	1	1	0	1	0	0
1	0	0	0	1	0	1	1	1	1	0	0
0	1	0	0	0	1	0	1	0	1	1	1
0	0	1	1	0	1	1	1	0	1	0	0
1	0	1	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	0	1	1	1	1	1

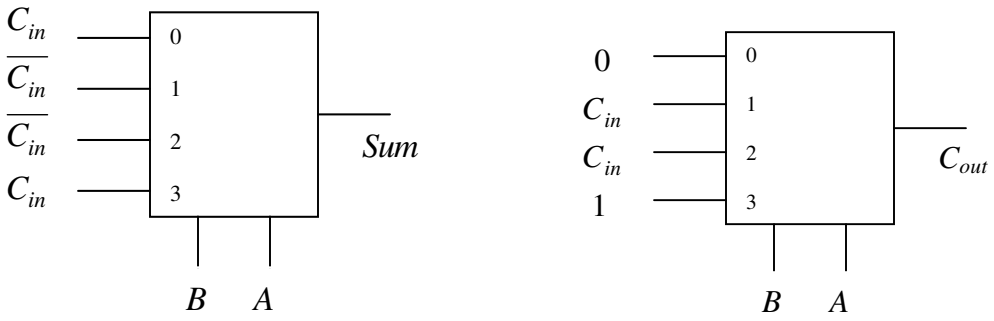
From the table, the modulus of the counter is 6.

Q8.a. The full adder functions can be written as

$$Sum = A \oplus B \oplus C_{in} = A\overline{B}\,\overline{C_{in}} + \overline{A}B\,\overline{C_{in}} + AB\,C_{in} + \overline{A}\,\overline{B}\,C_{in}$$

$$C_{out} = AB + B\,C_{in} + C_{in}\,A$$

which can be realized with two 4-1 multiplexers as shown below. The inputs to the multiplexers are the residues of the two functions. For example, when *B=A=0*, the residues are *Sum=*C_{in} and C_{out}=0.



Q8.b. To implement F_1, F_2, F_3 using a ROM requires the ROM to have three outputs. Since the functions are of four variables, the ROM is required to have 2^4=16 Locations. Thus, the size of the ROM is 16x3. The data in the ROM is as per the Truth-table of the functions as shown below, where x means 0 or 1.

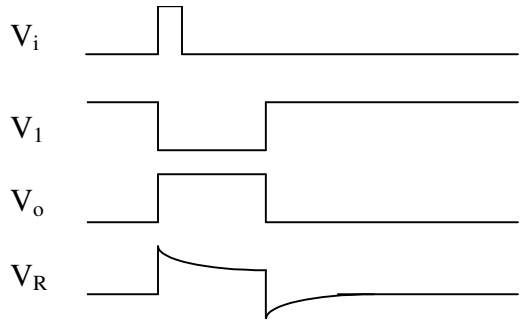
ABCD	$F_1F_2F_3$
0000	1 0 0
0001	0 0 0
0010	0 0 0
0011	0 0 x

ABCD	$F_1F_2F_3$
0100	0 1 0
0101	0 1 x
0110	0 1 0
0111	0 1 x

ABCD	$F_1F_2F_3$
1000	0 1 0
1001	0 1 0
1010	0 1 0
1011	0 1 0

ABCD	$F_1F_2F_3$
1100	0 0 0
1101	0 0 1
1110	0 1 0
1111	1 1 1

Q9.a. Assuming that the input impedance of the CMOS gate is infinite and that the gate delays are zero, the waveforms at various points in the given monostable circuit are as given below with V_1 as the waveform at the output of first NOR gate.



A sudden change in V_o is transferred to the resistance R. The capacitor C discharges till V_R equals the threshold voltage of the driver transistor of the NOR gate (assume it to be $0.5V_{DD}$). At this time, V_1 suddenly switches to V_{DD} and V_o to zero. This change is also transferred to R and the capacitor then charges asymptotically to zero. Thus, during the time when $V_o = V_{DD}$ (logic 1),

$$V_R = V_{DD}\left(1 - e^{-t/RC}\right)$$

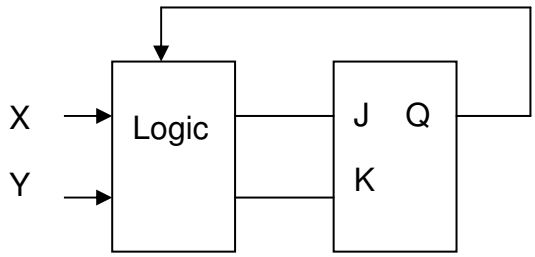
where RC=(50x10^3)x(0.01x10^{-6})=5x10^{-6}s. The time period T of the output pulse will end when $V_R = 0.5V_{DD}$. For this condition, T can be evaluated as 7.2x10^{-6}s.

b. The truth-table and the excitation table of the flipflop are as given below

X Y	Q_{n+1}
0 0	$\overline{Q_n}$
0 1	1
1 0	0
1 1	Q_n

Exc.	*X Y*
0 → 0	1 x
0 → 1	0 x
1 → 0	x 0
1 → 1	x 1

To convert a *JK* flipflop to *XY* flipflop, one needs to design a logic whose inputs are *X,Y* and *Q*, and whose outputs are *J* and *K* inputs of the *JK* flipflop as shown



The truth table for this logic can be written as

$X\ Y\ Q_n$	Q_{n+1}	$J\ K$
0 0 0	1	1 1
0 0 1	0	1 1
0 1 0	1	1 0
0 1 1	1	1 0

$X\ Y\ Q_n$	Q_{n+1}	$J\ K$
1 0 0	0	0 1
1 0 1	0	0 1
1 1 0	0	0 0
1 1 1	1	0 0

From this table, $J = \overline{X}$ and $K = \overline{Y}$.

Q10.a. For 4-bit 2's complement adder/subtracter, refer to Sections 7.2, 7.3 [2].

b. For a TTL to CMOS interface, refer to Section 8.12 [3] and for a TTL to ECL interface, refer to Section7.12 [3]

Q11. (i) For PLA, refer to Section 7.15 [2].
(ii) For CCD, refer to Section 9.7 [2].
(iii) For Shottky diode as a switch, refer to 1.12 [3].
(iv) For IC power amplifiers, refer to Section 14.8 [1].
(v) For Parity Check Generator, refer to Section 7.5 [2].
(vi) For Switched mode power supply, refer to Section 17.7 [2].

DETAILED SOLUTIONS A-09 DEC2003

Q1.a. D The OpAmp is working as a comparator and its negative terminal is at a higher potential than the positive terminal. Therefore, the output will saturates to –18 volts, approximately.

b. B The equivalent resistance is equal to $\frac{1}{f\,C}$ where f = 10KHz and $C = 1.5\mu F$.

c. B $7\text{x}10^6$ bytes = $7\text{x}8\text{x}10^6$ bits.

d. D The binary number 01101100 = 108 (decimal) corresponds to input voltage of 2.16 volts. It is the highest level smaller than 2.17 volts.

e. A If T-input is at logic 1, the output waveform has a period twice as that of the input waveform.

f. A MOS Opamps have better linearity and better noise performance.

g. A The transfer function *H(s)* of an RC highpass filter is $H(s) = \frac{s}{s + 1/RC}$, which is proportional to s if $\frac{1}{RC} >> f$.

h. D Apply Demorgan's theorem once to write the give expression as $\overline{A\bar{B}CD}$. Apply Demorgan's theorem once more to get the result.

PART I

Q2. a. For biquadratic transfer functions, refer to Table 12.16 [1]

b. With finite gain A, the negative input terminal of the Opamp will be at $\left(V_o/A\right)$.

KCL at this terminal can be written as

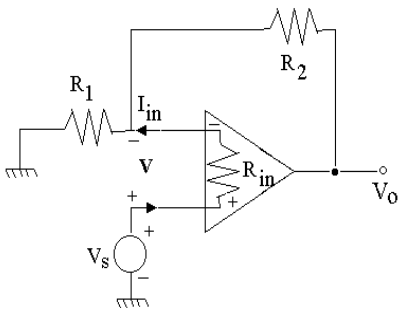
$$\frac{V_{in} - \frac{V_o}{A}}{R_1 + 1/sC_0} = \frac{\frac{V_o}{A} - V_o}{R_2} \text{ , or } V_{in}R_2 = V_o\left[\frac{1}{A}\left(R_2 + R_1 + \frac{1}{sC_0}\right) + \left(R_1 + \frac{1}{sC_0}\right)\right]$$

Substituting for $A = \left(\frac{A_0\omega_p}{s}\right)$ and simplifying gives the bandpass transfer function as

$$\frac{V_o}{V_{in}} = \frac{sR_2\left(A_0\omega_p\right)}{s^2 + s\left[A_0\omega_p R_1 + \frac{1}{C_0}\right] + \frac{A_0\omega_p}{C_0}}.$$

Q3.a. The figure below shows the circuit of noninverting amplifier. The Opamp has an input impedance of R_{in} and the current flowing through it develops a small voltage V with the polarity shown in the figure. The KCL equation at negative terminal of Opamp can be written as

$$\frac{V_s - V}{R_1} + \frac{V_s - V - V_0}{R_2} = \frac{V}{R_{in}} = I_{in}$$



This can be simplified to

$$\frac{V_s}{I_{in}} = \left(\frac{V_0}{R_2 I_{in}} + 1\right)\left(R_1 \,\|\, R_2\right) + R_{in}$$

In a noninverting amplifier V_o is positive if V_s is positive. Thus, the input impedance as seen by the positive terminal of Opamp is greater than R_{in}, the impedance of the open loop amplifier.

b. For analog multipliers, refer to Sections 16.13, 16.14 [2].

Q4.a. For details of the given logarithmic amplifier, refer to Section 16.13 [2]. The conditions are required for the circuit to be a logarithmic amplifier are:

(i) Q_1 and Q_2 should be matched transistors.

(ii) The transistors should be biased such that $v_{BE1} = V_T \ln i_{C1}$ and $v_{BE2} = V_T \ln i_{C2}$.

(iii) The base voltage of Q_2 be very small compared to V_{REF}.

b. For Sample and Hold circuits, refer to Section 16.2 [2].

Q5.a. For transistor Switching times, refer to Section 3.8 [2].

b. For Gilbert multiplier, refer to Section 16.14 [2].

Q6. (i) For Slew rate of Opamps, refer to Section 2.6 [1].

(ii) For Dual Slope ADC, refer to Section 16.5 [2].

(iii) For Instrumentation Amplifier, refer to Section 2.4 [1].

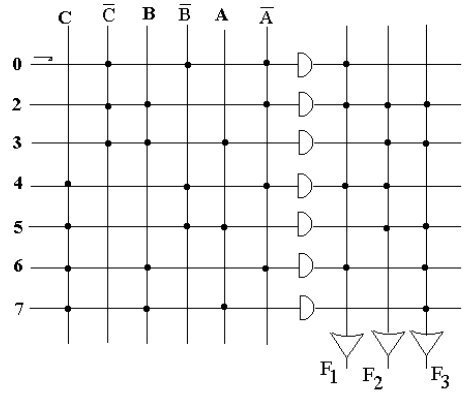
(iv) For Multiple Opamp Biquad, refer to Section 12.7 [1].

PART II

Q7.a. For Transfer Characteristics of TTL, refer to Sections 6.5, 6.6, 6.7 [3].

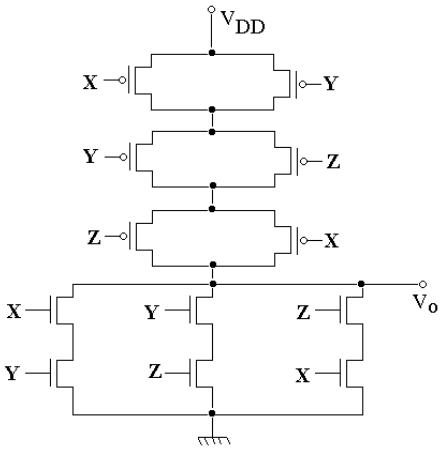
b. For TTL-CMOS interfacing, refer to Section 8.12 [3].

Q8.a. A simple PLA implementation of the given functions is shown in figure below.

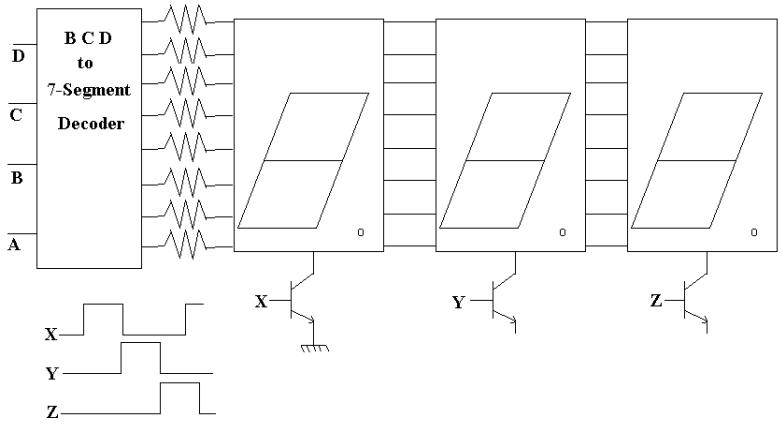


b. For PROM, refer to Section 11.6 [1]. For PAL and PLA, refer to Sections 7.14 and 7.15 [2].

Q9.a. For rule of CMOS gate formation, refer to Section 10.3 [1]. Using this rule, the following circuit for the given function results.



b. A circuit for a 3-digit display using using only one decoder is shown below. The data to be displayed by the three displays comes in to the display decoder serially. The displays are also turned ON serially (one at a time) by mutually exclusive waveforms applied to the displays as shown in the figure. Thus, a single BCD to 7-segment decoder can be multiplexed to turn ON the three displays.



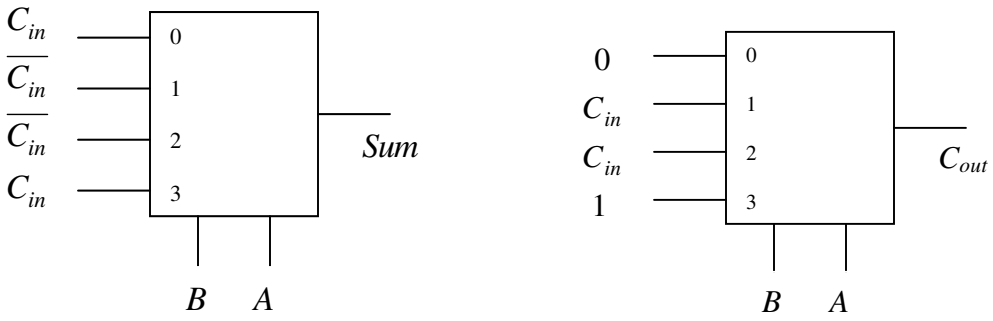
Q10.a. For description of a comparator circuit, refer to Section 7.4 [2].

b. The Boolean functions describing a full adder having A, B and C as inputs, are given as

$$Sum = A \oplus B \oplus C$$

$$C_{out} = AB + BC + CA$$

The implementation using two 4:1 multiplexers is shown in the figure.



Q11. (i) For comparison between TTL and ECL, refer to Section 7.1 [3].

(ii) For Shift Registers, refer to Section 8.5 [2].

(iii) For Memory Organization, refer to Sections 12.16,12.17 [3].

(iv) For Synchronous and Asynchronous counters, refer to Sections 8.6,8.7 [2].

Detailed Solution A-09 June 2004

Q1.a. D The output V_o is equal to V_+ (the voltage at the positive terminal of the OpAmp) for both $\omega = 0$ (both capacitors are open circuit) and $\omega = \infty$ (both capacitors are short circuit). This is not possible for LPF or HPF or BPF .

b. C The transfer function of the integrator is $\frac{V_o}{V_i} = \frac{(R_2/R_1)}{sCR_2 + 1}$. Its Bode plot has a corner frequency at 100 rad/s or 16 Hz. Thus limiting frequency should be ten times 16 Hz = 160 Hz.

d. A Refer to Section 12.7 [1]

d. D From the figure, slew rate = $\frac{3-(-3)}{0.25x10^{-6}} = 24\,volts/\mu s$.

e. B Transistor D is in series with parallel combination of transistors A, B and C. Thus, the result.

f. B After 16 pulses the counter will come back to the state it started with (1001). Another 7 pulses will take it to 0000.

h. D Refer to Section 4.3 [3].

h. B The time taken for the input pulse to ripple through all the *N* flip-flops will be 12*N* nsec. Thus, the maximum speed of operation of the counter is $1/(12x10^{-9}N)$.

$$\frac{1}{12x10^{-9}N} \geq 10x10^6$$

or N=8. Therefore modulo count is 2^N=256.

PART I

Q2. a. Refer to Sections 2.1, 2.2 [1].
Gain at corner frequency is equal to Open loop gain (in dB) – 3dB. If the open loop gain is 10^5, then gain at corner frequency = $20\log_{10}10^5 - 3 = 97$ dB.

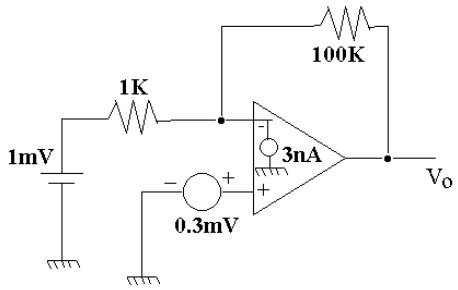
b. Compensating capacitor avoids oscillations in an amplifier by reducing its gain at a frequency at which the phase shift is 180^0. Such compensating capacitor introduces an additional pole at a frequency much lower than the frequencies of the natural poles of the amplifier. As such, the gain of the amplifier drops to unity at a smaller frequency.

If the slew rate is $1V/\mu s$, the smallest duration in which the output can change by 10*V* is $10\mu s$.

Maximum frequency of sine wave = $\frac{slew\ rate}{2\pi V_{\max}} = \frac{10^6}{2\pi 10} = 15915Hz$

c. For 10 degree change in temperature, the offset voltage will be $300\mu V$ while the

offset current will be 3*nA*. Thus, the Op-Amp inverter with input voltage, offset voltage and offset current is as shown in the figure below. The output voltage is obtained by writing KCL at the inverting terminal as



$$\frac{V_o - 0.3mV}{100K} + \frac{V_i - 0.3mV}{1K} = 3nA \ .$$

Thus, $V_o = 70.6mV$ and the error = 29.4*mV*.

Q3.a. For two-stage CMOS Op-Amp, refer to Section 9.1 [1].
c. For instrumentation amplifier, refer to Example 2.4 [1].

Q4. For details on Butterworth and Chebyshev filters, refer to Section12.3 [1].
With reference to the figure shown, the ripple factor ε can be evaluated from

$$\alpha_{\max} = 10\log_{10}\left(1+\varepsilon^2\right) \ .$$

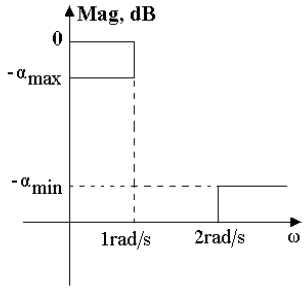
Thus, $\varepsilon = \sqrt{10^{(\alpha_{\max}/10)} - 1} = \sqrt{10^{0.05} - 1} = 0.122$. The order N_{CH} of the Chebyshev filter can be obtained from the following equation, with $A = 10^{\left(\alpha_{\min}/20\right)}$, as

$$N_{CH} = \frac{\cosh^{-1}\left[\sqrt{A^2-1}/\varepsilon\right]}{\cosh^{-1}\left[\Omega_S/\Omega_P\right]} = \frac{\cosh^{-1}\left[\sqrt{31.6228-1}/0.122\right]}{\cosh^{-1}[2]} = 3.4$$

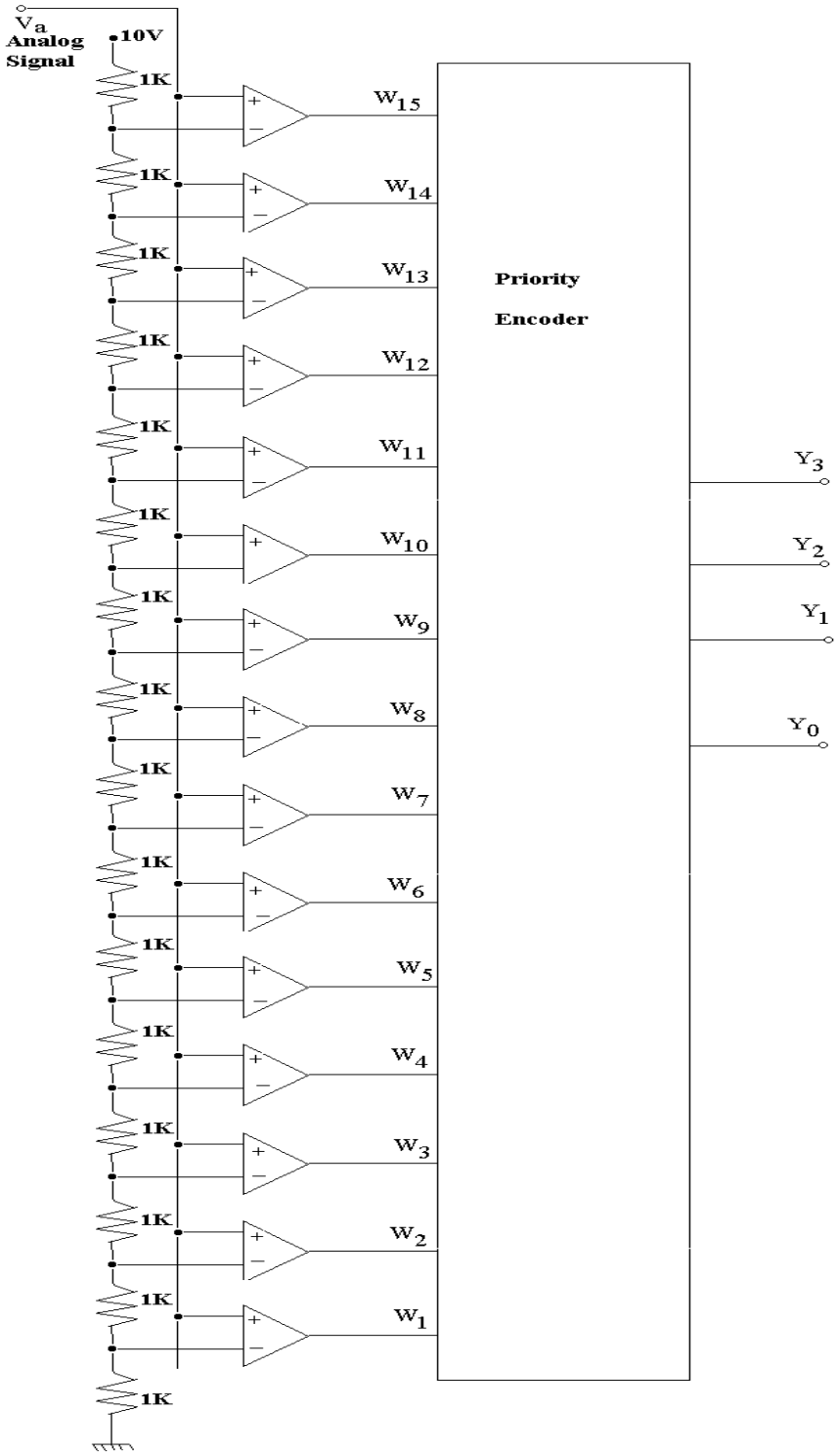
The order must be an integer. Thus $N_{CH} = 4$. Similarly, the order N_{BW} of the Butterworth filter having same specifications can be obtained from the following equation as

$$N_{CH} = \frac{\log_{10}\left[\sqrt{A^2-1}/\varepsilon\right]}{\log_{10}\left[\Omega_S/\Omega_P\right]} = \frac{\log_{10}\left[\sqrt{31.6228-1}/0.122\right]}{\log_{10}[2]} = 5.5 \ ,$$

or N_{BW} = 6, which is 2 higher than the order used for Chebyshev filter.



Q5.a. The flash analog to digital converter is the fastest conversion method. A 4-bit flash converter uses 2^4-1=15 comparators. The analog input V_a is applied to the positive terminal of each comparator. The negative terminal of the comparators is supplied with equally spaced reference voltages obtained from a potential divider network consisting of 2^4=16 1K resistances as shown in the figure below. This arrangement sorts the analog input in a range between two adjacent reference voltages. The outputs of the comparators are fed to a priority encoder to obtain the binary output. The required fifteen reference voltages are $\frac{10}{16}, \frac{20}{16}, \frac{30}{16}, ..., \frac{150}{16}$.



Inputs																		
W_{15}	W_{14}	W_{13}	W_{12}	W_{11}	W_{10}	W_9	W_8	W_7	W_6	W_5	W_4	W_3	W_2	W_1	Y_3			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0		
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	1
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The logic for the priority encoder can be obtained as per the following truth table.

If time taken for comparison is 50ns and that for priority encoder is 35ns, then total time for conversion is 85ns. Thus, the maximum possible conversion rate is $\frac{1}{85ns} = 11.8MHz$.

The output $Y_3Y_2Y_1Y_0$ for inputs 0V, 5.1V and 10V will be, respectively, 0000, 1010 and 1111.

b. For IC power amplifiers, refer to Section 14.8 [1]

Q6. For TTL, refer to Sections 6.5, 6.6, 6.7, 6.10 [3].

Q7.a. The truth table for BCD to Excess-3 code is shown in the truth table given below.

ROM Address				ROM Outputs			
W_4	W_3	W_2	W_1	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1

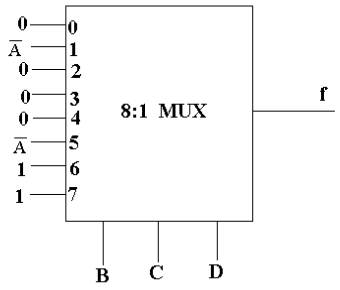
The table also shows the excess-3 outputs of the ROM for different BCD inputs given as ROM address. The data stored in the ROM for remaining inputs is **don't care**.

b. For truth table of Gray to binary converter, refer to Section 7.9 [2]. The corresponding Boolean functions can be obtained from this table as

$$Y_3 = W_3 \qquad Y_2 = Y_3 \oplus W_2$$
$$Y_1 = Y_2 \oplus W_1 \qquad Y_0 = Y_1 \oplus W_0$$

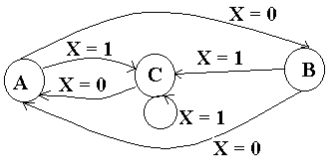
which can be easily implemented using Ex-OR gates.

Q8a. The residues of the given Boolean function for various combinations of B, C and D are shown in the following truth table, which can be implemented by an 8:1 MUX as shown in the figure



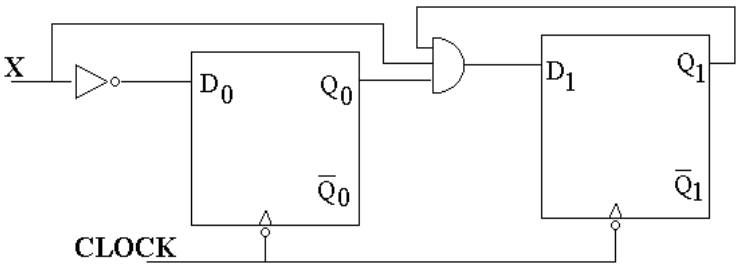
B	C	D	f
0	0	0	0
0	0	1	$\overline{A}$
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	$\overline{A}$
1	1	0	1
1	1	1	1

b. The state diagram for the problem and the state table along with D inputs of the two flipflops are as shown below.

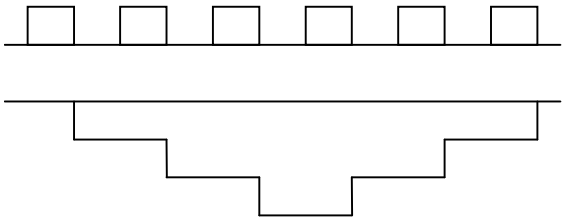


PS	NS		D_1		D_0	
Q_1Q_0	X=0	X=1	0	1	0	1
0 0	0 1	1 0	0	1	1	0
0 1	0 0	1 0	0	0	1	0
1 0	0 0	1 0	0	0	1	0

From the table, $D_1 = \overline{Q_1}\,\overline{Q_0}X$ and $D_0 = \overline{X}$. The circuit is as given below.

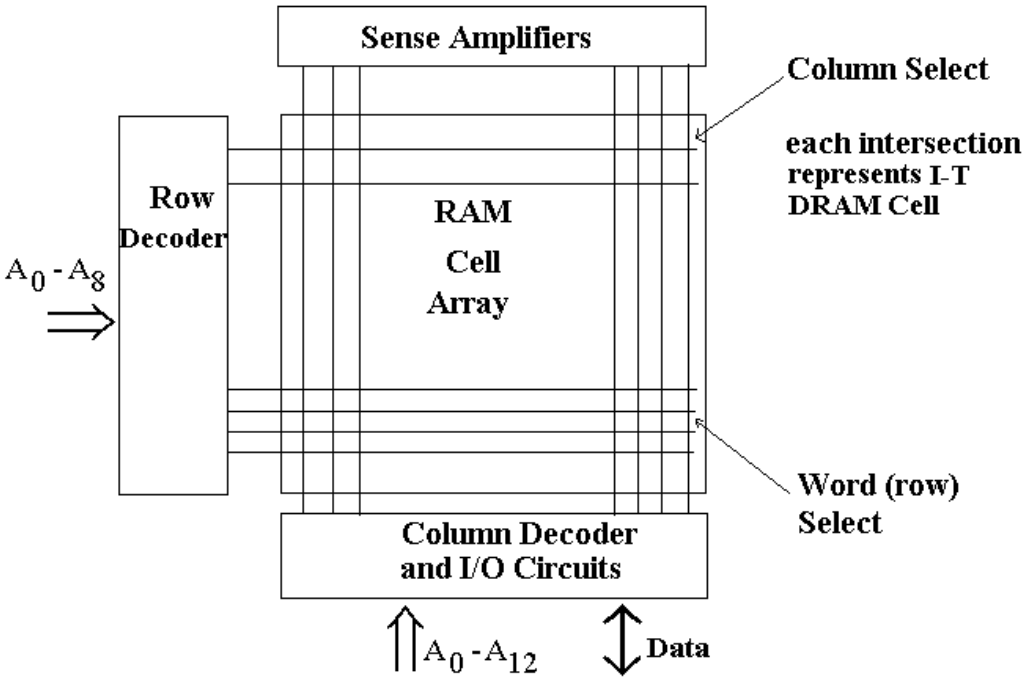


Q9.a. The given circuit is a modulo-6 twisted ring (Johnson) counter, whose outputs Q_0, Q_1, Q_2 are fed to an inverting summer amplifier. Count sequence of the counter is 000,100,110,111,011,001. Therefore, the output of the Opamp will be a repeating sequence 0V, -1V, -2V, -3V, -2V, -1V changing at every falling edge of the clock. as shown in the figure.



b. (i) 10
(ii) (5/1024) MHz, assuming a ripple counter.
(iii) 1024
(iv) 2060=1024+1024+12. Hence, counter will hold 12.
(v) Yes, in case of a ripple counter. In a synchronous counter, the clock is applied simultaneously to all flipflops and thus, the maximum frequency of operation does not depend on the modulus of the counter.

Q10.a. A 2½ D organized 16X1 memory is using two 2-4 decoders is shown in the figure below.
b. For programmable arrays, refer to Sections 7.14, 7.15 [2].
c.



Q11. (i) For sequence generators, refer to Section 10.17 [3].
(ii) For Single Amplifier Biquad , refer to Section 16.10[2].
(iii) For analog multipliers, refer to Sections 16.13, 16.14 [2]
(iv) For Switched Capacitor Filters, refer to Section 16.12 [2].

DETAILED SOLUTIONS A-09 DEC 2004

Q1. a. B Refer to Section 16.9 [2]. The correct answer is B with 2N-1 instaed of N-1

b. C By virtual ground, the input terminals of the Opamp are at same potential thus making resistances R_1 in series.

c. C The capacitors are open circuit at dc and the voltage at the inverting terminal of Opamp is the same as that at the noninverting terminal (equal to 0.5V). Since no current flows feedback resistances, the output voltage is also equal to 0.5V.

d. A The function can be expanded as

$$f = \overline{A}\,\overline{B}\,C\overline{D} + \overline{A}\,\overline{B}\,CD + \overline{A}BC\overline{D} + ABC\overline{D} + A\overline{B}\,\overline{C}D + AB\overline{C}D$$

e. D A T flipflop divides the frequency of the input clock by 2 and its output is a square wave.

f. D When inputs are 00, both outputs are 1. Switching the input to 11 makes one of the outputs race to 0 .

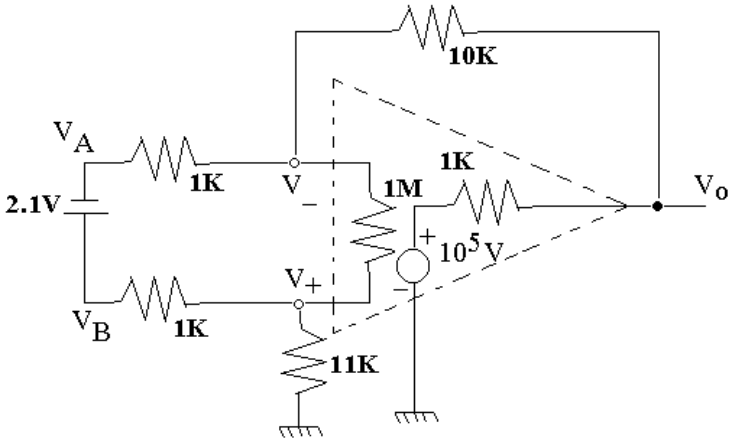
g. B Because there is a feedback.

h. C The load in a MOS differential amplifier is very large, often a current source.

PART I

Q2.a. With Opamp replaced by its equivalent circuit, the given amplifier can be drawn as shown in the figure where V_i = -2.1V. The node equations at negative and positive terminals of the Opamp may be respectively written as

$$\frac{V_- - V_A}{1K} + \frac{V_- - AV}{11K} - \frac{V}{1M} = 0 \qquad and \qquad \frac{V_B - V_+}{1K} = \frac{V}{1M} + \frac{V_+}{11K}$$



where $V=V_+-V_-$ and $A=10^5$. Solving these equations with $V_B - V_A = 2.1V$ give $V=0.231$mV.

b. Same figure can be used to obtain the gain. Neglecting current through 1M input impedance of the Opamp, the node equations can be written as

$$\frac{V_A - V_-}{1K} = \frac{V_- - AV}{11K} \qquad and \qquad \frac{V_B - V_+}{1K} = \frac{V_+}{11K}$$

Which give $AV = 11(V_B - V_A)$. Further, the following equations may be written for currents through the three 1K resistances.

$$V_A - V_- = V_+ - V_B = V_o - AV$$

These two equations can be solved to get $2V_o = 2AV - (V_B - V_A)$. Substituting for AV gives $V_o = 10.5(V_B - V_A)$. Thus, the gain is 10.5.

c. Same figure can be used to obtain the gain. Writing KVL for the loop containing the source, we get

$$\frac{V_B - V_S - V_A}{R_S} + \frac{V_B - V - V_A}{2K} = 0 \qquad or \qquad V_B - V_A = \frac{V_S}{3} + \frac{V}{3} \cong \frac{V_S}{3}$$

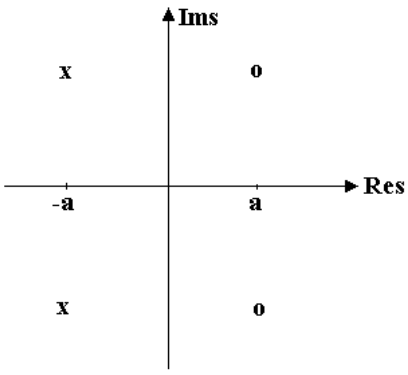
where V_S is the source voltage and R_S =1K is the source resistance. Using the result of Q2c gives

$$V_o = 10.5(V_B - V_A) = 10.5\frac{V_S}{3}.$$

Thus, the gain is 3.5.

Q3. (i) The poles and zeros of H(s) are respectively given by

$$s_p = \frac{-a \pm \sqrt{b^2 - 4ac}}{2} \text{ and } s_z = \frac{a \pm \sqrt{b^2 - 4ac}}{2}$$



Thus, the poles are at mirror image locations of the zeros as shown in the figure.

(ii) The magnitude of this allpass filter is K. For plots of magnitude and phase, refer to p.1105 [1].

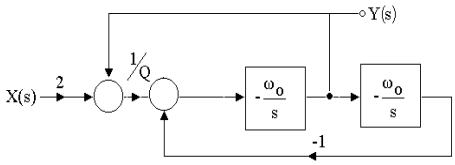
(iii) For passive realization, refer to Section 12.5.7 [1].

(iv) With $a = \frac{\omega_0}{Q}$, $b = \omega_0^2$, *H(s)* can be written as

$$H(s) = \frac{Y(s)}{X(s)} = K - \frac{K2(\omega_0/Q)s}{s^2 + (\omega_0/Q)s + \omega_0^2}$$

Or, $$Y(s) = -(\omega_0/s)[2X(s) + Y(s)]\frac{1}{Q} - \frac{\omega_0^2}{s^2}Y(s)$$

which can be realized as shown in the figure below.



Q4. For a description of Dual slope converter and derivation of expressions, refer to Section 16.5 [2].

(i) Time required for the out put to reach its maximum value is same as the time required by the counter to reach its maximum count of 2^{12}. For a clock of 1MHz, this is equal to $\frac{2^{12}}{10^6} = 4.096ms = t_1$.

(ii) For a 5V input, $t_2 = t_1 \frac{V_{in}}{|V_{ref}|} = 2.048ms$. Thus, conversion time is equal to *t1+t2* = 6.144ms.

Q5.a. For electron density distribution and explanation, refer to Section 1.20 [3].

b. For diode switching, refer to Section 1.18 [3]

Q6. (i) For DC level shifting, refer to Section 14.4 [2].
(ii) For Sample and Hold circuits, refer to Section 16.2 [2].
(iii) For Sensitivity of a Biquad, refer to Section 12.9 [1].
(iv) For MOS Opamps, refer to Section 14.13[2].

PART II

Q7.a. Assuming Q to be in active region, base current of Q = I/100 = 2.5x10^{-5}A.
Thus, $V = 5 - I_B 1.4K - V_{BE} - V_D = 3.25$ V. It is easily seen that the collector voltage is 5-$I_C R_C$=5-0.25=4.75V. and the base voltage is 3.25+0.7+0.7=4.65V.
Thus, V_{BC} = -0.1V indicating that Q is indeed in active region.

b. A trivial solution is when V_i < 2 *volts* and V_o = 12 *volts.*

Assume both transistors are in saturation. Then

$$k_p(12 - V_i - V_T)^2 = k_n(V_i - V_T)^2$$

Solving with k_p=k_n and V_T = 2 *volts*, gives V_i = 6 *volts.*

PMOS will be in saturation if V_o - V_i < V_T , or V_o < 8 *volts.* Also, NMOS will be in saturation if V_i - V_o < V_T , or V_o > 4 *volts.* The range when both transistors are in saturation is 4< V_o <8.

Q8.a. It is easily seen that for AB equal to 00, 01, 10, 11, the output of multiplexer will 0, 1, 1, 1, respectively. Thus *f = A+B*.

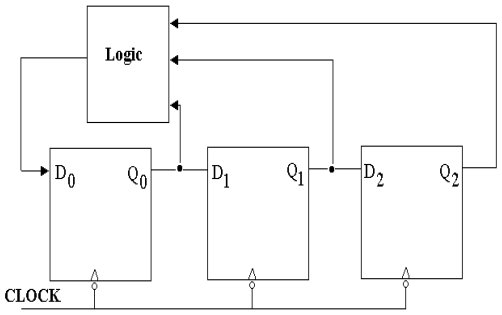
b. The required table is shown below

A	B	C	D	E	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
x	x	x	0	x	0	0	0	0	0	0	0	0
x	x	x	0	x	0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0	0	0	0	0	0
0	1	0	0	1	0	0	1	0	0	0	0	0
0	1	1	0	1	0	0	0	1	0	0	0	0
1	0	0	0	1	0	0	0	0	1	0	0	0
1	0	1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	1	0	0	0	0	0	0	1	0
1	1	1	0	1	0	0	0	0	0	0	0	1

Q9.a. For an explanation of Master-Slave JK flipflop and its advantages, refer to Section 8.4 [2]. A NAND flipflop will take 2 gate delays to stabilize the output after the inuts are applied. Thus, both Master and Slave sections of the flipflop require 3 gate delays. Add 1 gate delay for the gate used for complementing the clock. Thus the delay required after the positive edge of the clock is 4 gate delays or 20ns.

b. A sequence generator is a shift register whose first flipflop gets its D-input from the present state of the shift register through a combinational logic as shown in the figure below. The output of a flipflop in this circuit is a delayed version of its predecessor flipflop. This makes the truth table of the logic block as shown below. From the truth table the Boolean function for the sequence generator can be found to be $D = Q_0 \oplus Q_2$.

Q_0	Q_1	Q_2	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



Q10.a. For description of given circuit, refer to Section 11.4 [1].

b. For static RAM Cell, refer to Section 9.5 [2].

c. The following table derives the operational sequence of the counter, assuming $K_2 = 1$ and $J_2 = Q_0$.

PS								NS		
Q_0	Q_1	Q_2	J_0	K_0	J_1	K_1	J_2 K_2	Q_0	Q_1	Q_2
0	0	0	1	1	1	1	0 1	1	1	0
1	1	0	1	1	1	1	1 1	0	0	1
0	0	1	0	1	1	1	0 1	0	1	0
0	1	0	1	1	1	1	0 1	1	0	0
1	0	0	1	1	1	1	1 1	0	1	1
0	1	1	0	1	1	1	0 1	0	0	0

Thus, it is a mod-6 counter.

Q11. (i) For Emitter-coupled OR gate, refer to Section 7.2 [3].
(ii) For CMOS logic gates, refer to Section 10.3 [1].
(iii) For BJT inverter, refer to Section 6.10 [2].
(iv) For Schottky diode, refer to Section 1.19 [3]