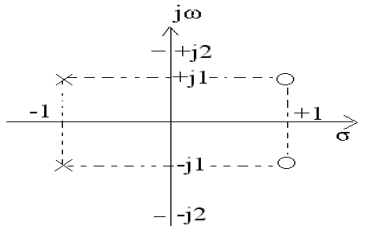
Code: A-09/C-03/T-03 **Subject: ANALOG & DIGITAL ELECTRO**
Time: 3 Hours **Max. Marks: 1**

NOTE: There are 11 Questions in all.

- **Question 1 is compulsory and carries 16 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Answer any THREE Questions each from Part I and Part II. Each of these questions carries 14 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

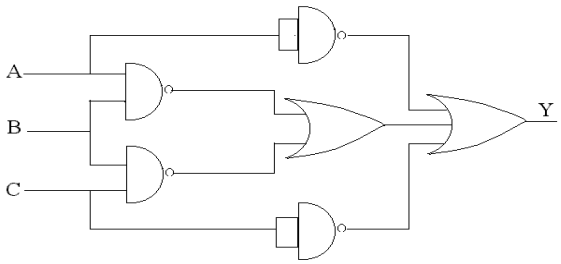
Q.1 Choose the correct or best alternative in the following: (2x8)

a. The pole zero pattern of a certain filter is shown in Fig. below. The filter must be
(A) low pass.
(B) high pass.
(C) all pass.
(D) band pass.



b. For the logic circuit shown in Fig. below, the output y is equal to

(A) $\overline{ABC}$.
(B) $\overline{A}+\overline{B}+C$.
(C) $\overline{AB}+\overline{BC}+\overline{A}+\overline{C}$.
(D) $\overline{A}+\overline{B}+\overline{C}$.



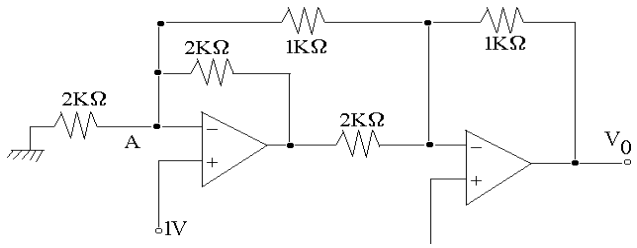
c. 2's complement representation of 16 bit number (one sign bit and 15 magnitude bits) is FFFF. Its magnitude in decimal representation is

(A) 0. **(B)** 1.
(C) 32,767. **(D)** 65,535.

d. A pulse train with a frequency of 1 MHz is counted using a module 1024 ripple counter built with JK flipflops. For proper operation of the counter, the maximum propagation delay per flipflop stage is
(A) 0.1 μs. **(B)** 10 μs.
(C) 1 μs. **(D)** 0.01 μs.

e. The output voltage V_0 for the following circuit is

(A) 6V.
(B) 4V.
(C) 5V.
(D) 3V.



f. The threshold voltage of an n-channel MOSFET can be increased by
(A) increasing the channel dopant concentration.
(B) reducing the channel dopant concentration.
(C) reducing the gate oxide thickness.
(D) reducing the channel length.

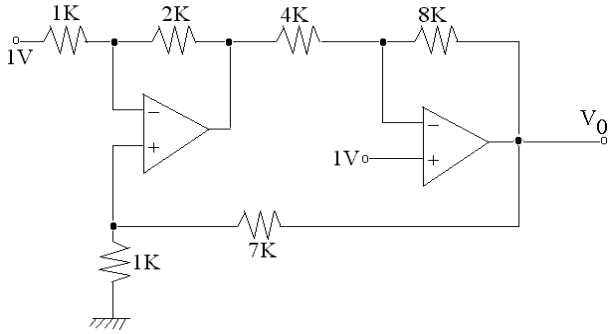
g. A dynamic RAM consists of
(A) 6 transistors. **(B)** 2 transistors and 2 capacitors.
(C) 1 transistor and 1 capacitor. **(D)** 2 capacitors only.

h. A PLA can be used
(A) as a microprocessor. **(B)** as a dynamic memory.
(C) to realize sequential logic. **(D)** to realize a combinational logic.

PART I

Answer any THREE Questions. Each question carries 14 marks.

Q.2 a. Find the output voltage of the following circuit assuming ideal op-amp behaviour. **(5)**

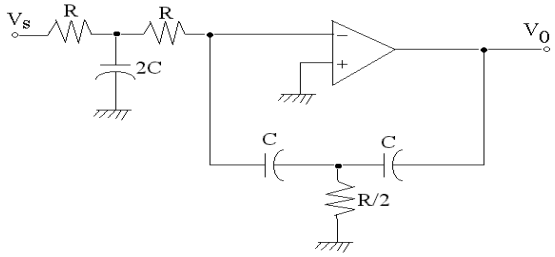


b. How is pole-zero compensation achieved in an op-amp? **(5)**

c. Explain how a sawtooth wave can be generated using an op-amp. **(4)**

Q.3 Explain the operation of
(i) Sample and hold circuit. **(4)**
(ii) Anti log amplifier. **(5)**
(iii) Four quadrant analog multiplier. **(5)**

Q.4 a. Show that the system shown in Fig. below is a double integrator. Assume ideal op-amp. **(7)**



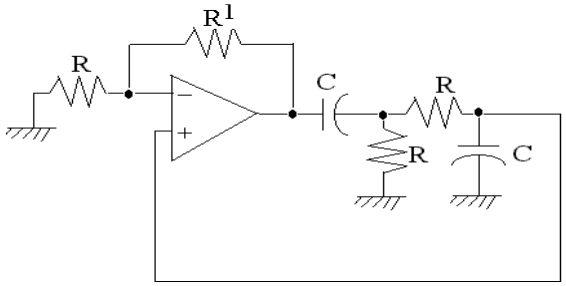
$$\frac{V_o(S)}{V_s(S)} = -\frac{1}{(CRS)^2}$$

b. Design an active second order band pass filter with a centre frequency of 2 KHz, a bandwidth of 150 Hz and a midband gain of 20. Derive the equations used. **(7)**

Q.5 a. Explain with necessary timing diagram, the function of a dual slope A to D converter deriving the necessary expressions for the same. **(8)**

b. For a 12 bit ADC, the normal full scale output is 12 volts. Determine
(i) resolution.
(ii) Input voltage corresponding to all 1's at the output.
(iii) Weightage of MSB. **(6)**

Q.6 a. Find the value of R^1 in the circuit shown below for generating sinusoidal oscillations and determine an expression for frequency of oscillation. **(7)**

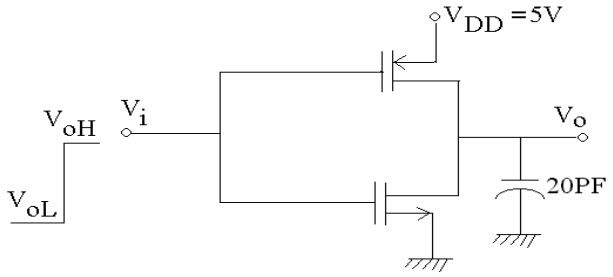


b. In the CMOS inverter circuit shown the input V_i makes a transition from V_{OL} (OV) to V_{OH} (5V). Determine the high to low propagation delay time (t_{PHL}) when it is driving a capacitive load of 20 pF. Device data :

NMOS: $V_{TN} = 1V.\ k_N = \mu_n C_{OX} \left(\frac{W}{L}\right)_n = 40\,\mu\,A/V^2, \quad \lambda = 0;$

PMOS : $V_{TH} = -1V, \quad k_p = \mu_p. \quad C_{OX}\left(\frac{W}{L}\right)_P = 20\mu A/V^2, \quad \lambda = 0.$

Neglect body effect. **(7)**

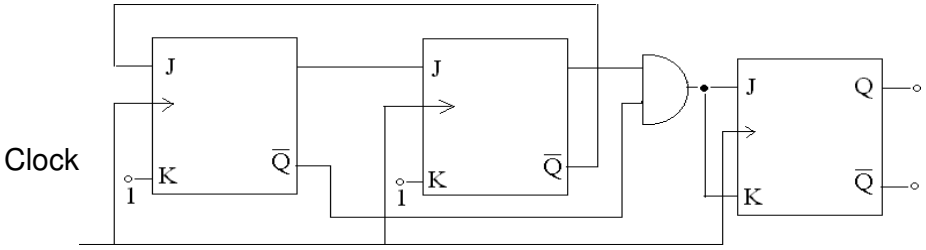


PART II

Answer any THREE Questions. Each question carries 14 marks.

Q.7 a. In a certain application, four inputs A, B, C, D (all are available in complemented and uncomplemented forms) are fed to a logic circuit, producing an output F which operates a relay. The relay turns on when F(ABCD) = 1 for the following states of the inputs (ABCD); 0000, 0010, 0101, 0110, 1101 and 1110. States 1000 and 1001 do not occur and for the remaining states, the relay is off. Minimise F and realize it using minimum number of 3-input NAND gates. **(7)**

b. The circuit diagram of a synchronous counter is shown below. Determine the sequence of states of the counter assuming that the initial state is '000'. Give your answer in a tabular form showing the present state, next state and the JK inputs. From the table determine the modulus of the counter. **(7)**



Q.8 a. Design a full adder using Multiplexers. **(7)**

b. A ROM is to be used to implement the Boolean functions given below :

$F_1(A,B,C,D) = ABCD + \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$

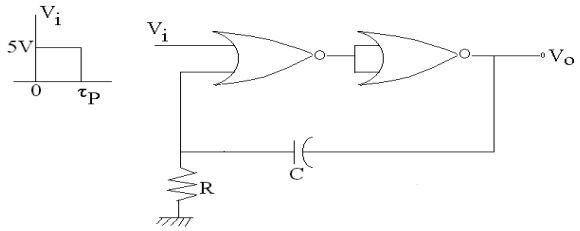
$F_2(A,B,C,D) = (A+B)(\overline{A}+\overline{B}+C)$

$F_3(A,B,C,D) = \sum (13,15) + \sum_{\phi}(3,5)$

(i) What is the minimum size of the ROM required ?

(ii) Determine the data in each location of the ROM. **(7)**

Q.9 a. For the CMOS monostable multivibrator shown in Fig. below, R=50 KΩ, C=0.01 μF, $V_{DD} = 5V$ and the CMOS NOR gates have a threshold of 1.5 volts, V_i is a trigger pulse ($\tau_P << RC$) as shown.



(i) Plot V_0 and V_R as function of time.

(ii) Write the equation for $V_R(t)$, for $t > 0$.

(iii) Find the time period of the output pulse. **(7)**

b. A new clocked X-Y flipflop is defined with two inputs, X and Y in addition to the clock input. The flipflop functions as follows :
If XY = 00, the flipflop changes state with each clock pulse.
If XY = 01, the flipflop state Q becomes 1 with the next clock pulse.
If XY = 10, the flipflop state Q becomes 0 with the next clock pulse.
If XY = 11, no change of state occurs with the clock pulse.

(i) Write the truth table for the X-Y flipflop.

(ii) Write the excitation table for the X-Y flipflop.

(iii) It is desired to convert a JK flipflop to the X-Y flipflop (as mentioned above) by adding some external gates, if necessary. Draw a circuit to show how will you implement the X-Y flipflop using JK flipflop. **(7)**

Q.10 a. Design a 4 bit adder cum subtractor using shift registers. **(8)**

b. Discuss how interfacing is achieved between

(i) TTL and CMOS gates. (ii) TTL and ECL gates. **(6)**

Q.11 Write explanatory notes on (Any **FOUR**):

(i) PLA.

(ii) CCD.

(iii) Schottky diode as a switch.

(iv) IC power amplifiers.

(v) Parity check generator.

(vi) Switched mode power supply. **(14)**

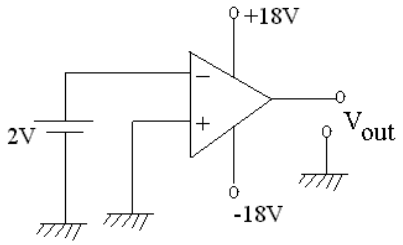
Code: A-09/C-03/T-03 **Subject: ANALOG & DIGITAL ELECTRO**
Time: 3 Hours **Max. Marks: 1**

NOTE: There are 11 Questions in all.

- **Question 1 is compulsory and carries 16 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Answer any THREE Questions each from Part I and Part II. Each of these questions carries 14 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: **(2x8)**

a. Output voltage (V_{out}) of the circuit shown below is approximately



(A) $-2V$.
(B) -2×10^{5} V.
(C) α.
(D) $-18V$.

b. In switching capacitor circuit, the value of resistor corresponding to switched capacitor of value $1.5\,\mu f$ and switching frequency 10 KHz is

(A) $0.015\,\Omega$.
(B) $66.6\,\Omega$.
(C) $1.5\times10^{-10}\,\Omega$.
(D) $0.666\times10^{10}\,\Omega$.

c. A 7-M-byte memory chip has the capacity of

(A) 7×10^{6} bits.
(B) 56×10^{6} bits.
(C) 7×10^{20} bits.
(D) 7×10^{23} bits.

d. A successive approximation ADC has a resolution of 20 mV. The digital output for an analog input of 2.17 V is

(A) 01101101.
(B) 01101011.
(C) 01110111.
(D) 01101100.

e. A square wave with a period of $10\,\mu s$ drives a T-flip-flop. The period of the output signal will be

(A) $20\,\mu s$.
(B) $10\,\mu s$.
(C) $5\,\mu s$.
(D) $100\,\mu s$.

f. In comparison to Bipolar op-amps, the MOS op-amps are

(A) superior in quality.
(B) inferior in quality.
(C) quality is almost same.
(D) much much superior in quality.

g. A high pass RC filter acts as a pure differentiator when

(A) $RC << \frac{1}{f}$. **(B)** $RC >> \frac{1}{f}$.

(C) $RC = \frac{1}{f}$. **(D)** $RC = \alpha$.

h. Boolean expression $\overline{\overline{A(B+\overline{C})}D}$ is equal to

(A) $A + \overline{B} + \overline{C}D$. **(B)** $\overline{A} + \overline{B} + C + D$.

(C) $\overline{A} + B + C + \overline{D}$. **(D)** $\overline{A} + B + \overline{C} + \overline{D}$.

PART I

Answer any THREE Questions. Each question carries 14 marks.

Q.2 a. Write biquadratic transfer function for lowpass, highpass, bandbass and band reject filters. **(6)**

b. Using $A = \frac{A_0 W_p}{S}$, verify that the circuit given in Fig.1 below is a band pass filter. **(8)**

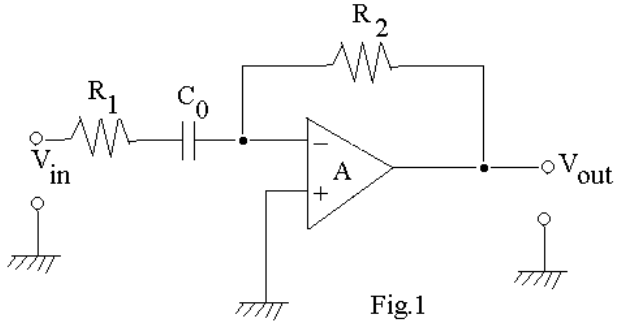


Fig.1

Q.3 a. Derive the input impedance of a close loop non-inverting op-Amp. amplifier and show that it is greater than the open loop input impedance. **(8)**

b. What is an analog multiplier? Compare in brief, the performances of 1-quadrant, 2-quadrant and 4-quadrant multipliers. **(6)**

Q.4 a. Under what condition the circuit of Fig.2 can function as a log-amplifier? Use ideal op-amps. **(8)**

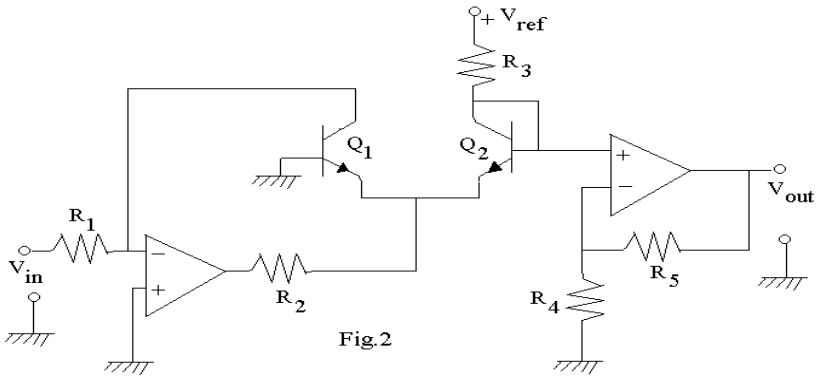


Fig.2

b. Draw an op-amp based sample and hold circuit and explain the operation. **(6)**

Q.5 a. Discuss the switching time of a transistor with the help of a pulse waveform at the input of a transistor. **(4)**

b. Draw the circuit of a 4-quadrant Gilbert multiplier and derive its output. State the approximation made, if any. **(10)**

Q.6 Write short notes on any **TWO** of the following :

(i) Slew rate of op-amp.
(ii) Dual slope type of ADC.
(iii) Instrumentation Amplifier.
(iv) Multiple op-amps Biquad filter. **(7 x 2 = 14)**

PART II

Answer any THREE Questions. Each question carries 14 marks.

Q.7 a. Derive the necessary parameters to sketch and explain the transfer characteristic of the TTL circuit of Fig.3 below :- **(8)**

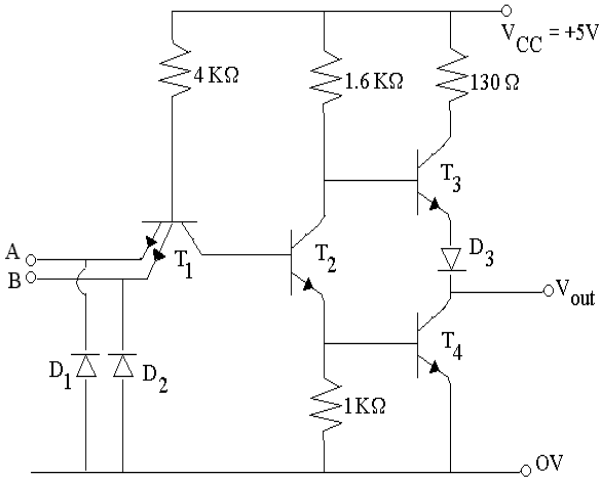


Fig.3

b. What are the problems associated with the interfacing of TTL with CMOS and Vice Versa? How can these problems be removed? **(6)**

Q.8 a. Implement a simplest PLA circuit for the Boolean function given below. **(8)**

$$F_1(C, B, A) = \sum m(0, 2, 4, 6)$$
$$F_2(C, B, A) = \sum m(2, 3, 4, 5)$$
$$F_3(C, B, A) = \sum m(2, 3, 5, 6, 7)$$

b. Compare PROM, PAL and PLA with an example for each. **(6)**

Q.9 a. Discuss the rule of formation of CMOS network for arbitrary combinational function. Using this rule form the CMOS network for the function f. $f = \overline{XY + YZ + ZX}$ **(8)**

b. Design and explain a basic circuit to display a 3-digit number using only one 7-segment decoder. **(6)**

Q.10 a. Design a digital circuit to compare two numbers A and B having 2-bit each for three outputs A > B, A = B and A < B. Use only AND, OR NOT and NOR gates. **(8)**

b. Implement a full adder circuit with MUX modules. **(6)**

Q.11 Write short notes on any **TWO** of the following :

(i) Compare between TTL and ECL family.
(ii) Shift Registers.
(iii) Memory organization.
(iv) Synchronous vs Asynchronous counters. **(7 x 2 = 14)**

Code: A-09/C-03/T-03 **Subject: ANALOG & DIGITAL ELECTRO**
Time: 3 Hours **Max. Marks: 1**

NOTE: There are 11 Questions in all.

- **Question 1 is compulsory and carries 16 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Answer any THREE Questions each from Part I and Part II. Each of these questions carries 14 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x8)

a. The circuit shown in the Fig.1 represents

(A) LPF.
(B) HPF.
(C) BPF.
(D) BSF.

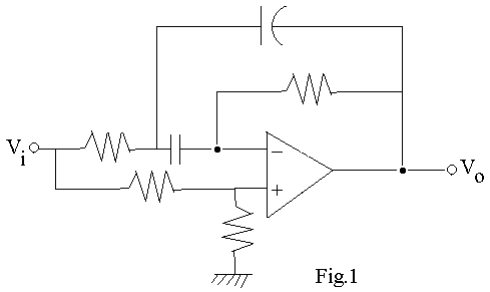


Fig.1

b. The frequency limit for the circuit shown in Fig.2 to operate as an integrator will be

(A) 1.6 Hz.
(B) 16 Hz.
(C) 160 Hz.
(D) 1.6 KHz.

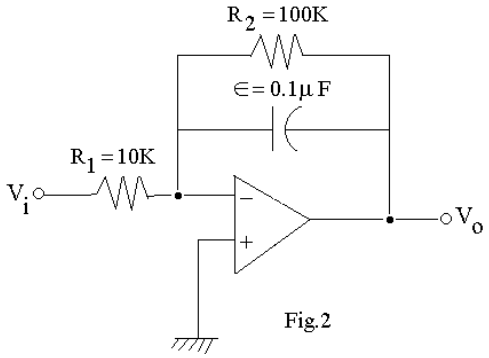


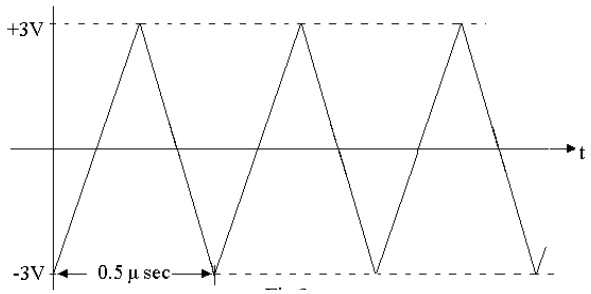
Fig.2

c. The three basic second order filtering functions LP, BP and HP are performed simultaneously by a universal active filter that can be implemented using

(A) two integrator loop Biquad. **(B)** Second order LCR resonator.
(C) single amplifier Biquad. **(D)** both by **(A)** and **(C)**.

d. The output of an op-amp voltage follower is a triangular wave shown in Fig.3 below, for a square wave input of frequency 2 MHz and 10 V peak to peak. The slew rate of the op-amp is

(A) 14 $v/\mu sec$.
(B) 28 $v/\mu sec$.
(C) 12 $v/\mu sec$.
(D) 24 $v/\mu sec$.



e. The circuit at Fig.4 gives an output Y given by

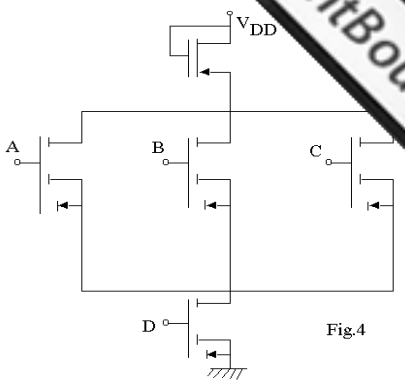


Fig.4

(A) $Y = \overline{ABC + D}$.
(B) $Y = \overline{(A + B + C)D}$.
(C) $Y = \overline{AB + CD}$.
(D) $Y = (A + B + C)D$.

f. A 4 bit ripple counter has a count of 1001 at some instant. The count after 23 pulses will be

(A) 1001. **(B)** 0000.
(C) 1110. **(D)** 0110.

g. The problem of current hogging is associated with

(A) DTL. **(B)** ECL.
(C) TTL. **(D)** DCTL.

h. A ripple counter uses flip flops having t_{pd} = 12 nsec. The largest mod counter that can be constructed from flip flops operated at 10 MHz is

(A) 128. **(B)** 256.
(C) 64. **(D)** 16.

PART I

Answer any THREE Questions. Each question carries 14 marks.

Q.2 a. What is the difference between open loop and closed loop gain of an op-amp? The dc open loop gain of an op-amp is 10^5. What will be the open loop gain at its break frequency? **(4)**

b. Does increasing the compensating capacitor increase or decrease the unity factor bandwidth? How fast can the output of an op-amp change by 10 V, if its slew rate is 1 $V/\mu sec$. Also find the maximum frequency for a sinewave output voltage of 10 V peak with an op-amp whose slew rate is 1 $V/\mu sec$. **(5)**

c. For a non-inverting amplifier R = 1KΩ, $R_f = 100K\Omega$. The op-amp has the following specifications.

$\frac{\Delta V}{\Delta T} = 30\mu v/^\circ C \max$

$\frac{\Delta I}{\Delta T} = 0.3\,nA/^\circ C \max$

Assume that the amplifier is nulled at $25^\circ C$. Calculate the value of the error voltage and the output voltage V_O at $35^\circ C$ if $V_i = 1mV\,dc$. **(5)**

Q.3 a. Explain with a circuit diagram, a two stage CMOS op-amp configuration. What is systematic offset? How can it be minimized? **(7)**

b. For an instrumentation amplifier, show that the output voltage is given by

$$V_0 = \frac{R_2}{R_1}\left(1+\frac{2R'}{R}\right)(V_1 - V_2)$$

Where the symbols have usual significance. **(7)**

Q.4 Determine the ripple factor and order N of the network function that uses Chebyshev approximation to satisfy the following requirements

$\alpha_{max} \le 0.5\,dB \qquad \Omega_p = 1\,r/s$

$\alpha_{min} \ge 30\,dB \qquad \Omega_s = 2\,r/s$

Compare the value of N with Butterworth approximation for same specifications. Derive the necessary expressions. **(14)**

Q.5 a. What is a flash converter? Explain. Consider the design of a 4 bit flash ADC. How many comparators are required? For an input signal in the range of 0 to +10V, what are the reference voltages needed? Show how they can be generated using a 10V reference and several 1 KΩ resistors. If a comparison is possible in 50 nsec and the associated logic requires 35 nsec, what is the maximum possible conversion rate? Indicate the digital code you expect at the output of the comparators and at the output of the logic for an input of
(i) 0V (ii) + 5 .1 V and (iii) +10 V. **(10)**

b. Write a note on IC power amplifiers. **(4)**

Q.6 With reference to any logic family, explain the following :

(i) Transfer characteristics.
(ii) Sourcing and sinking current.
(iii) DC Noise Margin and AC Noise Margin..
(iv) Totem pole TTL and Tristate TTL.
(v) Speed power product. **(14)**

PART II
Answer any THREE Questions. Each question carries 14 marks.

Q.7 a. Design a BCD to excess-3 code converter using a diode ROM circuit. **(6)**

b. Design a combinational circuit that converts a 4 bit reflected code number to a 4 bit binary number. Implement the circuit with exclusive OR gates. **(8)**

Q.8 a. Signals A, B, C, D and $\overline{A}$ are available. Using only one 8 : 1 MUX and no other gates, implement the function,

$$f(A,B,C,D) = BC + AB\overline{D} + \overline{A}\overline{C}D$$ **(7)**

b. A clocked sequential circuit has 3 states A, B, C and input X. As long as X = 0, the circuit alternates between states A and B. If X becomes 1 (either in state A or B), circuit goes to state C and remains in state C as long as X = 1. The circuit goes to state A if X becomes 0 again and then repeats the behaviour. Assume state assignments as A = 00, B = 01 and C = 10.
(i) Draw the state diagram.
(ii) Prepare the state table.
(iii) Draw the circuit using D flip flops. **(7)**

Q.9 a. For the circuit shown in Fig.5 below, sketch V_0 against time. Assume that all flip flops are reset to zero before the clock is applied. **(8)**

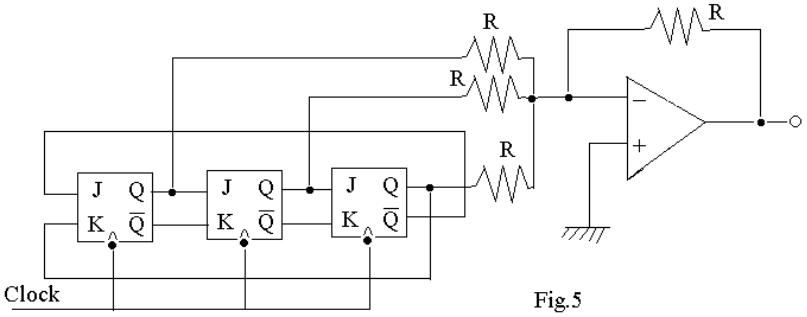


Fig.5

b. (i) How many flip flops are required to build a binary counter circuit to count from 0 to 1023?
(ii) What is the frequency of the output of last flip flop for an input clock frequency of 5 MHz?
(iii) What is the counter's MOD number?
(iv) If the counter is initially at zero, what will it hold after 2060 pulses?
(v) Does the maximum frequency of a counter depend on the modulus for
- Synchronous counter?
- Ripple counter?

Explain. **(6)**

Q.10 a. What is the difference between a 2D organised memory and $2\frac{1}{2}$D organisation? Illustrate the $2\frac{1}{2}$D memory organisation for a 16 word, 1 bit / word memory. **(7)**

b. Explain the difference between PLD, PAL and PLA. **(3)**

c. Illustrate with a block diagram, 4M x 1 DRAM organisation using 8192 column 512 row cell array. **(4)**

Q.11 Write explanatory notes on any **TWO** :
(i) Sequence Generators.
(ii) Single Amplifier Biquad.
(iii) Analog Multipliers.
(iv) Switched capacitor filters. **(7 x 2 = 14)**

JUNE/2004

Code: A-09/C-03/T-03 **Subject: ANALOG & DIGITAL ELECTRO**
Time: 3 Hours **Max. Marks: 1**

NOTE: There are 11 Questions in all.

- **Question 1 is compulsory and carries 16 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Answer any THREE Questions each from Part I and Part II. Each of these questions carries 14 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x8)

a. The magnitude response $|H(j\omega)|$ of a Butterworth filter of order N has maximally flat characteristics because

(A) first N derivatives of $|H(j\omega)|$ are equal to 0 at $\omega = 0$.

(B) first N-1derivatives of $|H(j\omega)|$ are equal to 0 at $\omega = 0$.

(C) first N-1 derivatives of $|H(j\omega)|$ are equal to 0 at $\omega = \infty$.

(D) first N derivatives of $|H(j\omega)|$ are equal to 0 at $\omega = \infty$.

b. Input impedance of the OpAmp circuit shown in the fig.1 is

(A) $R_2 + 2R_1$

(B) $R_2 + \frac{R_1}{2}$.

(C) $2R_1$.

(D) $\frac{R_1}{2}$.

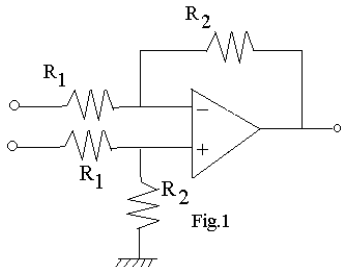


Fig.1

c. Output V_0 for $V_i = 1V$ dc for the circuit shown in the fig.2 will be

(A) 1.0 V.
(B) -0.5 V.
(C) 0.5 V.
(D) 0.0 V.

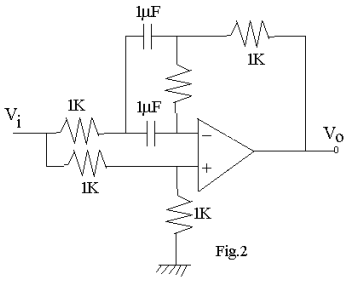


Fig.2

d. The Boolean expression $f(A,B,C,D) = \overline{A}C\overline{B} + BC\overline{D} + A\overline{C}D$ can equivalently be written, in terms of its minterms, as

(A) $\sum m(2,3,6,14,9,13)$. **(B)** $\sum m(3,4,6,14,9,13)$.

(C) $\sum m(2,3,6,14,8,12)$. **(D)** $\sum m(2,3,5,15,9,13)$.

e. The T-input of a negative edge triggered has been tied to logic '1'. If its clock input is as shown in the fig.3, then ON and OFF time of its $\overline{Q}$ out will be, respectively

(A) 0.2 ms and 1.8 ms.
(B) 1.8 ms and 0.2 ms.
(C) 0.5 ms and 0.5 ms.
(D) 1.0 ms and 1.0 ms.

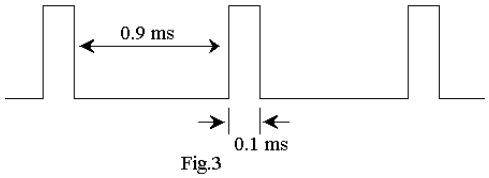


Fig.3

f. Immediately after the inputs to a NAND RS flipflop are simultaneously switched from 00 to 11, the output Q of the flipflop will
(A) be equal to '0'. **(B)** be equal to '1'.
(C) race around. **(D)** be unpredictable.

g. The circuit shown in the fig.4 is a
(A) flipflop.
(B) sequential circuit.
(C) combinational circuit.
(D) parity checker.

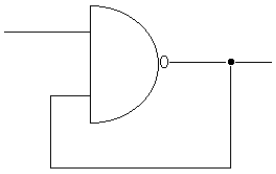


Fig.4

h. A MOS differential amplifier has a large gain because
(A) the current through each driver transistor is a constant.
(B) sum of currents through both driver transistors is a constant.
(C) the load is a current source and offers a large resistance.
(D) there is a no feedback in the circuit.

PART I
Answer any THREE Questions. Each question carries 14 marks.

Q.2 The OpAmp shown in the circuit of fig.5 has an open loop gain of 10000, input impedance of 1MΩ and an output impedance of 1KΩ.

(i) Determine $V = V_+ - V_-$ if –2.1V is applied between terminals A and B. **(5)**

(ii) Find the gain $\frac{V_o}{V_i}$ of this amplifier. **(5)**

(iii) Find the gain of the amplifier when the input has a source resistance of 1KΩ. **(4)**

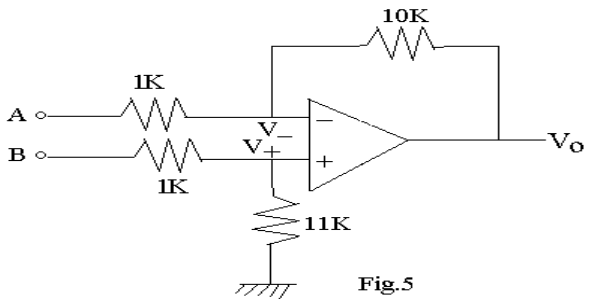


Fig.5

Q.3 Consider the function $H(s) = K\frac{s^2 - as + b}{s^2 + as + b}$.

(i) Draw its pole-zero diagram. **(2)**
(ii) Sketch magnitude and phase responses of this function. **(4)**
(iii) For K=1, draw a passive circuit to realize H(s). **(5)**
(iv) Draw a block diagram circuit to realize this function using integrators, summers and multipliers. **(3)**

Q.4 Explain the working of a 12-bit dual-slope analog to digital converter using appropriate diagrams and derive the relevant expression for the digital output. If the input voltage is in range (0V, 10V) and the counter in the converter is given a clock of 1 MHz, determine

(i) the time taken for output of the integrator to reach its maximum value. **(8)**

(ii) conversion time for input voltage = 5V, assuming reference voltage of –10V. **(6)**

Q.5 a. Through proper sketches explain the electron density distribution in the base of a n-p-n Bipolar Junction Transistor when

(iv) in Active region

(v) in Saturation.

How will the explanation be different for a p-n-p transistor? **(6)**

b. The input voltage V switches from +5V to –10V in diode circuit shown in the fig.6. Sketch the current through the diode and explain various regions of this waveform. **(8)**

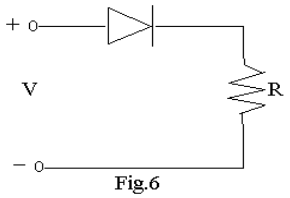


Fig.6

Q.6 With short notes on any **TWO** of the following:

(i) DC level shifting in OpAmps.

(ii) Sample-and-Hold circuits and their applications.

(iii) Sensitivity of a single OpAmp Biquad.

(iv) MOS operational amplifiers. **(14)**

PART II

Answer any THREE Questions. Each question carries 14 marks.

Q.7 a. A portion of TTL gate circuit is shown in the Fig.7(a), where the transistor Q has $\beta = 100$. Base-to-emitter voltage of the transistor is equal to 0.7V when it is in active region and 0.75V when Q is in saturation. Determine the output voltage V if the current I=2.5mA. **(6)**

b. Both NMOS and PMOS transistors in the circuit of Fig.7(b) have a threshold voltage of 2V and equal characteristic constants. Determine the value of input voltage V_i and the range of output voltage for which both transistors will be in saturation. **(8)**

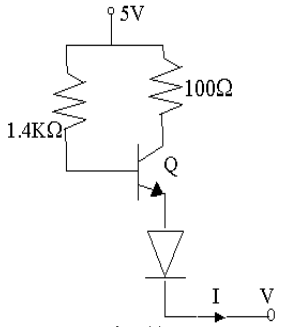


Fig.7(a)

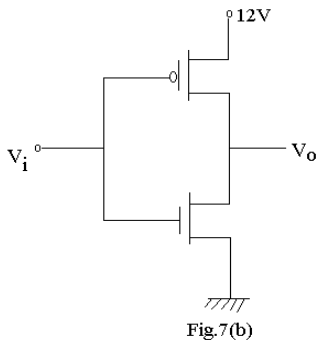
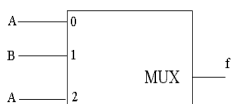


Fig.7(b)

Q.8 a. Determine the Boolean function implemented by the multiplexer circuit shown in the fig.8 (a). **(4)**



b. A 3-to-8 decoder has two enable inputs E1 and $\overline{E2}$ as shown in fig.8 (b). Write a truth table showing the outputs $O_0 - O_7$ in terms of inputs $A_0 - A_7$. **(5)**

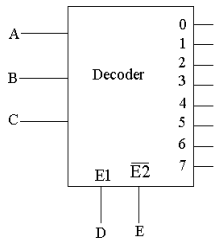


Fig.8(b)

c. With the help of a diagram using Full-adders, explain the working of a 4-bit parallel addition/subtraction of 2's complement numbers. **(5)**

Q.9 a. Explain the working of a positive-edge-triggered Master-Slave JK flipflop. What are its advantages over a normal JK flipflop? If all NAND gates used in the flipflop have a propagation delay of 5 ns, compute the delay of the Master-Slave. **(6)**

b. Design a circuit to generate the sequence 100010 using JK flipflops and logic gates as required. **(8)**

Q.10 a. What is the function of the circuit shown in the fig.9? Explain its working. **(4)**

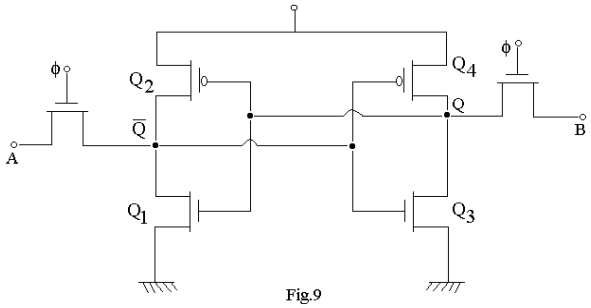


Fig.9

b. Draw the circuit of a CMOS static RAM cell and explain its operation. **(4)**

c. Three negative edge triggered flipflops having inputs $J_0 K_0$, $J_1 K_1$ and $J_2 K_2$ respectively, are connected to make a counter such that $J_0 = \overline{Q_2}, K_0 = 1, J_1 = K_1 = 1, J_2 = Q_1 Q_0$

Starting with $Q_2 Q_1 Q_0 = 000$, what sequence(s) of states will the counter go through? **(6)**

Q.11 Write short notes on any **THREE** of the following:

(i) Emitter-Coupled OR gate.
(ii) CMOS logic gates.
(iii) BJT inverter.
(iv) Schottky diodes and its applications in digital circuits. **(14)**